

Am27C4096

4 Megabit (256 K x 16-Bit) CMOS EPROM

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
 - Speed options as fast as 90 ns
- **Low power consumption**
 - 100 μ A maximum CMOS standby current
- **JEDEC-approved pinout**
 - Plug-in upgrade of 1 Mbit and 2 Mbit EPROMs
 - 40-pin DIP/PDIP
 - 44-pin PLCC
- **Single +5 V power supply**
- **$\pm 10\%$ power supply tolerance standard**
- **100% Flashrite programming**
 - Typical programming time of 32 seconds
- **Latch-up protected to 100 mA from -1 V to $V_{CC} + 1$ V**
- **High noise immunity**

GENERAL DESCRIPTION

The Am27C4096 is a 4 Mbit, ultraviolet erasable programmable read-only memory. It is organized as 256 Kwords, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. The Am27C4096 is ideal for use in 16-bit microprocessor systems. The device is available in windowed ceramic DIP packages, and plastic one time programmable (OTP) PDIP and PLCC packages.

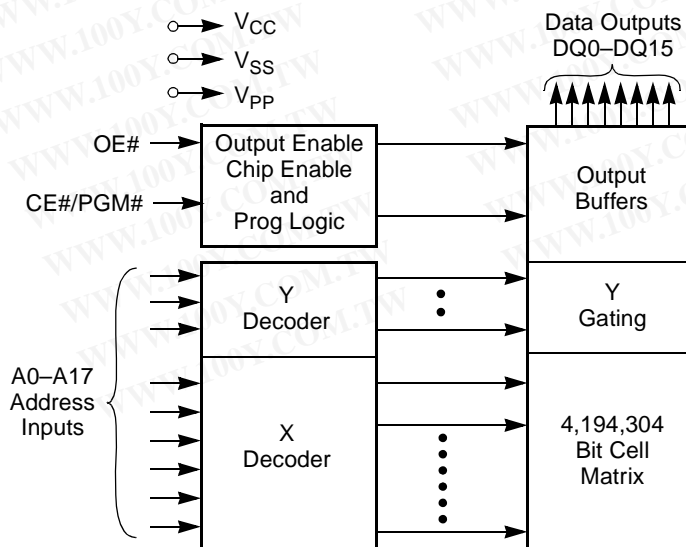
Data can be typically accessed in less than 90 ns, allowing high-performance microprocessors to operate without any WAIT states. The device offers separate Output Enable (OE#) and Chip Enable (CE#) controls,

thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 125 μ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The device supports AMD's Flashrite programming algorithm (100 μ s pulses), resulting in a typical programming time of 32 seconds.

BLOCK DIAGRAM



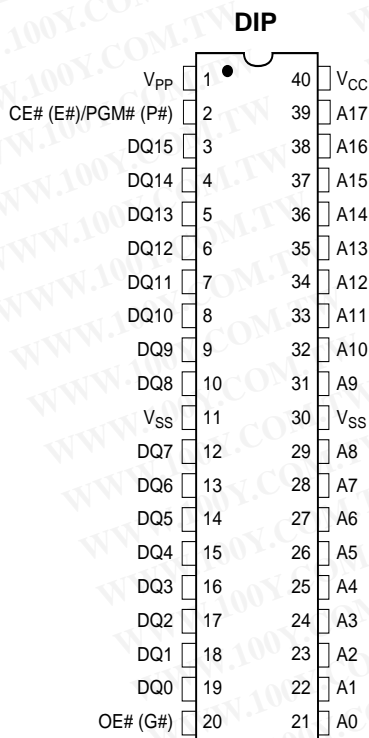
11408F-1

PRODUCT SELECTOR GUIDE

Family Part Number		Am27C4096					
Speed Options	$V_{CC} = 5.0\text{ V} \pm 5\%$	-95	-105				-255
	$V_{CC} = 5.0\text{ V} \pm 10\%$		-100	-120	-150	-200	
Max Access Time (ns)		90	100	120	150	200	250
CE# (E#) Access (ns)		90	100	120	150	200	250
OE# (G#) Access (ns)		50	50	50	65	75	75

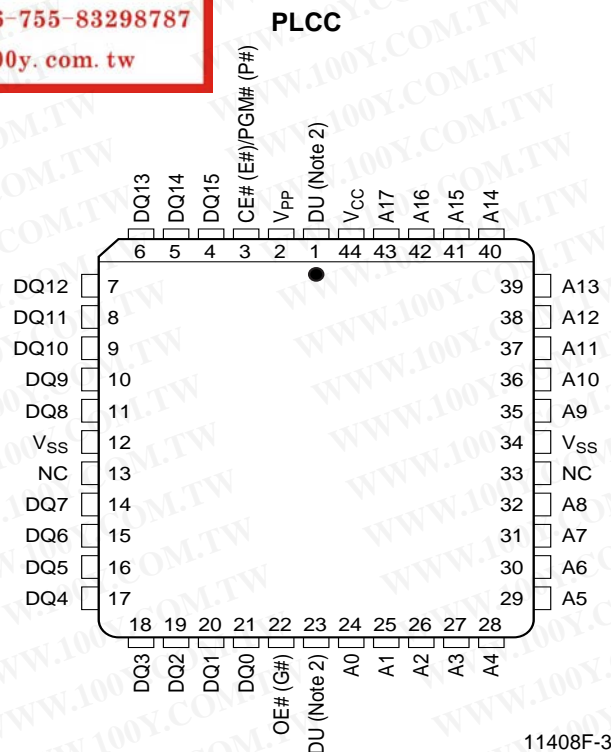
CONNECTION DIAGRAMS

Top View



11408F-2

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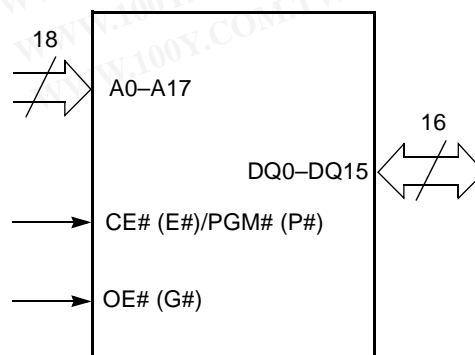
Notes:

1. JEDEC nomenclature is in parenthesis.
2. Don't use (DU) for PLCC.

PIN DESIGNATIONS

A0–A17 = Address Inputs
 CE# (E#)/PGM# (P#) = Chip Enable Input/
 Program Enable Input
 DQ0–DQ15 = Data Input/Outputs
 OE# (G#) = Output Enable Input
 V_{CC} = V_{CC} Supply Voltage
 V_{PP} = Program Voltage Input
 V_{SS} = Ground

LOGIC SYMBOL

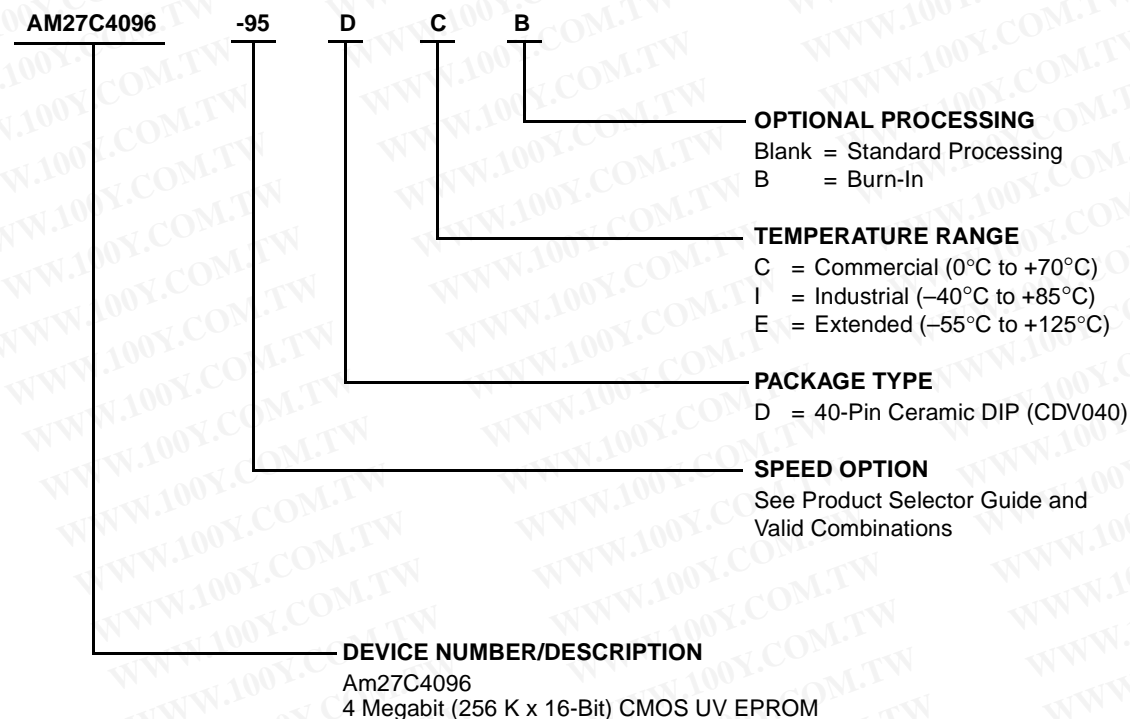


11408F-4

ORDERING INFORMATION

UV EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
AM27C4096-95 $V_{CC} = 5.0 \text{ V} \pm 5\%$	DC, DCB
AM27C4096-100	DC, DCB, DI, DIB
AM27C4096-105 $V_{CC} = 5.0 \text{ V} \pm 5\%$	
AM27C4096-120	
AM27C4096-150	DC, DCB, DE, DEB, DI, DIB
AM27C4096-200	
AM27C4096-255 $V_{CC} = 5.0 \text{ V} \pm 5\%$	DC, DCB, DI, DIB

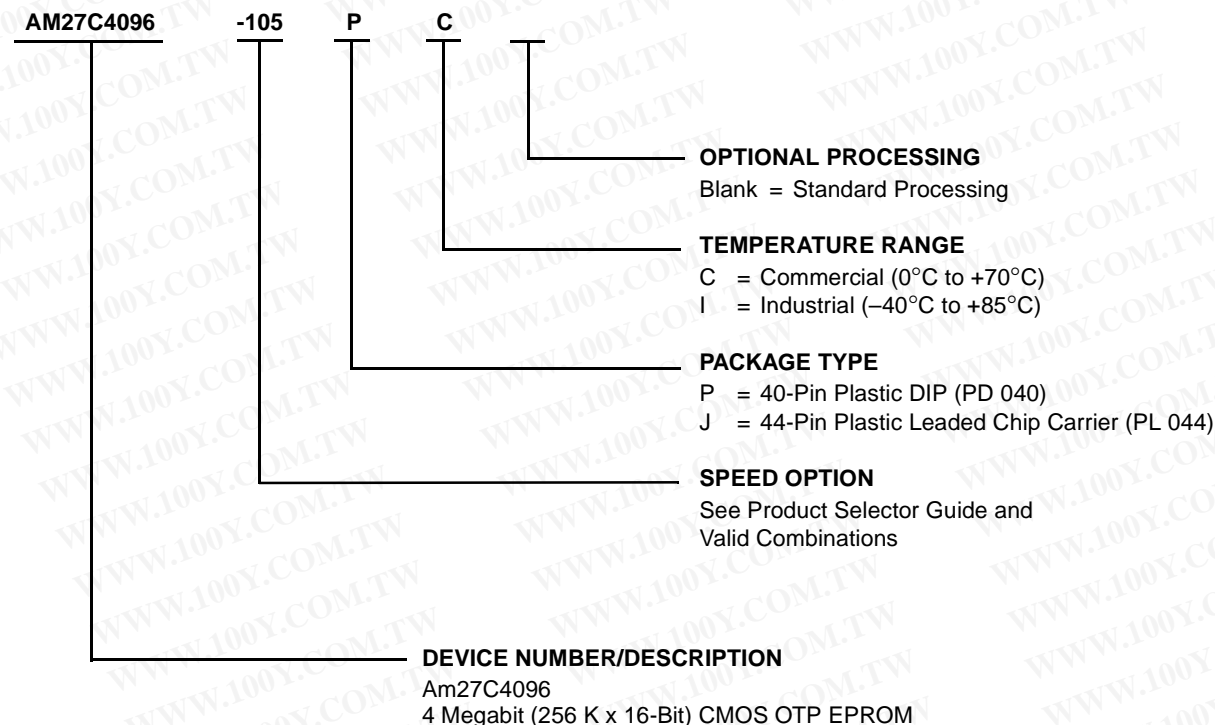
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
AM27C4096-105 $V_{CC} = 5.0 \text{ V} \pm 5\%$	PC, JC
AM27C4096-120	PC, PI, JC, JI
AM27C4096-150	
AM27C4096-200	
AM27C4096-255 $V_{CC} = 5.0 \text{ V} \pm 5\%$	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Device Erasure

In order to clear all locations of their programmed contents, the device must be exposed to an ultraviolet light source. A dosage of 15 W seconds/cm² is required to completely erase the device. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 μW/cm² for 15 to 20 minutes. The device should be directly under and about one inch from the source, and all filters should be removed from the UV light source prior to erasure.

Note that all UV erasable devices will erase with light sources having wavelengths shorter than 4000 Å, such as fluorescent light and sunlight. Although the erasure process happens over a much longer time period, exposure to any light source should be prevented for maximum system reliability. Simply cover the package window with an opaque label or substance.

Device Programming

Upon delivery, or after each erasure, the device has all of its bits in the “ONE”, or HIGH state. “ZEROS” are loaded into the device through the programming procedure.

The device enters the programming mode when 12.75 V ± 0.25 V is applied to the V_{PP} pin, and CE#/PGM# is at V_{IL} and OE# is at V_{IH}.

For programming, the data to be programmed is applied 16 bits in parallel to the data pins.

The flowchart in the Programming section (Section 5, Figure 5-1) shows AMD's Flashrite algorithm. The Flashrite algorithm reduces programming time by using a 100 μs programming pulse and by giving each address only as many pulses to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum pulses allowed is reached. This process is repeated while sequencing through each address of the device. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V_{CC} = V_{PP} = 5.25 V.

Please refer to Section 5 for additional programming information and specifications.

Program Inhibit

Programming different data to multiple devices in parallel is easily accomplished. Except for CE#/PGM#, all like inputs of the devices may be common. A TTL low-level program pulse applied to one device's CE#/PGM# input with V_{PP} = 12.75 V ± 0.25 V and OE# HIGH will program that particular device. A high-level

CE#/PGM# input inhibits the other devices from being programmed.

Program Verify

A verification should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with OE# at V_{IL}, CE#/PGM# at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Autoselect Mode

The autoselect mode provides manufacturer and device identification through identifier codes on DQ0–DQ7. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force V_H on address line A9. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} (that is, changing the address from 00h to 01h). All other address lines must be held at V_{IL} during the autoselect mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. Both codes have odd parity, with DQ7 as the parity bit.

Read Mode

To obtain data at the device outputs, Chip Enable (CE#/PGM#) and Output Enable (OE#) must be driven low. CE#/PGM# controls the power to the device and is typically used to select the device. OE# enables the device to output data, independent of device selection. Addresses must be stable for at least t_{ACC}–t_{OE}. Refer to the Switching Waveforms section for the timing diagram.

Standby Mode

The device enters the CMOS standby mode when CE#/PGM# is at V_{CC} ± 0.3 V. Maximum V_{CC} current is reduced to 100 μA. The device enters the TTL-standby mode when CE#/PGM# is at V_{IH}. Maximum V_{CC} current is reduced to 1.0 mA. When in either standby mode, the device places its outputs in a high-impedance state, independent of the OE# input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function provides:

- low memory power dissipation, and
- assurance that output bus contention will not occur.

CE#/PGM# should be decoded and used as the primary device-selecting function, while OE# be made a

common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of

these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode	CE#/PGM#	OE#	A0	A9	V _{PP}	Outputs
Read	V _{IL}	V _{IL}	X	X	X	D _{OUT}
Output Disable	V _{IL}	V _{IH}	X	X	X	High Z
Standby (TTL)	V _{IH}	X	X	X	X	High Z
Standby (CMOS)	V _{CC} \pm 0.3 V	X	X	X	X	High Z
Program	V _{IL}	V _{IH}	X	X	V _{PP}	D _{IN}
Program Verify	V _{IH}	V _{IL}	X	X	V _{PP}	D _{OUT}
Program Inhibit	V _{IH}	X	X	X	V _{PP}	High Z
Autoselect (Note 3)	Manufacturer Code	V _{IL}	V _{IL}	V _H	X	01h
	Device Code	V _{IL}	V _{IH}	V _H	X	19h

Notes:

1. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$.
2. $X = \text{Either } V_{IH} \text{ or } V_{IL}$.
3. $A1\text{--}A8 \text{ and } A10\text{--}17 = V_{IL}$.
4. See DC Programming Characteristics for V_{PP} voltage during programming.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature

OTP Products -65°C to $+125^{\circ}\text{C}$

All Other Products -65°C to $+150^{\circ}\text{C}$

Ambient Temperature

with Power Applied -55°C to $+125^{\circ}\text{C}$

Voltage with Respect to V_{SS}

All pins except A9, V_{PP} , V_{CC} . . . -0.6 V to $V_{CC} + 0.6\text{ V}$

A9 and V_{PP} (Note 2) -0.6 V to 13.5 V

V_{CC} (Note 1) -0.6 V to 7.0 V

Notes:

1. Minimum DC voltage on input or I/O pins -0.5 V . During voltage transitions, the input may overshoot V_{SS} to -2.0 V for periods of up to 20 ns . Maximum DC voltage on input and I/O pins is $V_{CC} + 5\text{ V}$. During voltage transitions, input and I/O pins may overshoot to $V_{CC} + 2.0\text{ V}$ for periods up to 20 ns .
2. Minimum DC input voltage on A9 is -0.5 V . During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to -2.0 V for periods of up to 20 ns . A9 and V_{PP} must not exceed $+13.5\text{ V}$ at any time.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) 0°C to $+70^{\circ}\text{C}$

Industrial (I) Devices

Ambient Temperature (T_A) -40°C to $+85^{\circ}\text{C}$

Extended (E) Devices

Ambient Temperature (T_A) -55°C to $+125^{\circ}\text{C}$

Supply Read Voltages

V_{CC} for $\pm 5\%$ devices $+4.75\text{ V}$ to $+5.25\text{ V}$

V_{CC} for $\pm 10\%$ devices $+4.50\text{ V}$ to $+5.50\text{ V}$

Operating ranges define those limits between which the functionality of the device is guaranteed.

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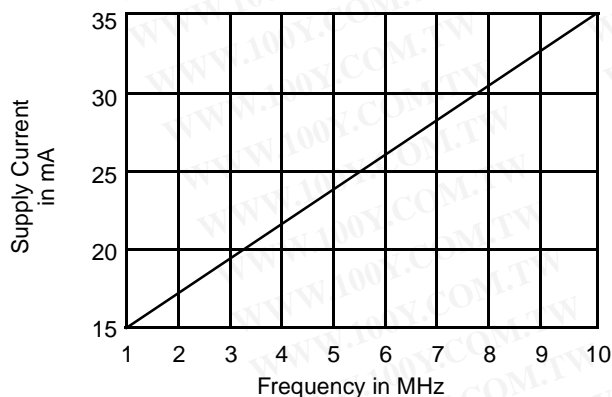
DC CHARACTERISTICS over operating range (unless otherwise specified)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400 \mu A$		2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$			0.45	V
V_{IH}	Input HIGH Voltage			2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage			-0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0 \text{ V to } V_{CC}$			1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0 \text{ V to } V_{CC}$			5.0	μA
I_{CC1}	V_{CC} Active Current (Note 2)	$CE\# = V_{IL}, f = 5 \text{ MHz}, I_{OUT} = 0 \text{ mA}$	C/I Devices		50	mA
			E Devices		60	
I_{CC2}	V_{CC} TTL Standby Current	$CE\# = V_{IH}$			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$CE\# = V_{CC} \pm 0.3 \text{ V}$			100	μA
I_{PP1}	V_{PP} Supply Current (Read)	$CE\# = OE\# = V_{IL}, V_{PP} = V_{CC}$			100	μA

Caution: The device must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.

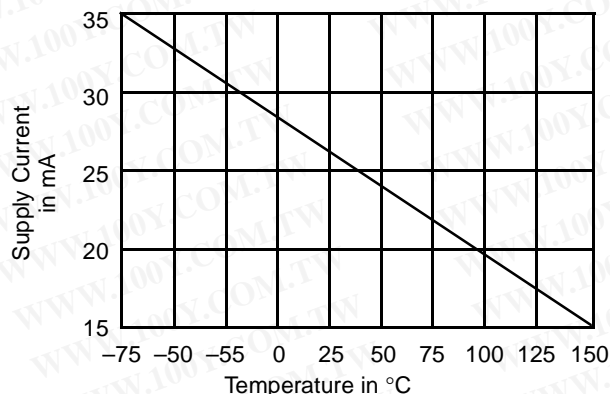
Notes:

- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
- I_{CC1} is tested with $OE\# = V_{IH}$ to simulate open outputs.
- Minimum DC Input Voltage is -0.5 V. During transitions, the inputs may overshoot to -2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is $V_{CC} + 0.5 \text{ V}$, which may overshoot to $V_{CC} + 2.0 \text{ V}$ for periods less than 20 ns.



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Figure 1. Typical Supply Current vs. Frequency
 $V_{CC} = 5.5 \text{ V}, T = 25^\circ\text{C}$

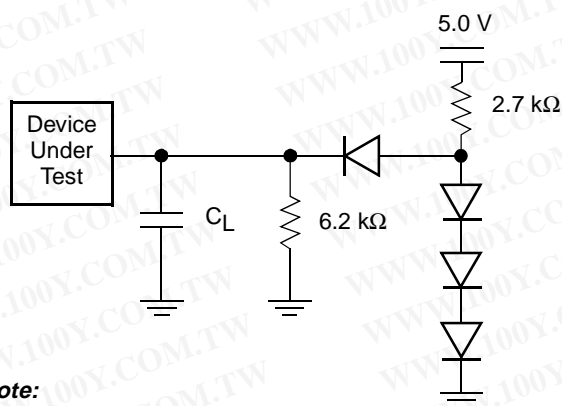


11408F-6

Figure 2. Typical Supply Current vs. Temperature
 $V_{CC} = 5.5 \text{ V}, f = 5 \text{ MHz}$

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TEST CONDITIONS



Note:
Diodes are IN3064 or equivalents.

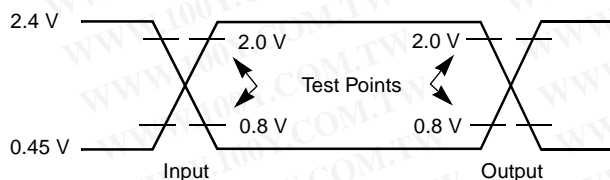
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Figure 3. Test Setup

Table 1. Test Specifications

Test Condition	All	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	100	pF
Input Rise and Fall Times	≤ 20	ns
Input Pulse Levels	0.45–2.4	V
Input timing measurement reference levels	0.8, 2.0	V
Output timing measurement reference levels	0.8, 2.0	V

SWITCHING TEST WAVEFORM



Note: For $C_L = 100$ pF.

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KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

AC CHARACTERISTICS

Parameter Symbols		Description	Test Setup	Am27C4096						Unit
JEDEC	Standard			-95	-105	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	CE#, OE# = V_{IL} Max	90	100	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL} Max	90	100	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	CE# = V_{IL} Max	50	50	50	65	75	75	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable High or Output Enable High to Output High Z, Whichever Occurs First	Max	30	30	40	40	40	60	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First	Min	0	0	0	0	0	0	ns

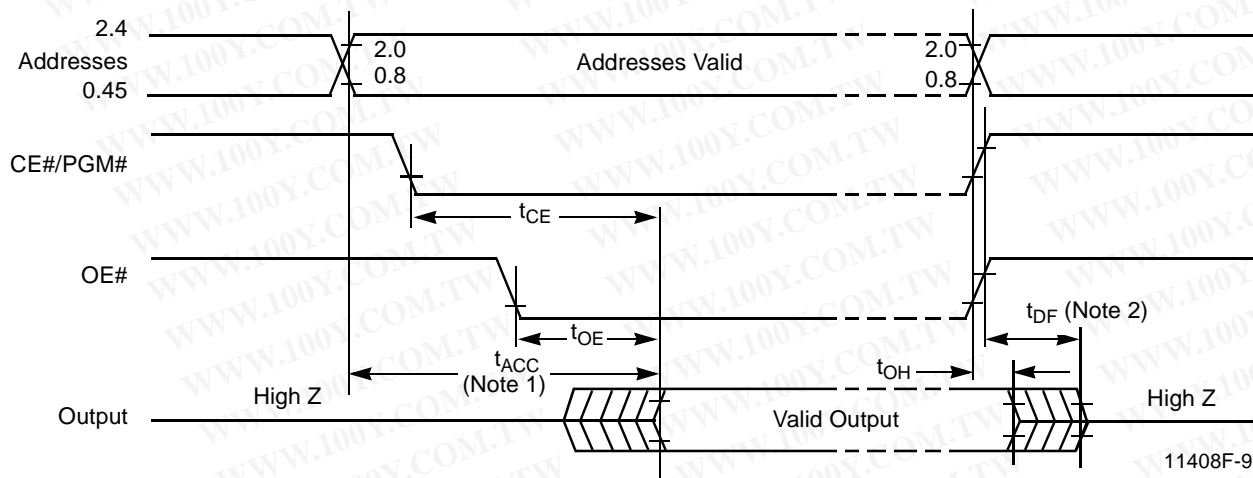
Caution: Do not remove the device from (or insert it into) a socket or board that has V_{PP} or V_{CC} applied.

Notes:

- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}
- This parameter is sampled and not 100% tested.
- Switching characteristics are over operating range, unless otherwise specified.
- See Figure 3 and Table 1 for test specifications.

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SWITCHING WAVEFORMS



Notes:

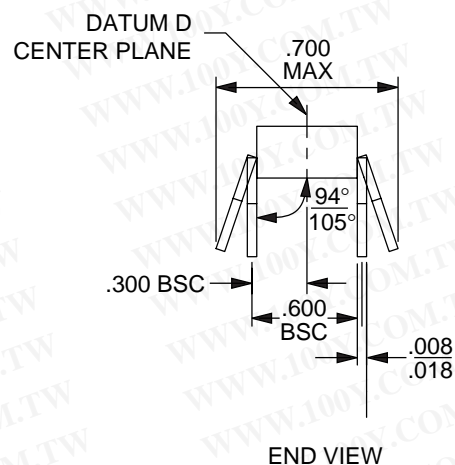
- OE# may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC} .
- t_{DF} is specified from OE# or CE#, whichever occurs first.

PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV040		PD 040		PL 044		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	$V_{IN} = 0$	10	13	6	8	10	13	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	10	13	8	10	12	14	pF

Notes:

- This parameter is only sampled and not 100% tested.
- $T_A = +25^\circ\text{C}$, $f = 1\text{ MHz}$.



16-000038H-3
CDV040
DF11
3-30-95 ae

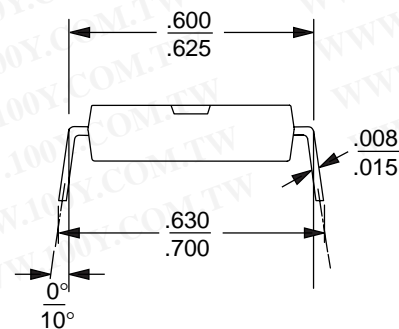
* For reference only. BSC is an ANSI standard for Basic Space Centering.

Top View Dimensions:

- Overall Width: 2.040
- Pin Pitch (Top): 2.080
- Pin 1 I.D. (Inner Diameter)
- Pin 1 Location: .045 (from left edge), .065 (from center line)
- Pin 1 to Pin 20 Distance: .005 MIN
- Pin 20 to Pin 21 Distance: .530
- Pin 21 to Pin 20 Distance: .580

Side View Dimensions:

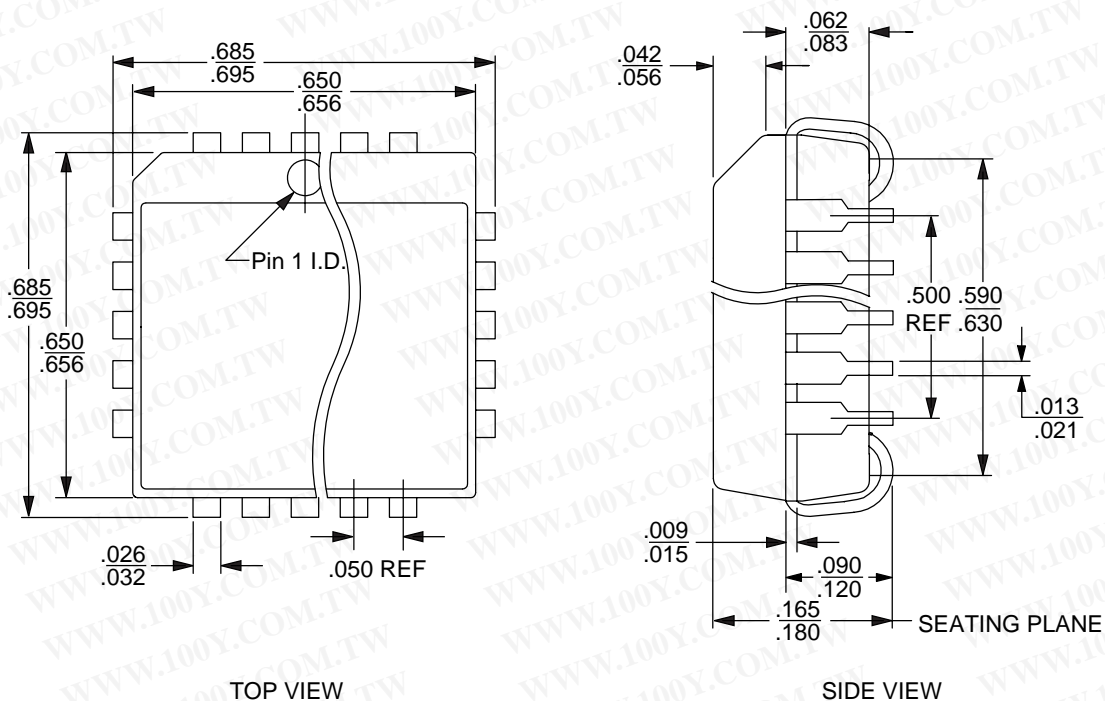
- Package Height: .140
- Pin Height: .225
- Pin Spacing (Side): .090
- Pin Spacing (Side): .110
- Pin Spacing (Side): .014
- Pin Spacing (Side): .022
- Pin Spacing (Side): .015
- Pin Spacing (Side): .060



16-038-SC_AF
PD 040
DG76
2-28-95 ae

PHYSICAL DIMENSIONS

PL 044—44-Pin Plastic Leaded Chip Carrier (measured in inches)



16-038-SQ
PL 044
EC80
11.3.97 lv

REVISION SUMMARY FOR AM27C4096

Revision F

Global

Changed formatting to match current data sheets.

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