

OPA131
OPA2131
OPA4131

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
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General Purpose FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

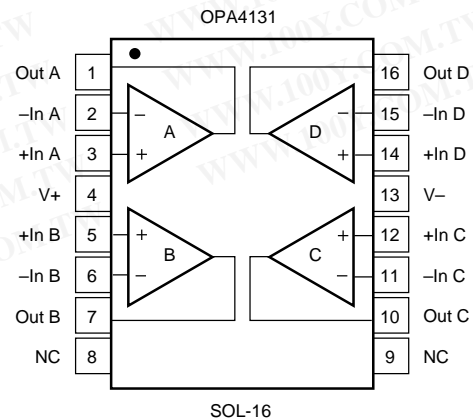
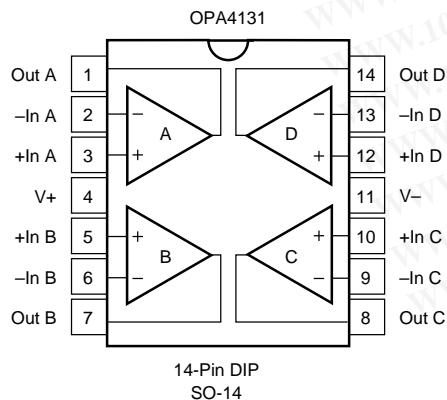
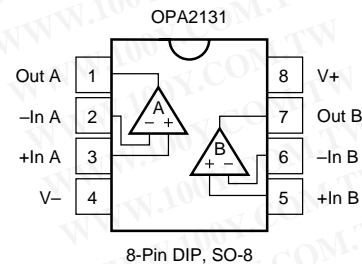
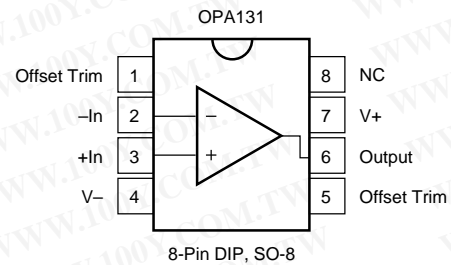
- FET INPUT: $I_b = 50\text{pA max}$
- LOW OFFSET VOLTAGE: $750\mu\text{V max}$
- WIDE SUPPLY RANGE: $\pm 4.5\text{V to } \pm 18\text{V}$
- SLEW RATE: $10\text{V}/\mu\text{s}$
- WIDE BANDWIDTH: 4MHz
- EXCELLENT CAPACITIVE LOAD DRIVE
- SINGLE, DUAL, QUAD VERSIONS

DESCRIPTION

The OPA131 series of FET-input op amps provides high performance at low cost. Single, dual and quad versions in industry-standard pinouts allow cost-effective design options.

The OPA131 series offers excellent general purpose performance, including low offset voltage, drift, and good dynamic characteristics.

Single, dual and quad versions are available in DIP and SOIC packages. Performance grades include commercial and industrial temperature ranges.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
 Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 2\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITION	OPA131PA, UA OPA2131PA, UA OPA4131PA, UA, NA			OPA131PJ, UJ OPA2131PJ, UJ OPA4131PJ, NJ			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage OPA131P, U models only vs Temperature ⁽¹⁾ vs Power Supply OPA131P, U models only	Operating Temperature Range $V_S = \pm 4.5\text{V to } \pm 18\text{V}$		± 0.2	± 1		*	± 1.5	mV
			± 0.2	0.75		*	*	mV
			± 2	± 10		*	*	$\mu\text{V}/^\circ\text{C}$
			50	200		*	*	$\mu\text{V}/\text{V}$
			50	100		*	*	$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT⁽²⁾ Input Bias Current vs Temperature Input Offset Current	$V_{CM} = 0\text{V}$		+5	± 50		*	*	pA
	$V_{CM} = 0\text{V}$		See Typical Curve	± 50		*	*	pA
NOISE Input Voltage Noise Noise Density, $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$			21			*		$\text{nV}/\sqrt{\text{Hz}}$
			16			*		$\text{nV}/\sqrt{\text{Hz}}$
			15			*		$\text{nV}/\sqrt{\text{Hz}}$
			15			*		$\text{nV}/\sqrt{\text{Hz}}$
			3			*		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection OPA131P, U models only	$V_{CM} = -12\text{V to } +14\text{V}$	$(V^-)+3$		$(V^+)-1$	*		*	V
		70	80		*	*		dB
		80	86					dB
INPUT IMPEDANCE Differential Common-Mode	$V_{CM} = 0\text{V}$		$10^{10} \parallel 1$			*		$\Omega \parallel \text{pF}$
			$10^{12} \parallel 3$			*		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN Open-Loop Voltage Gain OPA131P, U models only	$V_O = -12\text{V to } +12\text{V}$	94	110		*	*		dB
		100	110					dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.1% 0.01% Total Harmonic Distortion + Noise	$G = -1, 10\text{V Step}, C_L = 100\text{pF}$ $G = -1, 10\text{V Step}, C_L = 100\text{pF}$ 1kHz, $G = 1, V_O = 3.5\text{Vrms}$		4			*		MHz
			10			*		V/ μs
			1.5			*		μs
			2			*		μs
			0.0008			*		%
OUTPUT Voltage Output, Positive Negative Short-Circuit Current		$(V^+)-3$	$(V^+)-2.5$		*	*		V
		$(V^-)+3$	$(V^-)+2.5$	± 25	*	*		V mA
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_O = 0$		± 15			*		V
			± 4.5	± 18	*	*		V
			± 1.5	± 1.75		*	± 2	mA
TEMPERATURE RANGE Operating Range Storage Thermal Resistance, θ_{JA} 8-Pin DIP SO-8 Surface-Mount 14-Pin DIP SO-14, SOL-16 Surface-Mount		-40		+85	0		+70	$^\circ\text{C}$
		-40		+125	*		*	$^\circ\text{C}$
			100			*	*	$^\circ\text{C}/\text{W}$
			150			*	*	$^\circ\text{C}/\text{W}$
			80			*	*	$^\circ\text{C}/\text{W}$
			110			*	*	$^\circ\text{C}/\text{W}$

* Specifications same as OPA131PA, OPA131UA.

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at $T_J = 25^\circ\text{C}$.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V-	36V
Input Voltage	(V-) -0.7V to (V+) +0.7V
Output Short-Circuit ⁽¹⁾	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
Single		
OPA131PJ	8-Pin Plastic DIP	006
OPA131PA	8-Pin Plastic DIP	006
OPA131P	8-Pin Plastic DIP	006
OPA131UJ	SO-8 Surface-Mount	182
OPA131UA	SO-8 Surface-Mount	182
OPA131U	SO-8 Surface-Mount	182
Dual		
OPA2131PJ	8-Pin Plastic DIP	006
OPA2131PA	8-Pin Plastic DIP	006
OPA2131UJ	SO-8 Surface-Mount	182
OPA2131UA	SO-8 Surface-Mount	182
Quad		
OPA4131PJ	14-Pin Plastic DIP	010
OPA4131PA	14-Pin Plastic DIP	010
OPA4131UA	SOL-16 Surface-Mount	211
OPA4131NJ	SO-14 Surface-Mount	235
OPA4131NA	SO-14 Surface-Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
Single		
OPA131PJ	8-Pin Plastic DIP	0 to +70°C
OPA131PA	8-Pin Plastic DIP	-40°C to +85°C
OPA131P	8-Pin Plastic DIP	-40°C to +85°C
OPA131UJ	SO-8 Surface-Mount	0 to +70°C
OPA131UA	SO-8 Surface-Mount	-40°C to +85°C
OPA131U	SO-8 Surface-Mount	-40°C to +85°C
Dual		
OPA2131PJ	8-Pin Plastic DIP	0 to +70°C
OPA2131PA	8-Pin Plastic DIP	-40°C to +85°C
OPA2131UJ	SO-8 Surface-Mount	0 to +70°C
OPA2131UA	SO-8 Surface-Mount	-40°C to +85°C
Quad		
OPA4131PJ	14-Pin Plastic DIP	0 to +70°C
OPA4131PA	14-Pin Plastic DIP	-40°C to +85°C
OPA4131UA	SOL-16 Surface-Mount	-40°C to +85°C
OPA4131NJ	SO-14 Surface-Mount	0 to +70°C
OPA4131NA	SO-14 Surface-Mount	-40°C to +85°C



ELECTROSTATIC DISCHARGE SENSITIVITY

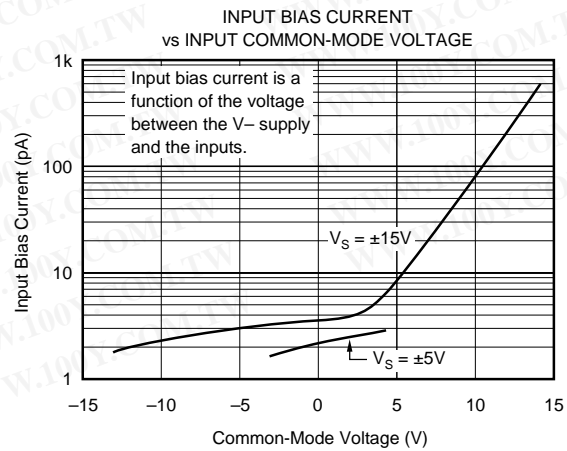
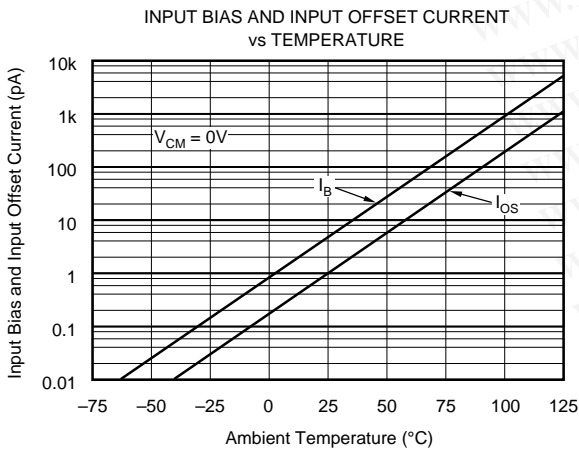
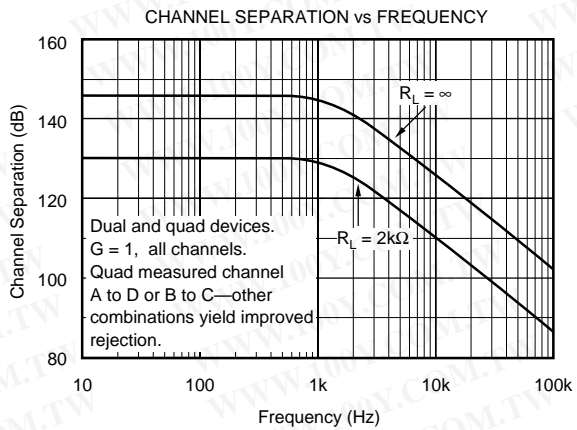
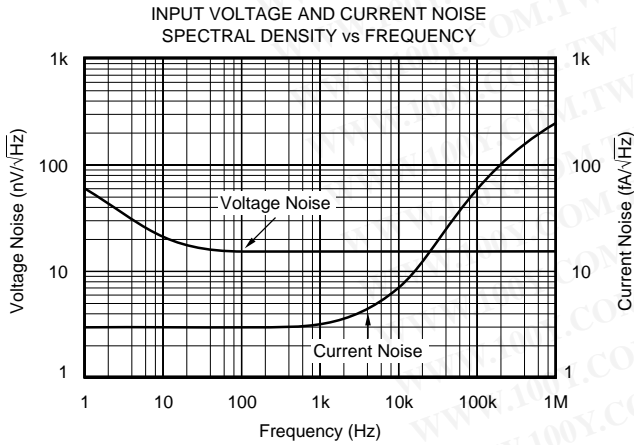
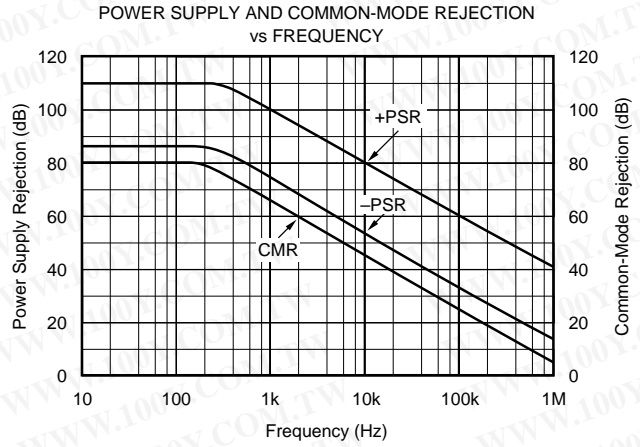
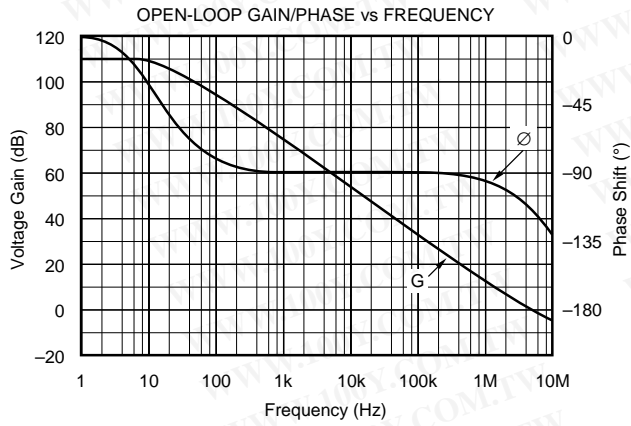
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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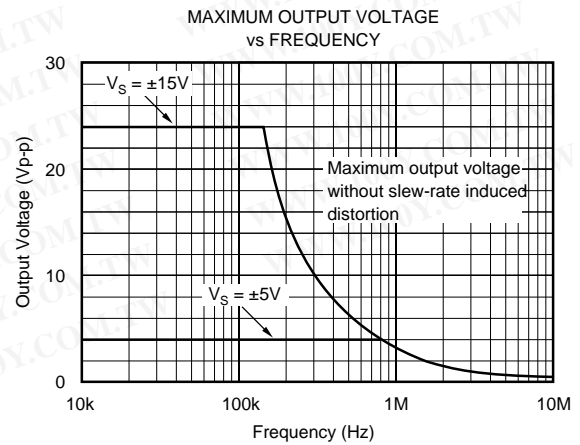
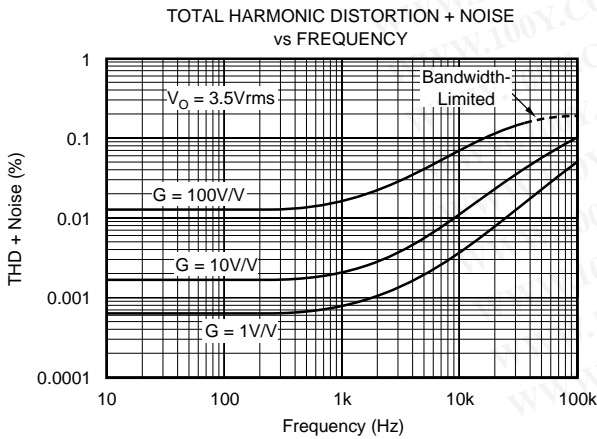
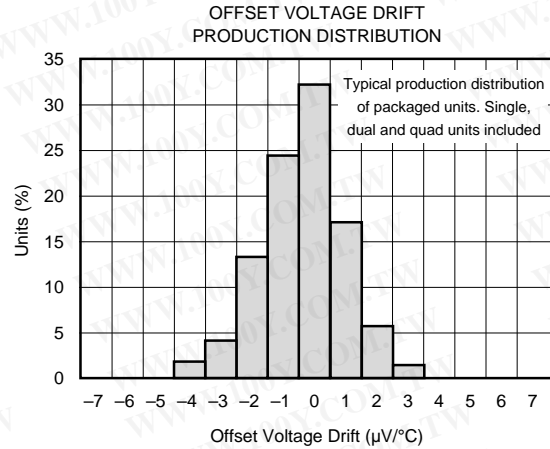
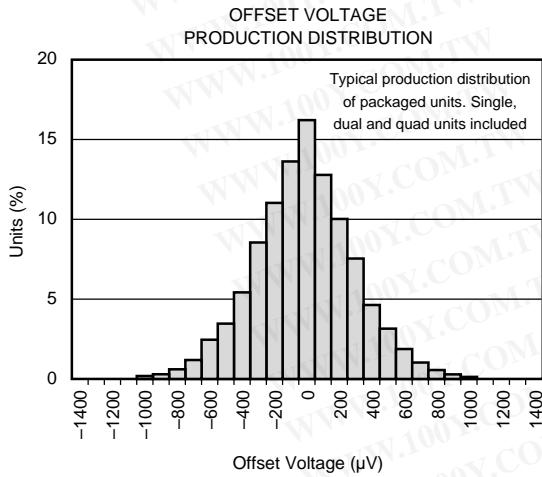
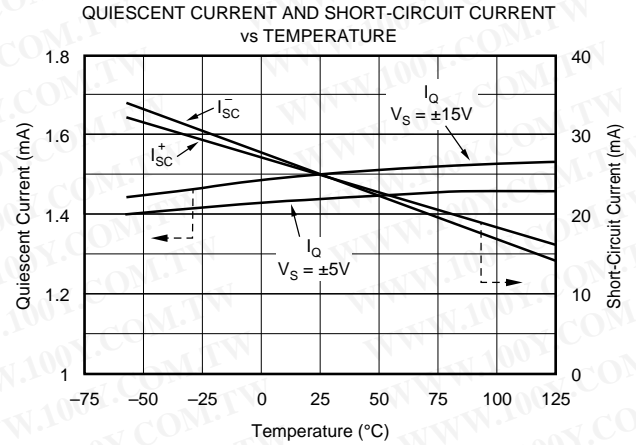
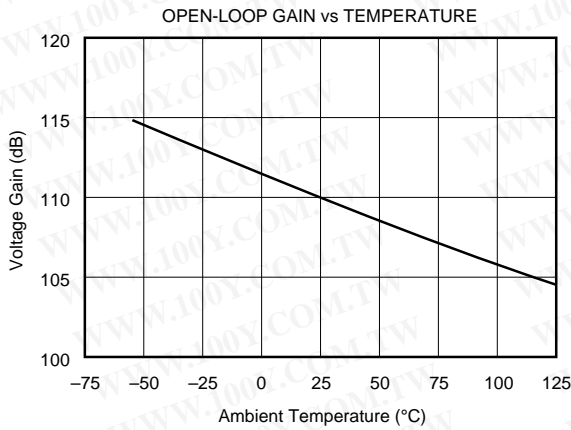
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 2\text{k}\Omega$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

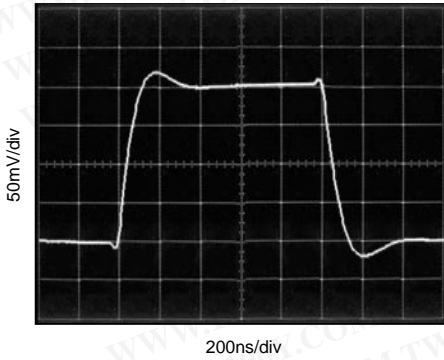
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 2\text{k}\Omega$, unless otherwise noted.



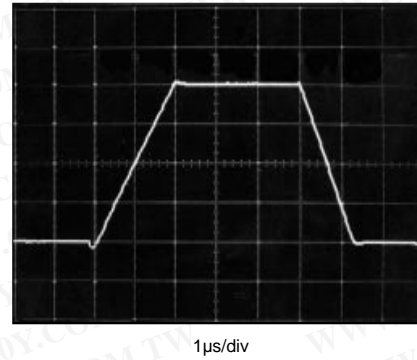
TYPICAL PERFORMANCE CURVES (CONT)

At $T_{CASE} = +25^{\circ}C$, $V_S = \pm 15V$, and $R_L = 2k\Omega$, unless otherwise noted.

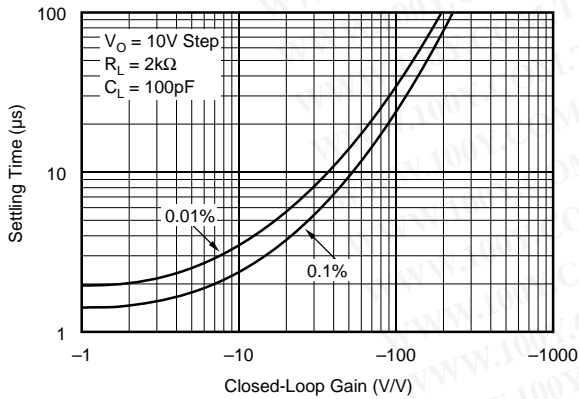
SMALL-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 300pF$



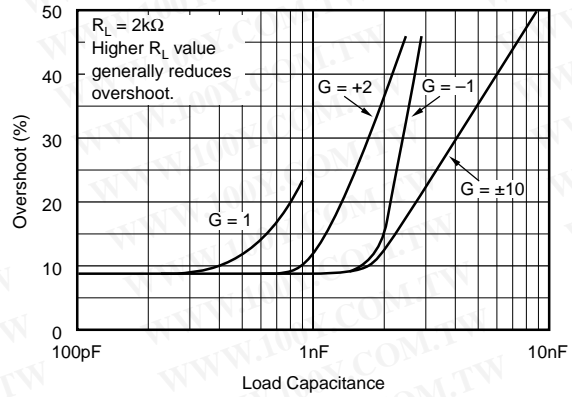
LARGE-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 300pF$



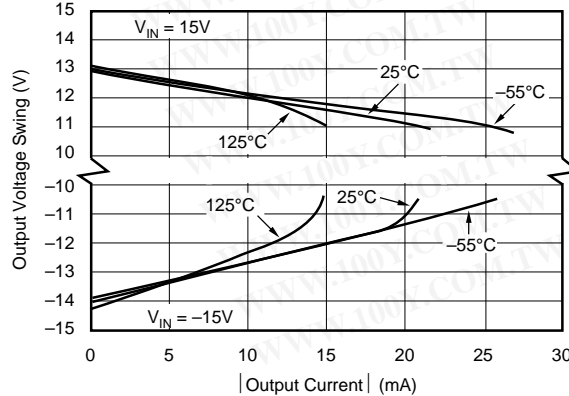
SETTLING TIME vs CLOSED-LOOP GAIN



SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



APPLICATIONS INFORMATION

OPA131 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA131 series op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OFFSET VOLTAGE TRIM

The OPA131 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not system offset or offset produced by the signal source.

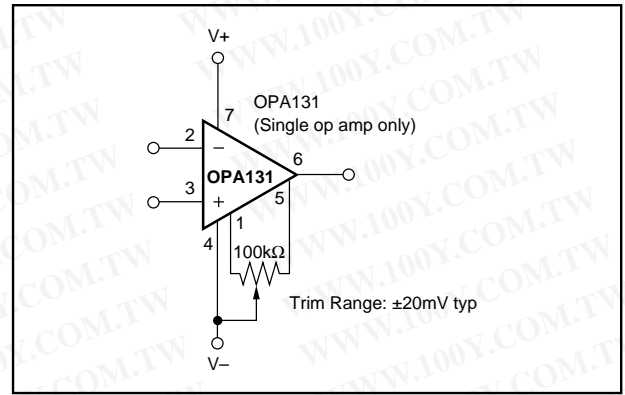


FIGURE 1. OPA131 Offset Voltage Trim Circuit.

INPUT BIAS CURRENT

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the typical performance curve “Input Bias Current vs Temperature.”

Input bias current also varies with common-mode voltage and power supply voltage. This variation is dependent on the voltage between the negative power supply and the common-mode input voltage. The effect is shown in the typical curve “Input Bias Current vs Common-Mode Voltage.”

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