**Thyristors** logic level BT169 series

#### GENERAL DESCRIPTION

#### Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose phase switching and control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

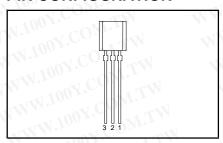
#### **QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	MAX.	UNIT
COWITT	BT169	B)	Dod		G	
$egin{array}{c} egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}$	Repetitive peak off-state voltages	200	400	500	600	V
I <sub>T(AV)</sub>	Average on-state current	0.5	0.5	0.5	0.5	Α
T <sub>(RMS)</sub>	RMS on-state current Non-repetitive peak on-state current	0.8 8	0.8 8	0.8 8	0.8 8	A A

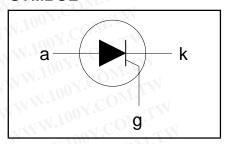
# **PINNING - TO92 variant**

Ī	PIN	DESCRIPTION
	1	anode
1	2	gate
	3	cathode
1	N	W.100Y.COM.TW

#### PIN CONFIGURATION



#### SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.		M	AX.	COL	UNIT
$V_{DRM}, V_{RRM}$	Repetitive peak off-state voltages	MMM.100X.CO	M-TV	<b>B</b> 200 <sup>1</sup>	<b>D</b> 400 <sup>1</sup>	<b>E</b> 500 <sup>1</sup>	<b>G</b> 600 <sup>1</sup>	V.V
I <sub>T(AV)</sub>	Average on-state current	half sine wave; T <sub>lead</sub> ≤ 83 °C	$O\overline{W}$	W	0	.5	nov.C	Α
I <sub>T(RMS)</sub>	RMS on-state current	all conduction angles	$CO_{M}$		0	.8 8		Α
I <sub>TSM</sub>	Non-repetitive peak	t = 10 ms	COM	, L '		8		CA.
	on-state current	t = 8.3 ms half sine wave; T <sub>i</sub> = 25 °C prior to surge	V.COD			9/// //		(,CO)
l <sup>2</sup> t	I <sup>2</sup> t for fusing	t = 10 ms		M.r.	0.	32		$A^2s$
dl <sub>⊤</sub> /dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 2 \text{ A}; I_{G} = 10 \text{ mA};$ $dI_{G}/dt = 100 \text{ mA/}\mu\text{s}$	007.C	$T_{MC}$	N 5	50		A/μs
$I_{GM}$	Peak gate current	WWW.	. Vāo.	Oh		1		A.
$V_{GM}$	Peak gate voltage	M.T.	705	COM	- 1	5		V
$V_{RGM}$	Peak reverse gate voltage	MIN.	1007		TW	5		V
P <sub>GM</sub>	Peak gate power	aver env 20 me period	N . 3=	1 CON		<u>ا</u>		W
P <sub>G(AV)</sub>	Average gate power Storage temperature	over any 20 ms period	-40	~ cO		.1 50		, V
$T_{stg}$	Operating junction temperature	CONT.TW WY	NW.10	ov.C	M.Ti	25 N		°C °C

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TWIN I MAY. COM TW September 1997 Rev 1.200

<sup>1</sup> Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

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#### THERMAL RESISTANCES

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R <sub>th j-lead</sub>	Thermal resistance junction to lead	X. COM.TW WWW.100X	.COM.TW	- N	60	K/W
$R_{\text{th j-a}}$	Thermal resistance junction to ambient	pcb mounted; lead length = 4mm	Y.CON.	150	-	K/W

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>GT</sub> OY.C	Gate trigger current	$V_D = 12 \text{ V}$ ; $I_T = 10 \text{ mA}$ ; gate open circuit	01.	50	200	μΑ
I <sub>1</sub>	Latching current	$V_{D}^{F} = 12 \text{ V}; I_{GT} = 0.5 \text{ mA}; R_{GK} = 1 \text{ k}\Omega$ $V_{D} = 12 \text{ V}; I_{GT} = 0.5 \text{ mA}; R_{GK} = 1 \text{ k}\Omega$	CY	2	N 6	mΑ
IH 100 X	Holding current	$V_D = 12 \text{ V}; I_{GT} = 0.5 \text{ mA}; R_{GK} = 1 \text{ k}\Omega$	00 -	2	.5	mA
V <sub>T</sub>	On-state voltage	$I_T = 1 \text{ A}$	. OC-Y.	1.2	1.35	V
$V_{GT}$	Gate trigger voltage	$\dot{V}_D = 12 \text{ V}$ ; $I_T = 10 \text{ mA}$ ; gate open circuit	100	0.5	0.8	l V
1 4.1	CO. TW	$V_D = V_{DRM(max)}$ ; $I_T = 10$ mA; $T_j = 125$ °C;	0.2	0.3	277	l V
	COM.	gate open circuit	1.10	$^{1}$ CO $_{M_{1}}$		1
$I_D, I_R$	Off-state leakage current	$ V_D = V_{DRM(max)}; V_B = V_{RRM(max)}; T_i = 125 °C;$	×1 +00	0.05	0.1	l mA
D, 'R	on state leakage current	$V_D = V_{DRM(max)}$ ; $V_R = V_{RRM(max)}$ ; $V_j = 125$ °C;	M.To.	0.00	) . U. I	''''

#### DYNAMIC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV <sub>D</sub> /dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125 °C;$ exponential waveform; $R_{CK} = 1 k\Omega$	MANN	25	CON	V/μs
t <sub>gt</sub>	Gate controlled turn-on time	$I_{TM} = 2 \text{ A}; V_D = V_{DRM(max)}; I_G = 10 \text{ mA};$ $dI_C/dt = 0.1 \text{ A/us}$	N-W	2	Y.C.O.	μs
t <sub>q</sub>	Circuit commutated turn-off time	$\begin{array}{l} V_{\text{DM}} = 67\% \ V_{\text{DRM(max)}}; \ T_j = 125 \ ^{\circ}\text{C}; \\ \text{exponential waveform;} \ R_{\text{GK}} = 1 \ \text{k}\Omega \\ I_{\text{TM}} = 2 \ \text{A}; \ V_{\text{D}} = V_{\text{DRM(max)}}; \ I_{\text{G}} = 10 \ \text{mA}; \\ dI_{\text{G}}/dt = 0.1 \ \text{A}/\mu\text{s} \\ V_{\text{D}} = 67\% \ V_{\text{DRM(max)}}; \ T_j = 125 \ ^{\circ}\text{C}; \\ I_{\text{TM}} = 1.6 \ \text{A}; \ V_{\text{R}} = 35 \ \text{V}; \ dI_{\text{TM}}/dt = 30 \ \text{A}/\mu\text{s}; \\ dV_{\text{D}}/dt = 2 \ \text{V}/\mu\text{s}; \ R_{\text{GK}} = 1 \ \text{k}\Omega \end{array}$	-NV	100	07.CC	μs

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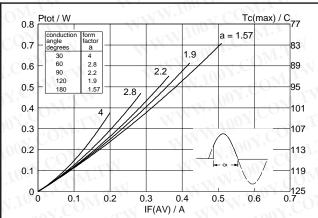


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{T(AV)}$ , where  $a = form \ factor = I_{T(RMS)} / I_{T(AV)}$ .

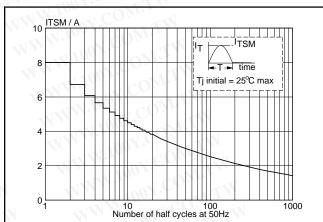


Fig.4. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents, f = 50 Hz.

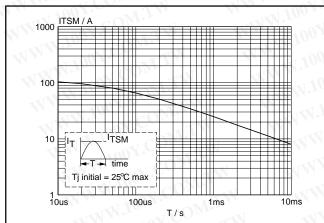


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \le 10$ ms.

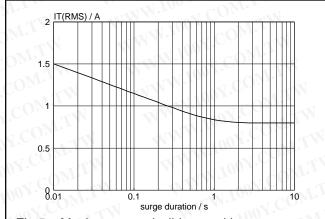


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents, f = 50 Hz;  $T_{lead} \le 83$  °C.

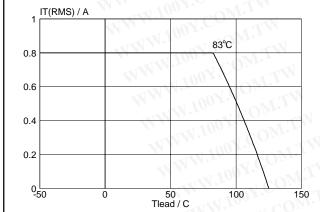
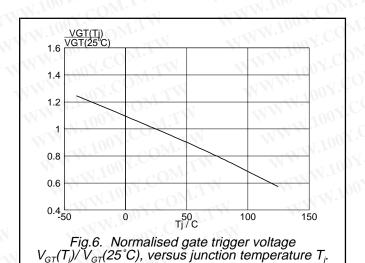


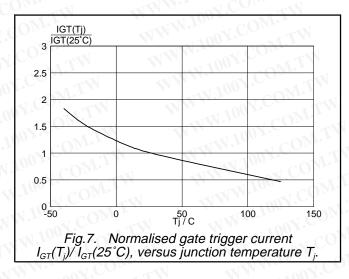
Fig.3. Maximum permissible rms current  $I_{T(RMS)}$ , versus lead temperature,  $T_{lead}$ .

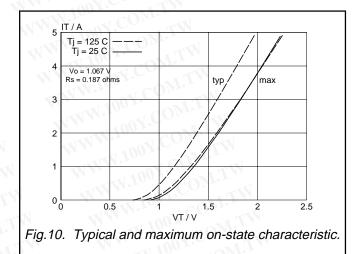


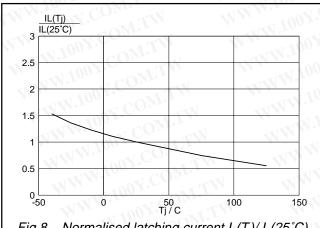
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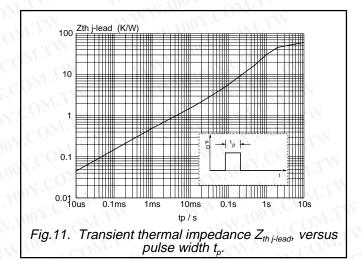
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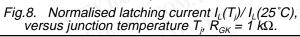
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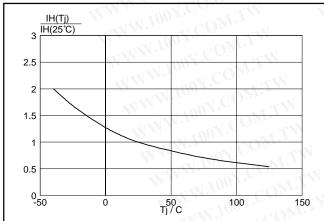












100

RGK = 1 kohms

10

10

Tj/C

100

150

dVD/dt (V/us)

1000

Fig.9. Normalised holding current  $I_H(T_i)/I_H(25^{\circ}C)$ , versus junction temperature  $T_i$ ,  $R_{GK}=1$  k $\Omega$ .

Fig.12. Typical, critical rate of rise of off-state voltage, dV<sub>D</sub>/dt versus junction temperature T<sub>i</sub>.

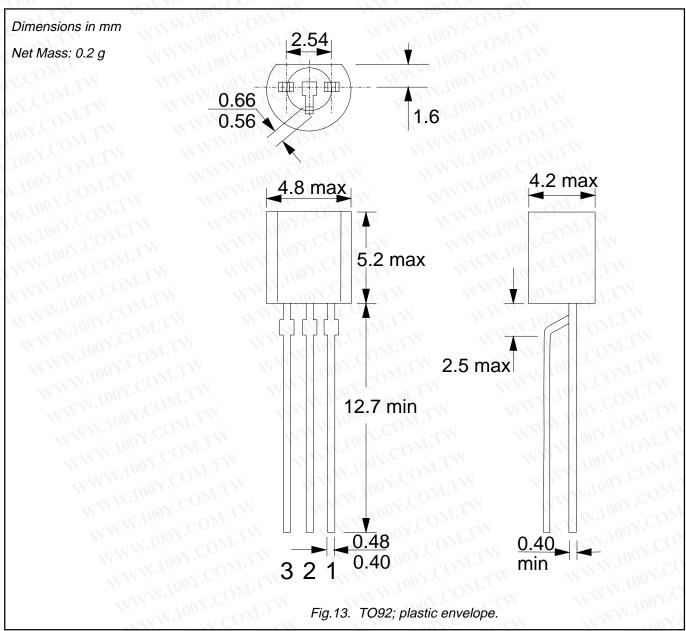
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#### **MECHANICAL DATA**



## Notes

1. Epoxy meets UL94 V0 at 1/8".

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#### **DEFINITIONS**

DEFINITIONS	W.100X.COW.TM WWW.100X.COW.TW
Data sheet status	NN 100 Y COM. THE WAY 100 Y COM. THE
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting Contract	

#### Limiting values

Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

#### **Application information**

Where application information is given, it is advisory and does not form part of the specification.

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