FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

CD4030C
Quad EXCLUSIVE-OR Gate

General Description

The CD4030C EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range: 3.0V to 15V
- Low power: 100 nW (typ.)
- Medium speed operation:
  $t_{PHL} = t_{PLH}$ = 40 ns (typ.) at C_L = 15 pF, 10V supply
- High noise immunity 0.45 V_{CC} (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

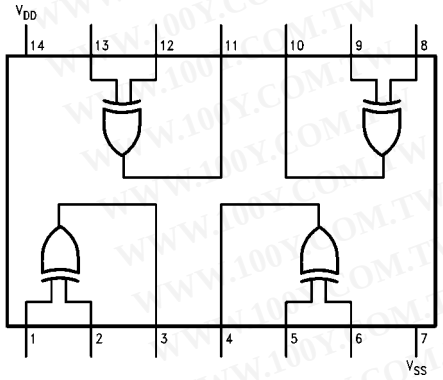
Ordering Code:

Order Number	Package Number	Package Description
CD4030CSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4030CN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOP

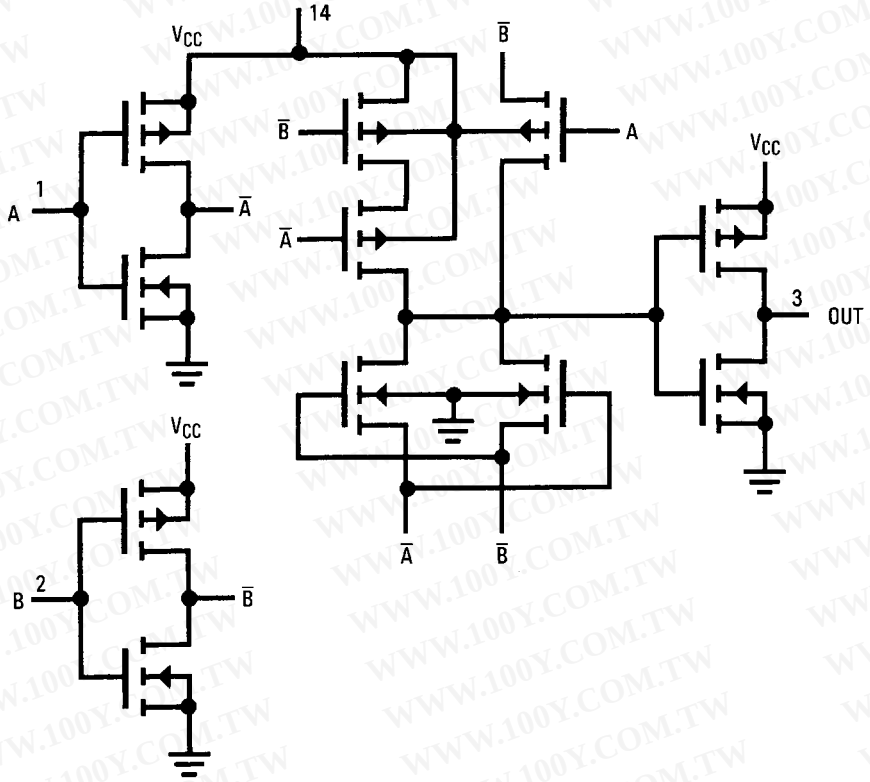


Truth Table

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH Level
0 = LOW Level

Logic Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin (Note 2)	V_{SS} −0.3V to V_{SS} +15.5V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{DD} Range	V_{SS} +3.0V to V_{SS} +15V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

Note 2: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Limits									Units
			−40°C			+25°C			+85°C			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device	V_{DD} = 5.0V			5.0		0.05	5.0			70	µA
	Current	V_{DD} = 10V			10		0.1	10			140	µA
P_D	Quiescent Device	V_{DD} = 5.0V			25		0.25	25			350	µW
	Dissipation Package	V_{DD} = 10V			100		1.0	100			1,400	µW
V_{OL}	Output Voltage	V_{DD} = 5.0V			0.05		0	0.05			0.05	V
	LOW Level	V_{DD} = 10V			0.05		0	0.05			0.05	V
V_{OH}	Output Voltage	V_{DD} = 5.0V	4.95			4.95	5.0		4.95			V
	HIGH Level	V_{DD} = 10V	9.95			9.95	10		9.95			V
V_{NL}	Noise Immunity	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	(All Inputs)	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
V_{NH}	Noise Immunity	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	(All Inputs)	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
I_DN	Output Drive Current	V_{DD} = 5.0V	0.35			0.3	1.2		0.25			mA
	N-Channel (Note 3)	V_{DD} = 10V	0.7			0.6	2.4		0.5			mA
I_DP	Output Drive Current	V_{DD} = 5.0V	−0.21			−0.15	−0.6		−0.12			mA
	P-Channel (Note 3)	V_{DD} = 10 V	−0.45			−0.32	−1.3		−0.25			mA
I_I	Input Current	V_I = 0V or V_I = V_{DD}					10					pA

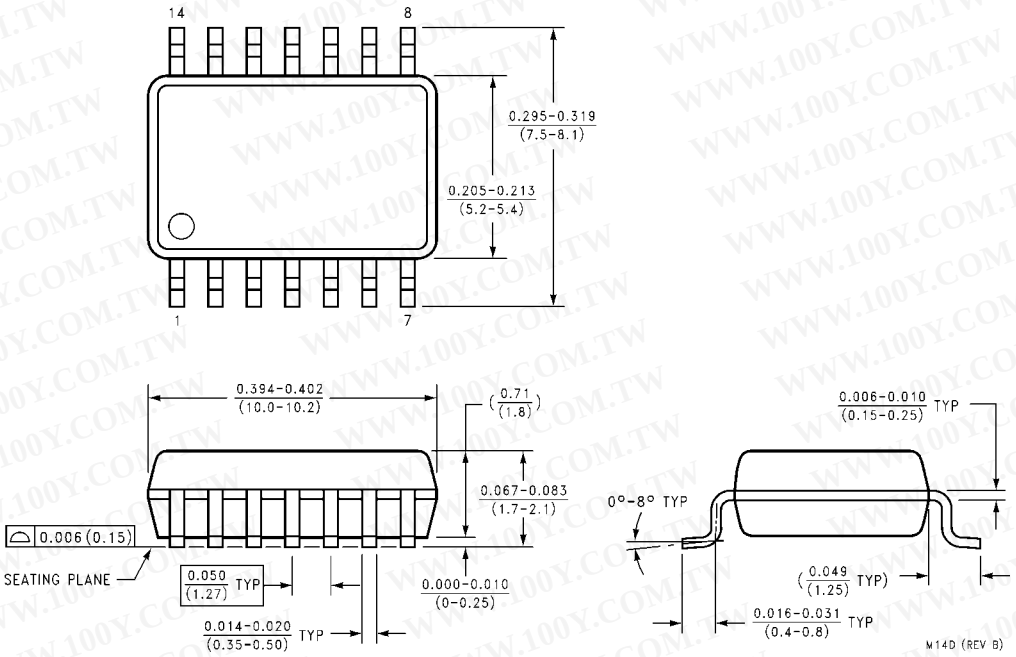
Note 3: I_DN and I_DP are tested one output at a time.

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
t_{PHL}	Propagation Delay Time	V_{DD} = 5.0V		100	300	ns
		V_{DD} = 10V		40	150	ns
t_{PLH}	Propagation Delay Time	V_{DD} = 5.0V		100	300	ns
		V_{DD} = 10V		40	150	ns
t_{THL}	Transition Time	V_{DD} = 5.0V		70	300	ns
	HIGH-to-LOW Level	V_{DD} = 10V		25	150	ns
t_{TLH}	Transition Time	V_{DD} = 5.0V		80	300	ns
	LOW-to-HIGH Level	V_{DD} = 10V		30	150	ns
C_I	Input Capacitance	V_I = 0V or V_I = V_{DD}		5.0		pF

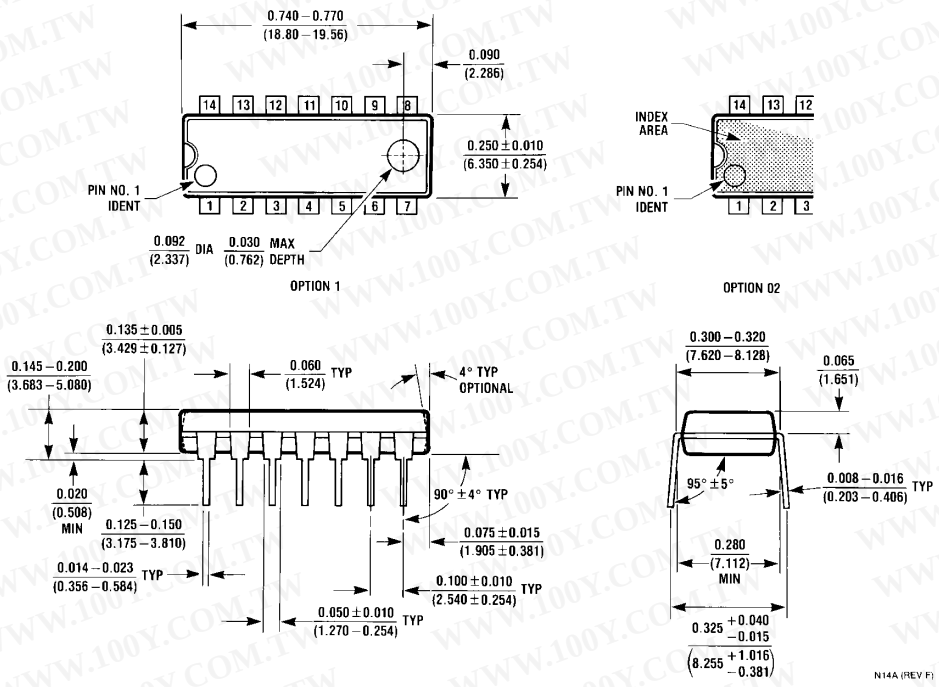
Note 4: AC Parameters are guaranteed by DC correlated testing.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.