

# CD54HC74, CD74HC74, CD74HCT74

## Dual D Flip-Flop with Set and Reset Positive-Edge Trigger

### Features

- Hysteresis on Clock Inputs for Improved Noise Immunity and Increased Input Rise and Fall Times
- Asynchronous Set and Reset
- Complementary Outputs
- Buffered Inputs
- Typical  $f_{MAX} = 50\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{V (Max)}$ ,  $V_{IH} = 2\text{V (Min)}$
  - CMOS Input Compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD54HC74, CD74HC74 and CD74HCT74 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

This flip-flop has independent DATA,  $\overline{\text{SET}}$ ,  $\overline{\text{RESET}}$  and CLOCK inputs and Q and  $\overline{\text{Q}}$  outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. SET and RESET are independent of the clock and are accomplished by a low level at the appropriate input.

The 74HCT logic family is functionally as well as pin compatible with the standard 74LS logic family.

### Ordering Information

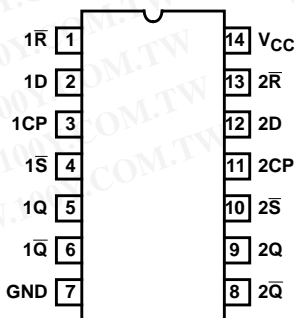
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD54HC74F	-55 to 125	14 Ld CERDIP	F14.3
CD74HC74E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT74E	-55 to 125	14 Ld PDIP	E14.3
CD74HC74M	-55 to 125	14 Ld SOIC	M14.15
CD74HCT74M	-55 to 125	14 Ld SOIC	M14.15

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout

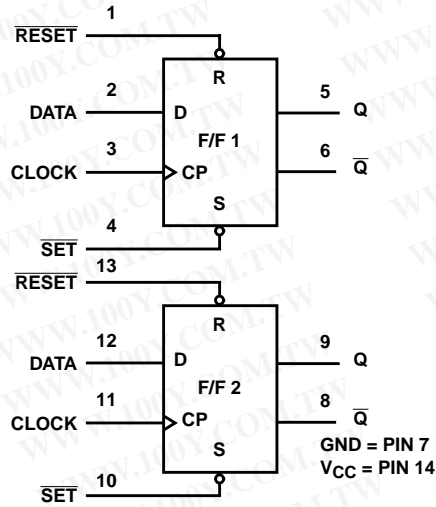
CD54HC74, CD74HC74, CD74HCT74  
(PDIP, SOIC, CERDIP)  
TOP VIEW



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## Functional Diagram



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TRUTH TABLE

INPUTS				OUTPUTS	
SET	RESET	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 3)	H (Note 3)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	Q̄0

NOTE:

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care

↑ = Low-to-High Transition

Q0 = the level of Q before the indicated input conditions were established.

- This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

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## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ ( $^{\circ}C/W$ )	$\theta_{JC}$ ( $^{\circ}C/W$ )
PDIP Package .....	90	-
SOIC Package .....	120	-
CERDIP Package .....	130	55
Maximum Junction Temperature (Hermetic Package or Die) .....	175 $^{\circ}C$	
Maximum Junction Temperature (Plastic Package) .....	150 $^{\circ}C$	
Maximum Storage Temperature Range .....	-65 $^{\circ}C$ to 150 $^{\circ}C$	
Maximum Lead Temperature (Soldering 10s) .....	300 $^{\circ}C$ (SOIC - Lead Tips Only)	

## Operating Conditions

Temperature Range ( $T_A$ ) .....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

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*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

4.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>													
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
				4.5	4.4	-	-	4.4	-	4.4	-	V	
				6	5.9	-	-	5.9	-	5.9	-	V	
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
				-4	4.5	3.98	-	-	3.84	-	3.7	-	V
				-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
				4.5	-	-	0.1	-	0.1	-	0.1	V	
				6	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
				4	4.5	-	-	0.26	-	0.33	-	0.4	V
				5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$	

## CD54HC74, CD74HC74, CD74HCT74

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	4	-	40	-	80	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-0.02	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-4	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			0.02	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	4	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	4	-	40	-	80	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 5)	V <sub>CC</sub> - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

5. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS
D	0.5
$\bar{R}$	0.5
CP	0.7
$\bar{S}$	0.75

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

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### Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Data to CP Setup Time (Figure 5)	t <sub>SU</sub>	-	2	60	-	-	75	-	90	-	ns
			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns

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Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Hold Time (Figure 5)	t <sub>H</sub>	-	2	3	-	-	3	-	3	-	ns
			4.5	3	-	-	3	-	3	-	ns
			6	3	-	-	3	-	3	-	ns
Removal Time $\bar{R}$ , $\bar{S}$ , to CP (Figure 5)	t <sub>REM</sub>	-	2	30	-	-	40	-	45	-	ns
			4.5	6	-	-	8	-	9	-	ns
			6	5	-	-	7	-	8	-	ns
Pulse Width $\bar{R}$ , $\bar{S}$ (Figure 1)	t <sub>W</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Pulse Width CP (Figure 1)	t <sub>W</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
CP Frequency	f <sub>MAX</sub>	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	25	-	20	-	MHz
			6	35	-	-	29	-	23	-	MHz

HCT TYPES

Data to CP Setup Time (Figure 6)	t <sub>SU</sub>	-	4.5	12	-	-	15	-	18	-	ns
Hold Time (Figure 6)	t <sub>H</sub>	-	4.5	3	-	-	3	-	3	-	ns
Removal Time $\bar{R}$ , $\bar{S}$ , to CP (Figure 6)	t <sub>REM</sub>	-	4.5	6	-	-	8	-	9	-	ns
Pulse Width $\bar{R}$ , $\bar{S}$ (Figure 2)	t <sub>W</sub>	-	4.5	16	-	-	20	-	24	-	ns
Pulse Width CP (Figure 2)	t <sub>W</sub>	-	4.5	18	-	-	23	-	27	-	ns
CP Frequency	f <sub>MAX</sub>	-	4.5	25	-	-	20	-	16	-	MHz

Switching Specifications Input t<sub>p</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay, CP to Q, $\bar{Q}$ (Figure 3)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	175	-	220	-	265	ns
		C <sub>L</sub> = 50pF	4.5	-	-	35	-	44	-	53	ns
		C <sub>L</sub> = 15pF	5	-	14	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	30	-	37	-	45	ns
Propagation Delay, $\bar{R}$ , $\bar{S}$ to Q, $\bar{Q}$ (Figure 3)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	200	-	250	-	300	ns
		C <sub>L</sub> = 50pF	4.5	-	-	40	-	50	-	60	ns
		C <sub>L</sub> = 15pF	5	-	17	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	34	-	43	-	51	ns
Transition Time (Figure 3)	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
		C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns
		C <sub>L</sub> = 50pF	6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>I</sub>	-	-	-	-	10	-	10	-	10	pF

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### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

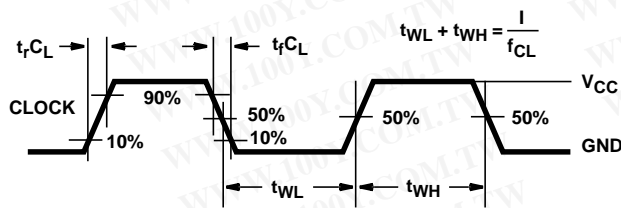
PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CP Frequency	$f_{MAX}$	$C_L = 15\text{pF}$	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 6, 7)	$C_{PD}$	-	5	-	25	-	-	-	-	-	pF
<b>HCT TYPES</b>											
Propagation Delay, CP to Q, $\bar{Q}$ (Figure 4)	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
Propagation Delay, R, S to Q, Q (Figure 4)	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	40	-	50	-	60	ns
Transition Time (Figure 4)	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	$C_I$	-	-	-	-	10	-	10	-	10	pF
CP Frequency	$f_{MAX}$	$C_L = 15\text{pF}$	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 6, 7)	$C_{PD}$	-	5	-	30	-	-	-	-	-	pF

**NOTES:**

6.  $C_{PD}$  is used to determine the dynamic power consumption, per flip-flop.

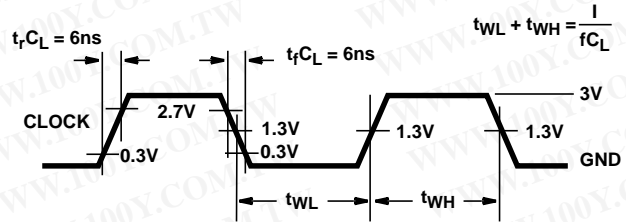
7.  $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

### Test Circuits and Waveforms



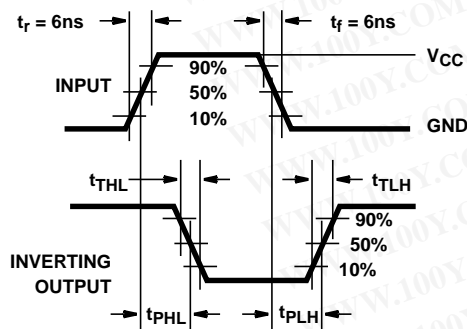
NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

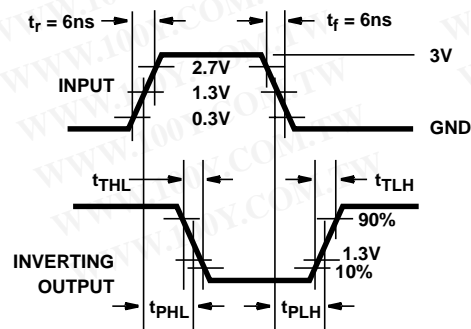


NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



**FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

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Test Circuits and Waveforms (Continued)

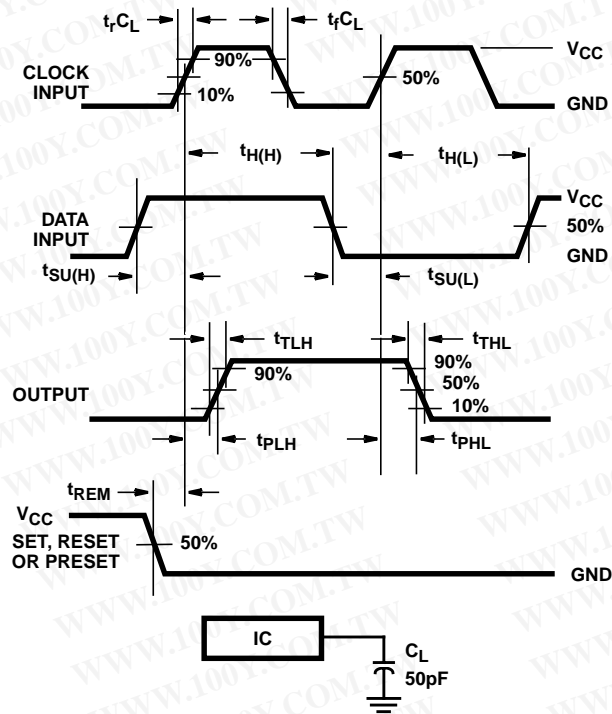


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

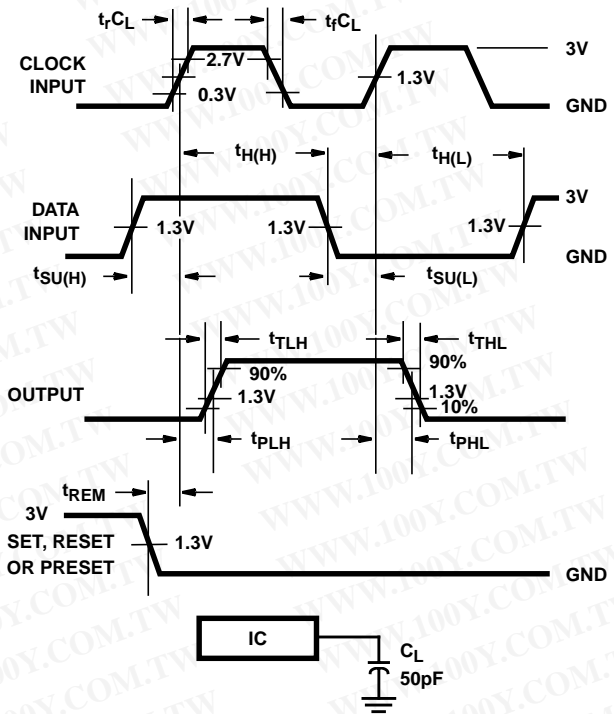


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

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