

Dual Monolithic CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- TWO DACs IN A 0.3" WIDE PACKAGE
- SINGLE +5V SUPPLY
- HIGH SPEED DIGITAL INTERFACE:
Serial—DAC7800
8 + 4-Bit Parallel—DAC7801
12-Bit Parallel—DAC7802
- MONOTONIC OVER TEMPERATURE
- LOW CROSSTALK: -94dB min
- FULLY SPECIFIED OVER -40°C TO +85°C

DESCRIPTION

The DAC7800, DAC7801 and DAC7802 are members of a new family of monolithic dual 12-bit CMOS multiplying Digital-to-Analog Converters (DACs). The digital interface speed and the AC multiplying performance are achieved by using an advanced CMOS process optimized for data conversion circuits. High stability on-chip resistors provide true 12-bit integral and differential linearity over the wide industrial temperature range of -40°C to +85°C.

DAC7800 features a serial interface capable of clocking-in data at a rate of at least 10MHz. Serial data is clocked (edge triggered) MSB first into a 24-bit shift register and then latched into each DAC separately or simultaneously as required by the application. An asynchronous CLEAR control is provided for power-on reset or system calibration functions. It is packaged in a 16-pin 0.3" wide plastic DIP.

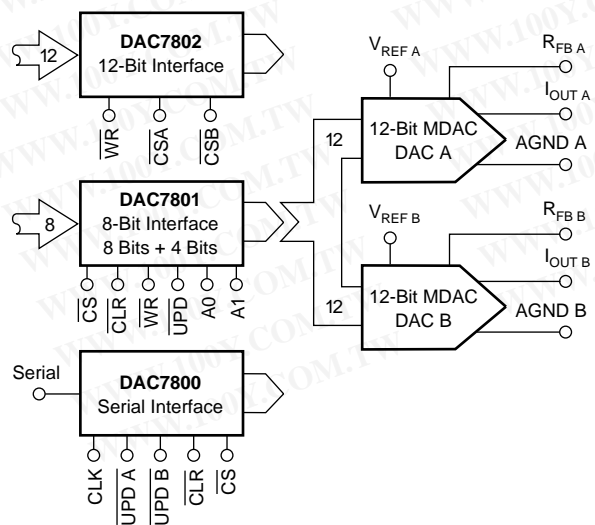
DAC7801 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. DAC7801 features an asynchronous CLEAR control. DAC7801 is packaged in a 24-pin 0.3" wide plastic DIP.

APPLICATIONS

- PROCESS CONTROL OUTPUTS
- ATE PIN ELECTRONICS LEVEL SETTING
- PROGRAMMABLE FILTERS
- PROGRAMMABLE GAIN CIRCUITS
- AUTO-CALIBRATION CIRCUITS

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

DAC7802 has a single-buffered 12-bit data word interface. Parallel data is loaded (edge triggered) into the single DAC register for each DAC. DAC7802 is packaged in a 24-pin 0.3" wide plastic DIP.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

| | |
|-----------------------------------|---------------------------------------------|
| V_{DD} to AGND | 0V, +7V |
| V_{DD} to DGND | 0V, +7V |
| AGND to DGND | -0.3, V_{DD} |
| Digital Input to DGND | -0.3, $V_{DD} + 0.3$ |
| $V_{REF A}$, $V_{REF B}$ to AGND | $\pm 16\text{V}$ |
| $V_{REF A}$, $V_{REF B}$ to DGND | $\pm 16\text{V}$ |
| $I_{OUT A}$, $I_{OUT B}$ to AGND | -0.3, V_{DD} |
| Storage Temperature Range | -55°C to $+125^\circ\text{C}$ |
| Operating Temperature Range | -40°C to $+85^\circ\text{C}$ |
| Lead Temperature (soldering, 10s) | $+300^\circ\text{C}$ |
| Junction Temperature | $+175^\circ\text{C}$ |



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

| PRODUCT | RELATIVE ACCURACY | GAIN ERROR | PACKAGE-LEAD | PACKAGE DESIGNATOR ⁽¹⁾ | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|-----------|----------------------|-------------------|--------------|-----------------------------------|--------------------------------------------|-----------------|-----------------|---------------------------|
| DAC7800KP | $\pm 1\text{LSB}$ | $\pm 3\text{LSB}$ | DIP-16 | N | -40°C to $+85^\circ\text{C}$ | DAC7800KP | DAC7800KP | Rails, 25 |
| DAC7800LP | $\pm 1/2\text{ LSB}$ | $\pm 1\text{LSB}$ | DIP-16 | N | | DAC7800LP | DAC7800LP | Rails, 25 |
| DAC7800KU | — | — | SO-16 | DW | -40°C to $+85^\circ\text{C}$ | DAC7800KU | DAC7800KU/1K | Tape and Reel, 1000 |
| DAC7800LU | — | — | SO-16 | DW | | DAC7800LU | DAC7800LU/1K | Tape and Reel, 1000 |
| DAC7801KP | $\pm 1\text{LSB}$ | $\pm 3\text{LSB}$ | DIP-24 | NT | -40°C to $+85^\circ\text{C}$ | DAC7801KP | DAC7801KP | Rails, 15 |
| DAC7801LP | $\pm 1/2\text{ LSB}$ | $\pm 1\text{LSB}$ | DIP-24 | NT | | DAC7801LP | DAC7801LP | Rails, 15 |
| DAC7801KU | — | — | SO-24 | DW | -40°C to $+85^\circ\text{C}$ | DAC7801KU | DAC7801KU/1K | Tape and Reel, 1000 |
| DAC7801LU | — | — | SO-24 | DW | | DAC7801LU | DAC7801LU/1K | Tape and Reel, 1000 |
| DAC7802KP | $\pm 1\text{LSB}$ | $\pm 3\text{LSB}$ | DIP-24 | NTG | -40°C to $+85^\circ\text{C}$ | DAC7802KP | DAC7802KP | Rails, 15 |
| DAC7802LP | $\pm 1/2\text{ LSB}$ | $\pm 1\text{LSB}$ | DIP-24 | NTG | | DAC7802LP | DAC7802LP | Rails, 15 |
| DAC7802KU | — | — | SO-24 | DW | -40°C to $+85^\circ\text{C}$ | DAC7802KU | DAC7802KU/1K | Tape and Reel, 1000 |
| DAC7802LU | — | — | SO-24 | DW | | DAC7802LU | DAC7802LU/1K | Tape and Reel, 1000 |

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

勝特力材料 86-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

ELECTRICAL CHARACTERISTICS

At $V_{DD} = +5\text{VDC}$, $V_{REF A} = V_{REF B} = +10\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC7800, 7801, 7802K | | | DAC7800, 7801, 7802L | | | UNITS |
|---------------------------------------------|---------------------------------------------------------------------------------|----------------------|-------|----------|----------------------|-----|-----------|-----------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| ACCURACY | | | | | | | | |
| Resolution | Measured Using $R_{FB A}$ and $R_{FB B}$. All Registers Loaded with All 1s. | 12 | | | * | | | Bits |
| Relative Accuracy | | | | ± 1 | | | $\pm 1/2$ | LSB |
| Differential Nonlinearity | | | | ± 1 | | | * | LSB |
| Gain Error | | | | ± 3 | | | ± 1 | LSB |
| Gain Temperature Coefficient ⁽¹⁾ | $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | 2 | 5 | | * | * | ppm/ $^\circ\text{C}$ |
| Output Leakage Current | | | 0.005 | 10 | | * | * | nA |
| | | | 3 | 150 | | * | * | nA |
| REFERENCE INPUT | | | | | | | | |
| Input Resistance | | 6 | 10 | 14 | * | * | * | k Ω |
| Input Resistance Match | | | 0.5 | 3 | | * | 2 | % |
| DIGITAL INPUTS | | | | | | | | |
| V_{IH} (Input HIGH Voltage) | $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | 2 | | | * | | | V |
| V_{IL} (Input LOW Voltage) | | | | 0.8 | | | * | V |
| I_{IN} (Input Current) | | | | ± 1 | | | * | μA |
| | | | | ± 10 | | | * | μA |
| C_{IN} (Input Capacitance) | | | 0.8 | 10 | | * | * | pF |
| POWER SUPPLY | | | | | | | | |
| V_{DD} | V_{DD} from 4.5V to 5.5V | 4.5 | | 5.5 | * | | * | V |
| I_{DD} | | | 0.2 | 2 | | * | * | mA |
| Power-Supply Rejection | | | | 0.002 | | | * | %/% |

* Same specification as for DAC7800, 7801, 7802K.

AC PERFORMANCE

OUTPUT OP AMP IS OPA602.

At $V_{DD} = +5VDC$, $V_{REF A} = V_{REF B} = +10V$, $T_A = +25^\circ C$, unless otherwise noted. These specifications are fully characterized but not subject to test.

| PARAMETER | CONDITIONS | DAC7800, 7801, 7802K | | | DAC7800, 7801, 7802L | | | UNITS |
|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|----------|-----------|----------------------|-----|-----|----------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| OUTPUT CURRENT SETTLING TIME | To 0.01% of Full-Scale $R_L = 100\Omega$, $C_L = 13pF$ | | 0.4 | 0.8 | | * | * | μs |
| DIGITAL-TO-ANALOG GLITCH IMPULSE | $V_{REF A} = V_{REF B} = 0V$ $R_L = 100\Omega$, $C_L = 13pF$ | | 0.9 | | | * | | nV-s |
| AC FEEDTHROUGH | $f_{VREF} = 10kHz$ | | -75 | -72 | | * | * | dB |
| OUTPUT CAPACITANCE | DAC Loaded with All 0s DAC Loaded with All 1s | | 30 70 | 50 100 | | * | * | pF pF |
| CHANNEL-TO-CHANNEL ISOLATION | $f_{VREF A} = 10kHz$ $V_{REF B} = 0V$, Both DACs Loaded with 1s $f_{VREF B} = 10kHz$ $V_{REF A} = 0V$, Both DACs Loaded with 1s | $V_{REF A}$ to $I_{OUT B}$ | -90 | -94 | * | * | | dB |
| | | $V_{REF B}$ to $I_{OUT A}$ | -90 | -101 | * | * | | dB |
| DIGITAL CROSSTALK | Full-Scale Transition $R_L = 100\Omega$, $C_L = 13pF$ | | 0.9 | | | * | | nV-s |

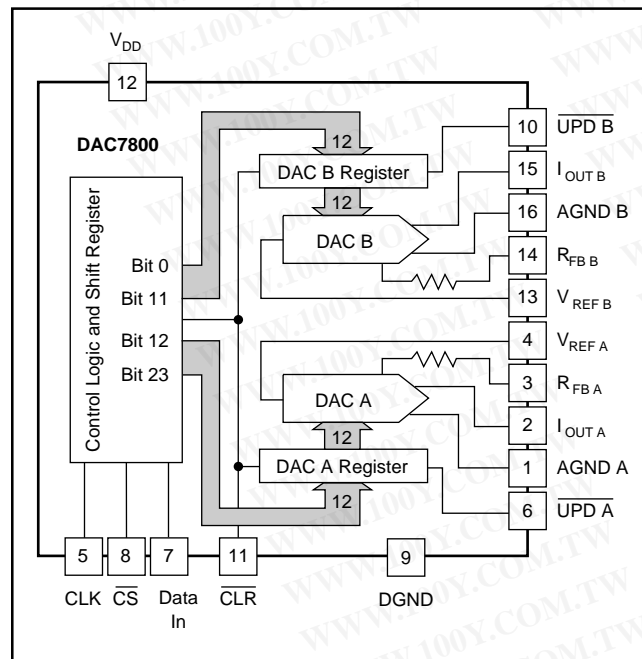
* Same specification as for DAC7800, 7801, and 7802K.

NOTE: (1) Ensured but not tested.

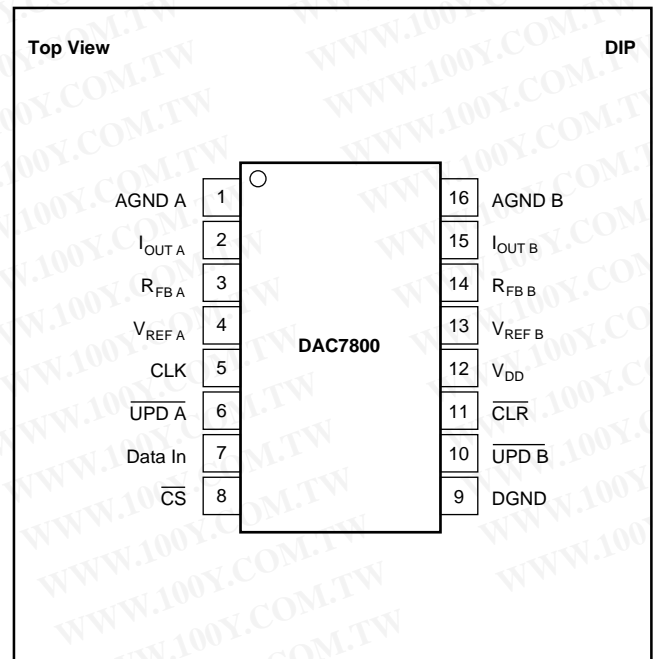
勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

DAC7800

BLOCK DIAGRAM



PIN CONFIGURATION



LOGIC TRUTH TABLE

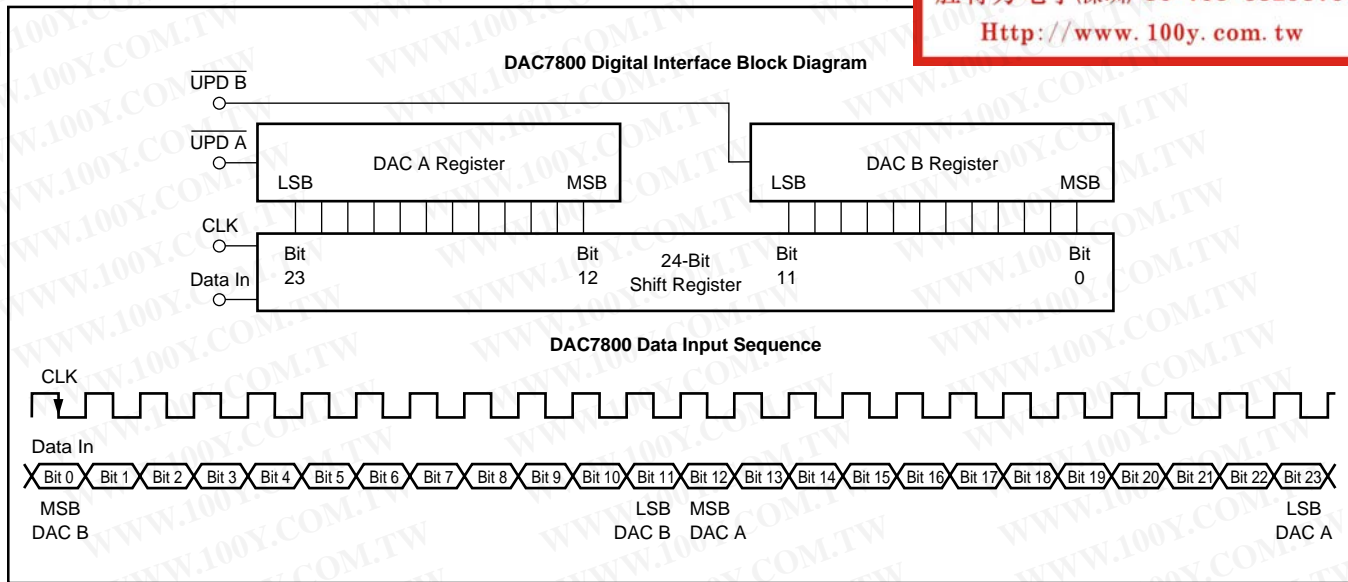
| CLK | UPD A | UPD B | CS | CLR | FUNCTION |
|----------------|-------|-------|----|-----|----------------------------------------------------------------------------------------------------------------------------------|
| X | X | X | X | 0 | All register contents set to 0's (asynchronous). |
| X | X | X | 1 | X | No data transfer. |
| $\overline{1}$ | X | X | 0 | 1 | Input data is clocked into input register (location Bit 23) and previous data shifts. |
| X | 0 | 1 | 0 | 1 | Input register bits 23 (LSB) - 12 (MSB) are loaded into DAC A. |
| X | 1 | 0 | 0 | 1 | Input register bits 11 (LSB) - 0 (MSB) are loaded into DAC B. |
| X | 0 | 0 | 0 | 1 | Input register bits 23 (LSB) - 12 (MSB) are loaded into DAC A, and input register bits 11 (LSB) - 0 (MSB) are loaded into DAC B. |

X = Don't care. $\overline{1}$ means falling edge triggered.

DAC7800 (Cont.)

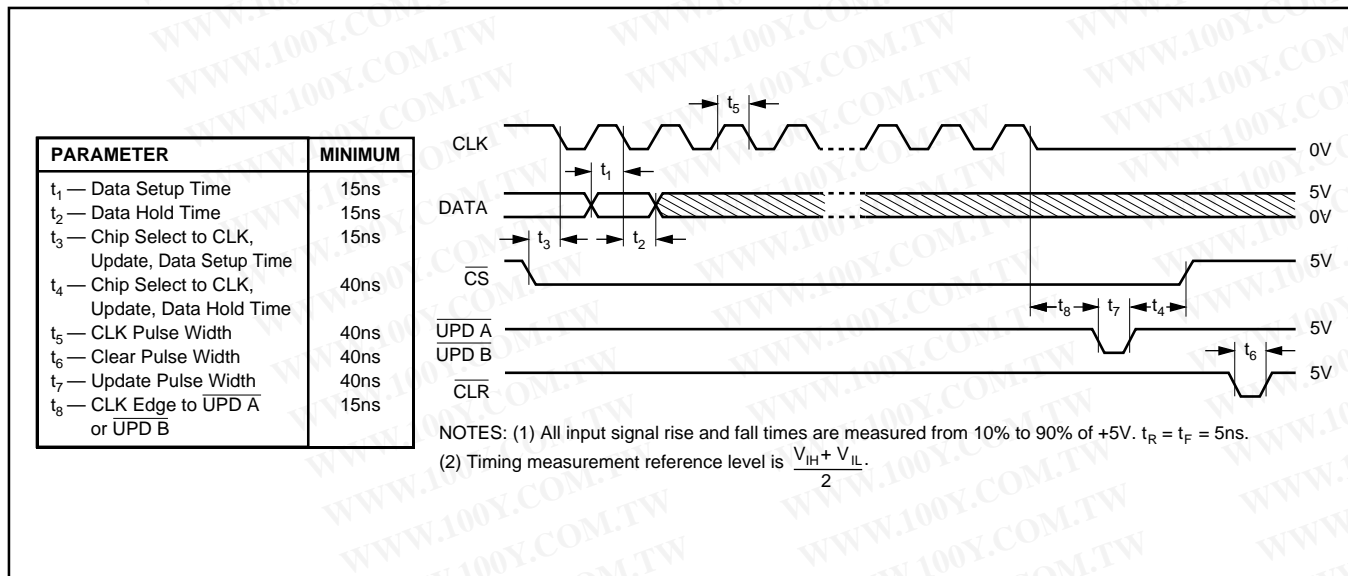
DATA INPUT FORMAT

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



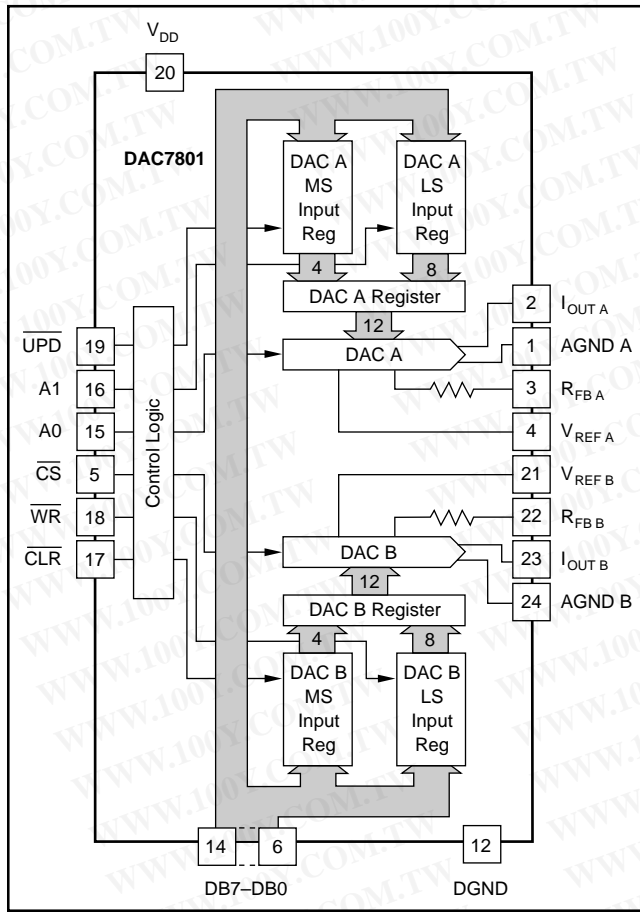
TIMING CHARACTERISTICS

$V_{DD} = +5V$, $V_{REF A} = V_{REF B} = +10V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

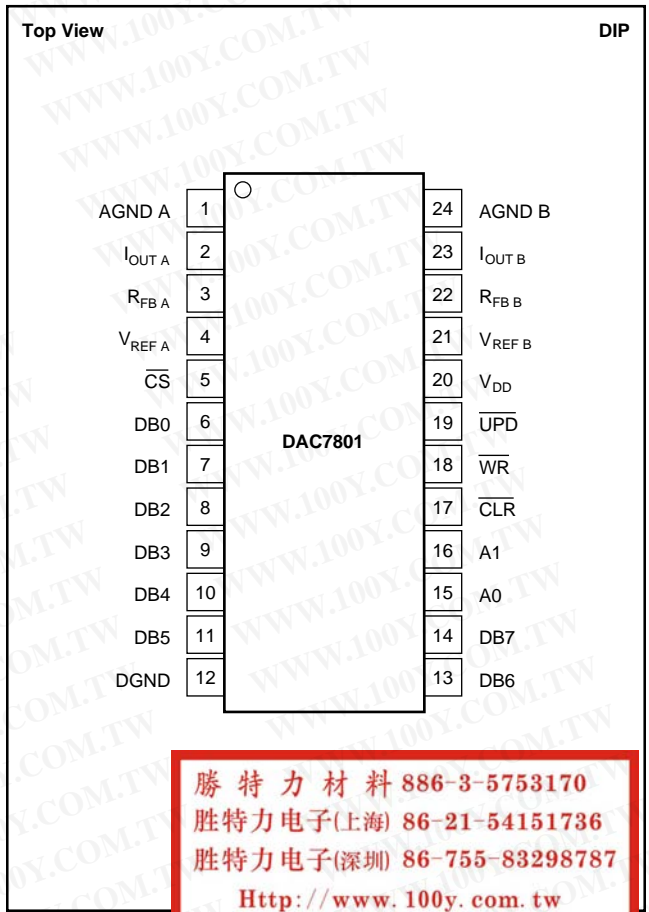


DAC7801

BLOCK DIAGRAM



PIN CONFIGURATION



勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

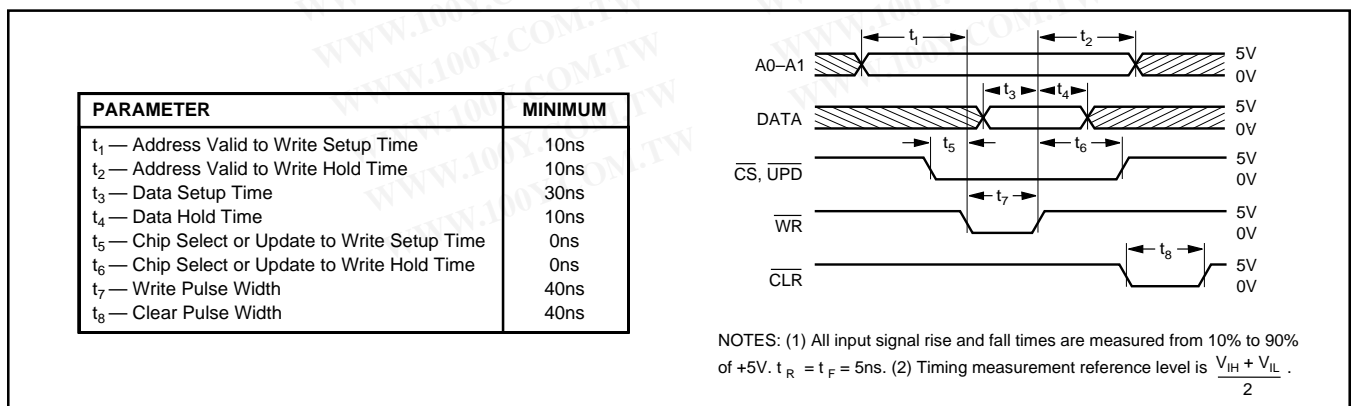
LOGIC TRUTH TABLE

| \overline{CLR} | \overline{UPD} | \overline{CS} | \overline{WR} | A1 | A0 | FUNCTION |
|------------------|------------------|-----------------|-----------------|----|----|--------------------------------------------------------------------|
| 1 | 1 | 1 | X | X | X | No Data Transfer |
| 1 | 1 | X | 1 | X | X | No Data Transfer |
| 0 | X | X | X | X | X | All Registers Cleared |
| 1 | 1 | 0 | 0 | 0 | 0 | DAC A LS Input Register Loaded with DB7 - DB0 (LSB) |
| 1 | 1 | 0 | 0 | 0 | 1 | DAC A MS Input Register Loaded with DB3 (MSB) - DB0 |
| 1 | 1 | 0 | 0 | 1 | 0 | DAC B LS Input Register Loaded with DB7 - DB0 (LSB) |
| 1 | 1 | 0 | 0 | 1 | 1 | DAC B MS Input Register Loaded with DB3 (MSB) - DB0 |
| 1 | 0 | 1 | 0 | X | X | DAC A, DAC B Registers Updated Simultaneously from Input Registers |
| 1 | 0 | 0 | 0 | X | X | DAC A, DAC B Registers are Transparent |

X = Don't care.

TIMING CHARACTERISTICS

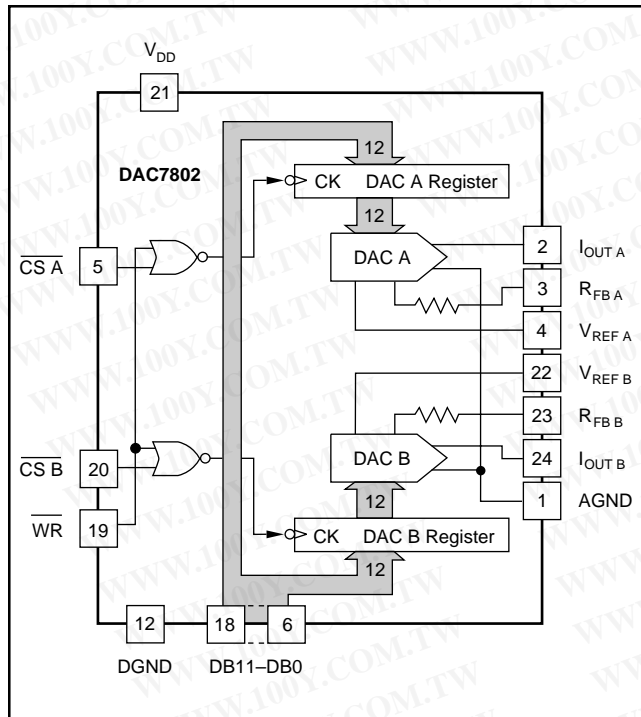
V_{DD} = +5V, V_{REF A} = V_{REF B} = +10V, T_A = -40°C to +85°C.



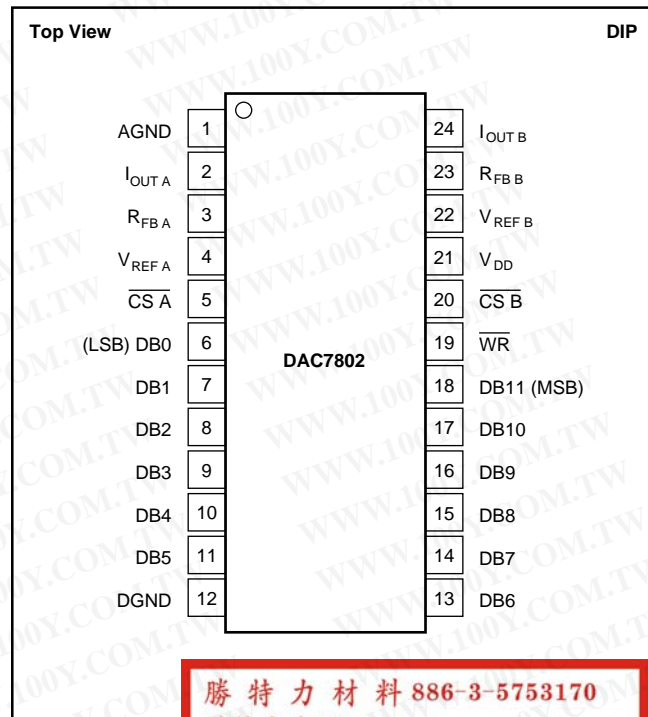
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. t_R = t_F = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

DAC7802

BLOCK DIAGRAM



PIN CONFIGURATION

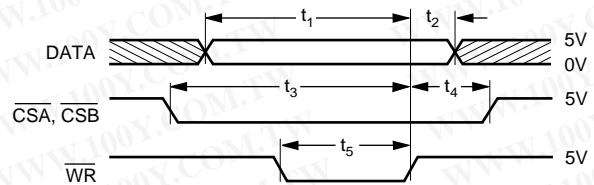


勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

TIMING CHARACTERISTICS

At V_{DD} = +5V, and T_A = -40°C to +85°C.

| PARAMETER | MINIMUM |
|--------------------------------------------------|---------|
| t ₁ - Data Setup Time | 20ns |
| t ₂ - Data Hold Time | 15ns |
| t ₃ - Chip Select to Write Setup Time | 30ns |
| t ₄ - Chip Select to Write Hold Time | 0ns |
| t ₅ - Write Pulse Width | 30ns |



NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. t_R = t_F = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

LOGIC TRUTH TABLE

| CSA | CSB | WR | FUNCTION |
|-----|-----|----|--------------------------------------------------------------|
| X | X | 1 | No Data Transfer |
| 1 | 1 | X | No Data Transfer |
| ┌ | ┌ | 0 | A Rising Edge on CSA or CSB Loads Data to the Respective DAC |
| 0 | 1 | ┌ | DAC A Register Loaded from Data Bus |
| 1 | 0 | ┌ | DAC B Register Loaded from Data Bus |
| 0 | 0 | ┌ | DAC A and DAC B Registers Loaded from Data Bus |

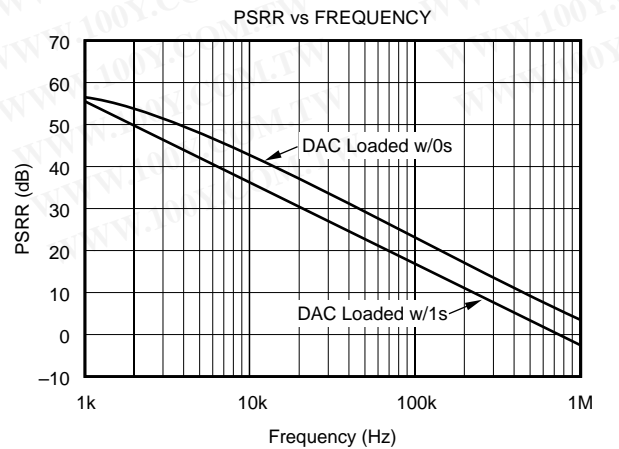
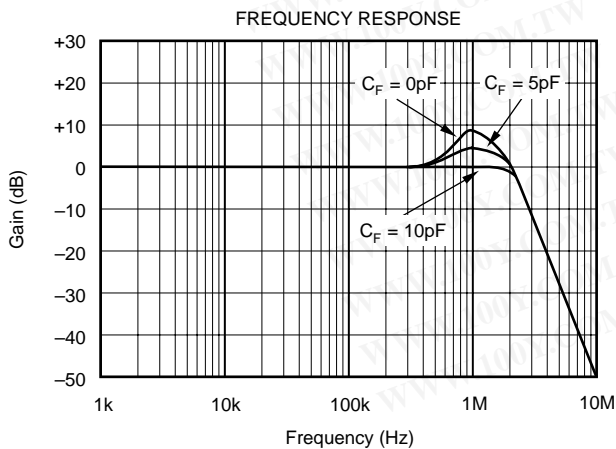
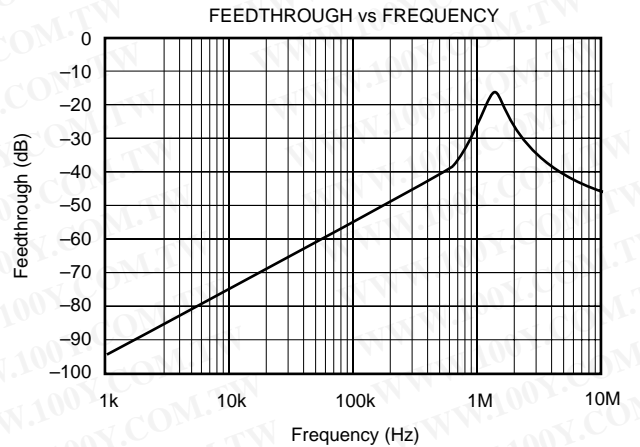
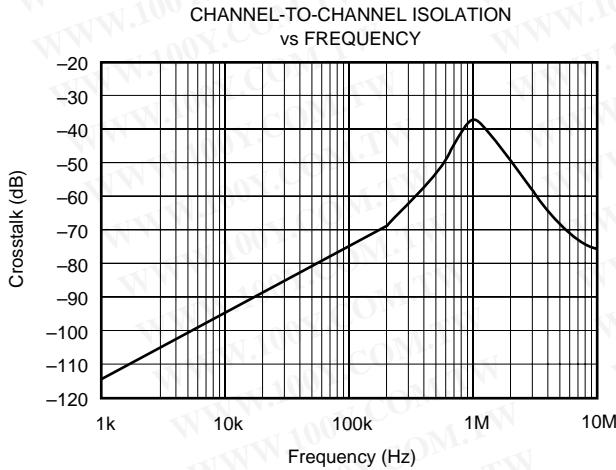
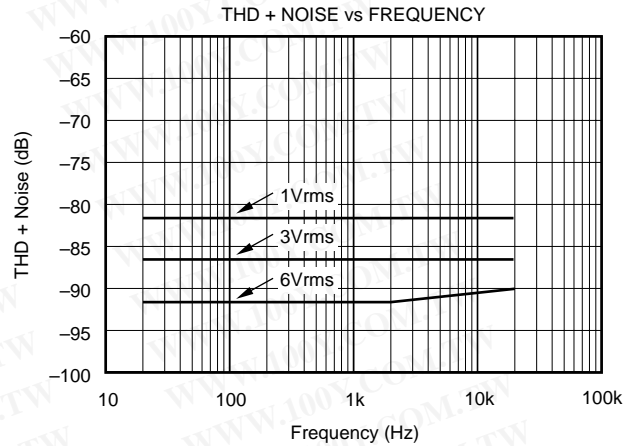
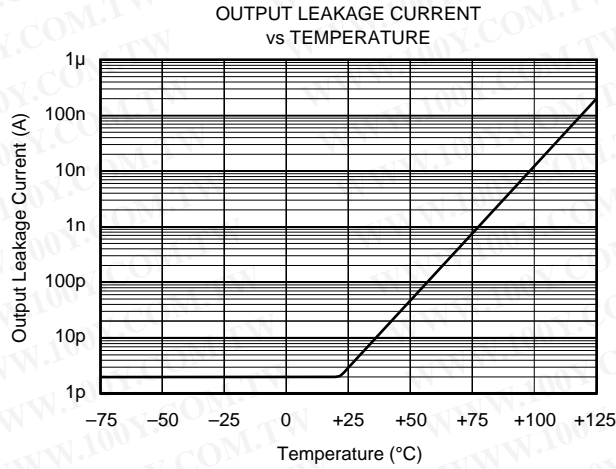
X = Don't care. ┌ means rising edge triggered.

TYPICAL CHARACTERISTICS

OUTPUT OP AMP IS OPA602.

$T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full-scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum ensures monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC780x is $-(4095/4096)V_{REF}$. Gain error may be adjusted to zero using external trims, see Figures 5 and 7.

OUTPUT LEAKAGE CURRENT

The current which appears at $I_{OUT A}$ and $I_{OUT B}$ with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from $I_{OUT A}$ or $I_{OUT B}$ to AGND.

CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DAC A to DAC B or DAC B to DAC A.

MULTIPLYING FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTling TIME

The time required for the output current to settle to within $\pm 0.01\%$ of final value for a full-scale step.

DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to DAC glitch is charge injected by digital logic switching transients.

DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full-scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC780x. The current from the $V_{REF A}$ pin is switched between $I_{OUT A}$ and AGND by 12 single-pole double-throw CMOS switches. This maintains a constant current in each leg of the ladder regardless of the input code. The input resistance at V_{REF} is therefore

constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to $\pm 20V$.

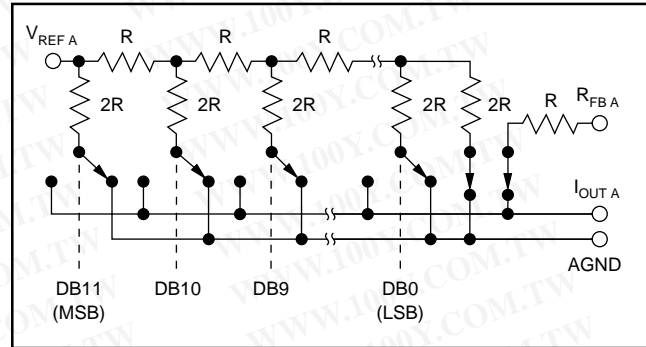


FIGURE 1. Simplified Circuit Diagram for DAC A.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, $R_{FB A}$, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for DAC A. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 30pF to 70pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every $10^{\circ}C$. R_O is the equivalent output resistance of the DAC and it varies with input code.

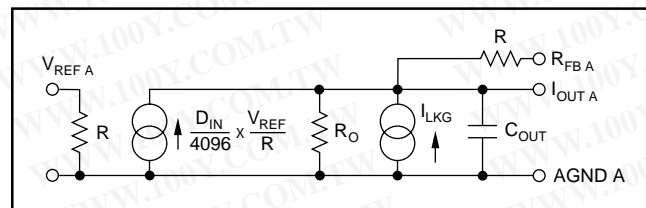


FIGURE 2. Equivalent Circuit for DAC A.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC780x incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500 Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER-SUPPLY CONNECTIONS

The DAC780x are designed to operate on $V_{DD} = +5V \pm 10\%$. For optimum performance and noise rejection, power-supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1 μF tantalum recommended) should be located close to the DAC. AGND and

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

DGND should be connected together at one point only, preferably at the power-supply ground point. Separate returns minimize current flow in low-level signal paths if properly connected. Output op amp analog common (+ input) should be connected as near to the AGND pins of the DAC780x as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Solder the DAC780x directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC780x should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the “noise gain” of the circuit. This “noise gain” is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the DAC I_{OUT} terminal and R_F is the feedback network impedance. The nonlinearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where $R_O = \infty$), the R_O will vary from $R/3R$ providing a “noise gain” variation between $4/3$ and 2 . In addition, the variation of R_O is nonlinear with code, and the largest steps in R_O occur at major code transitions where the worst differential nonlinearity is also likely to be experienced. The nonlinearity seen at the amplifier output is $2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3$. Thus, to maintain good nonlinearity the op amp offset should be much less than $1/2$ LSB.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC780x in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. If an application requires the DAC to have zero gain error, the circuit shown in Figure 4 may be used. Resistors R_2 and R_4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R_1 and R_3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R_2 and R_4 .

BIPOLAR CONFIGURATION

See Figure 5 for the DAC780x in a typical bipolar (four-quadrant) multiplying configuration. See Table III for the listing of the analog output values versus digital input code.

| DATA INPUT | | ANALOG OUTPUT | |
|----------------|-------|----------------------------------------|--|
| MSB ↓ | ↓ LSB | $-V_{REF}$ (4095/4096) | |
| 1111 1111 1111 | | $-V_{REF}$ (2048/4096) = $-1/2V_{REF}$ | |
| 1000 0000 0000 | | $-V_{REF}$ (1/4096) | |
| 0000 0000 0001 | | 0 Volts | |
| 0000 0000 0000 | | | |

TABLE II. Unipolar Output Code.

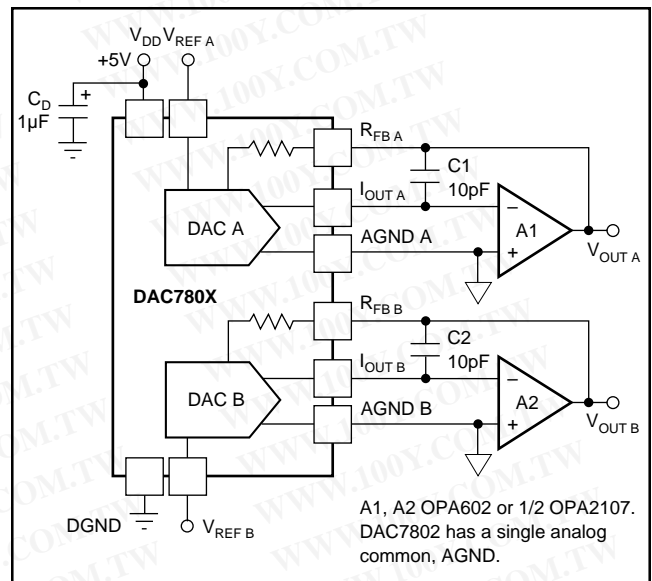


FIGURE 3. Unipolar Configuration.

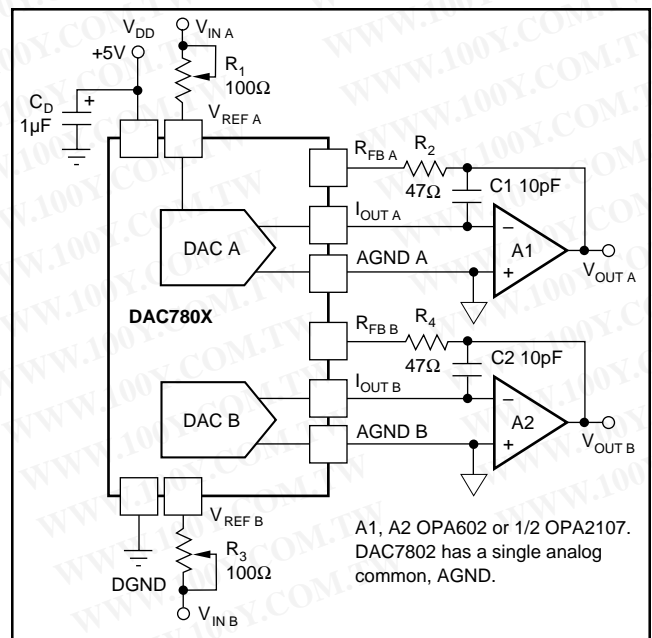


FIGURE 4. Unipolar Configuration with Gain Trim.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R_5 – R_7 and R_8 – R_{10} should be ratio-matched to 0.01% to ensure the specified gain error performance.

If an application requires the DAC to have zero gain error, the circuit may be used, see Figure 6. Resistors R_2 and R_4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R_1 and R_3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R_2 and R_4 .

| DATA INPUT | | ANALOG OUTPUT | |
|----------------|-------|------------------------|--|
| MSB ↓ | ↓ LSB | $+V_{REF}$ (2047/2048) | |
| 1111 1111 1111 | | $+V_{REF}$ (1/2048) | |
| 1000 0000 0001 | | 0 Volts | |
| 1000 0000 0000 | | $-V_{REF}$ (1/2048) | |
| 0111 1111 1111 | | $-V_{REF}$ (2048/2048) | |
| 0000 0000 0000 | | | |

TABLE III. Bipolar Output Code.

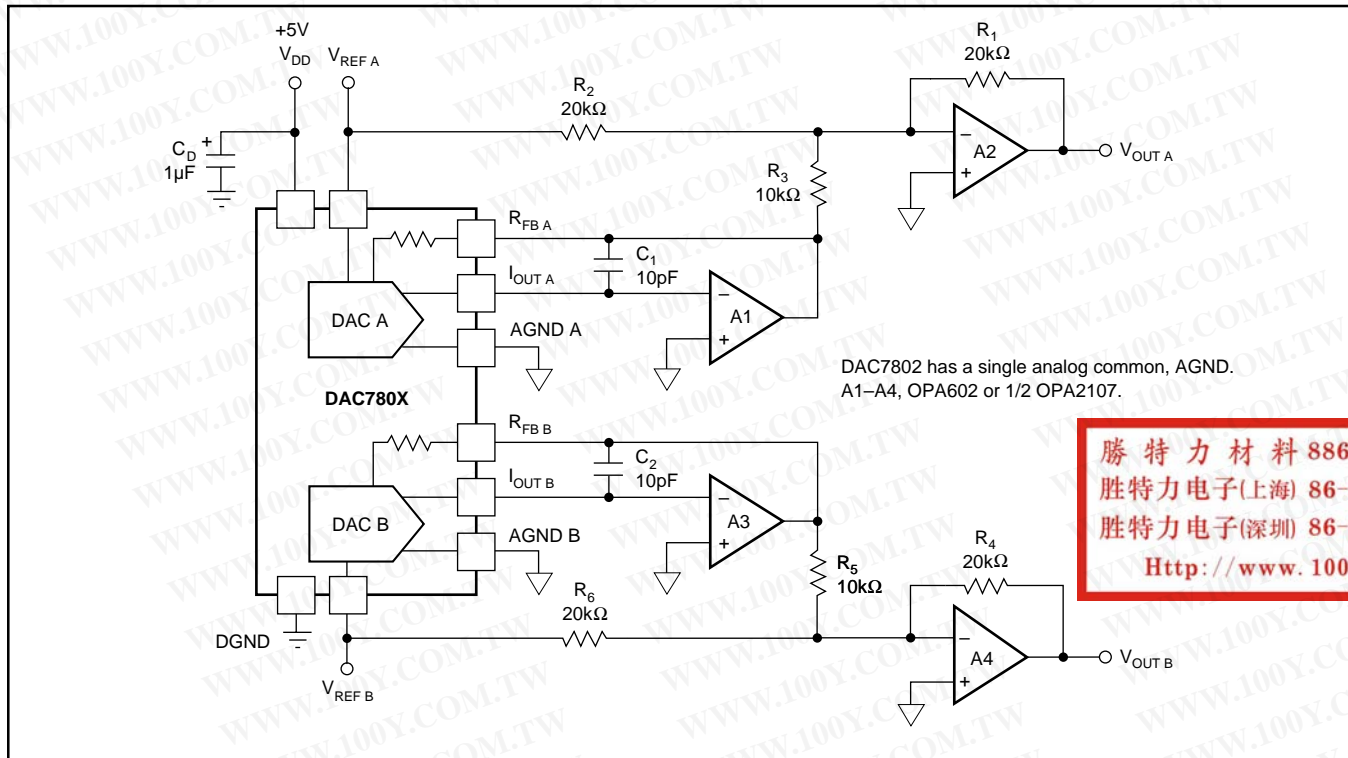


FIGURE 5. Bipolar Configuration.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

APPLICATIONS

12-BIT PLUS SIGN DACS

For a bipolar DAC with 13 bits of resolution, two solutions are possible. The addition of a precision difference amplifier and a high speed JFET switch provides a 12-bit plus sign voltage-output DAC, see Figure 7. When the switch selects the op amp output, the difference amplifier serves as a noninverting output buffer. If the analog ground side of the switch is selected, the output of the difference amplifier is inverted.

Another option, see Figure 8, also produces a 12-bit plus sign output without the additional switch and digital control line.

DIGITALLY PROGRAMMABLE ACTIVE FILTER

See Figure 9 for the DAC780x in a digitally programmable active filter application. The design is based on the state-variable filter, Texas Instruments UAF42, an active filter topology that offers stable and repeatable filter characteristics.

DAC1 and DAC2 can be updated in parallel with a single word to set the center frequency of the filter. DAC 4, which makes use of the uncommitted op amp in UAF42, sets the Q of the filter. DAC3 sets the gain of the filter transfer function without changing the Q of the filter. The reverse is also true.

The center frequency is determined by $f_c = 1/2\pi RC$ where R is the ladder resistance of the DAC (typical value, 10kΩ) and C the internal capacitor value (1000pF) of the UAF42. External capacitors can be added to lower the center frequency of the filter. But the highest center frequency for this circuit will be about 16kHz because the effective series resistance of the DAC cannot be less than 10kΩ.

Note that the ladder resistance of the DAC may vary from device to device. Thus, for best tracking, DAC2 and DAC3 should be in the same package. Some calibration may be necessary from one filter to another.

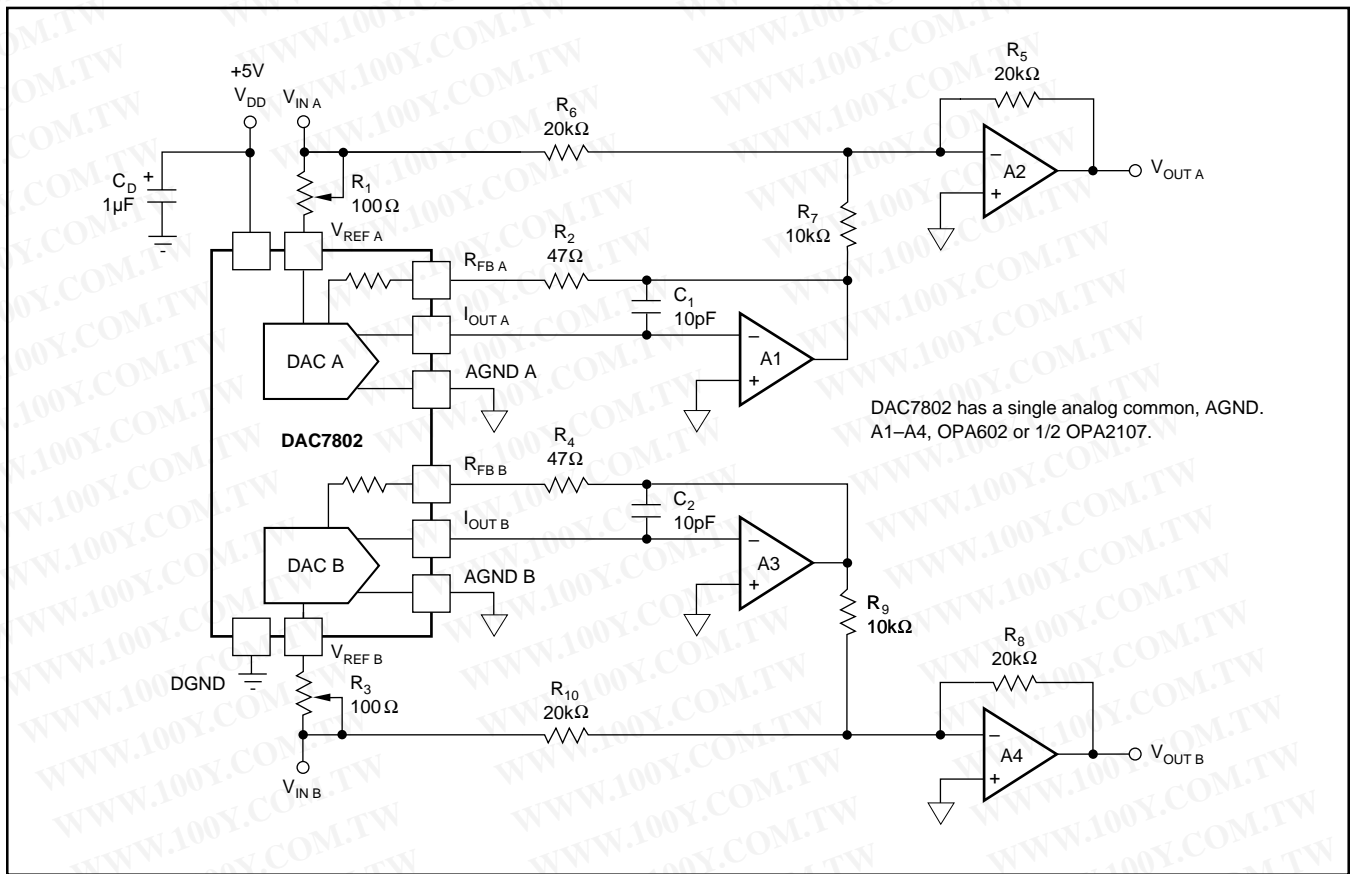


FIGURE 6. Bipolar Configuration with Gain Trim.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

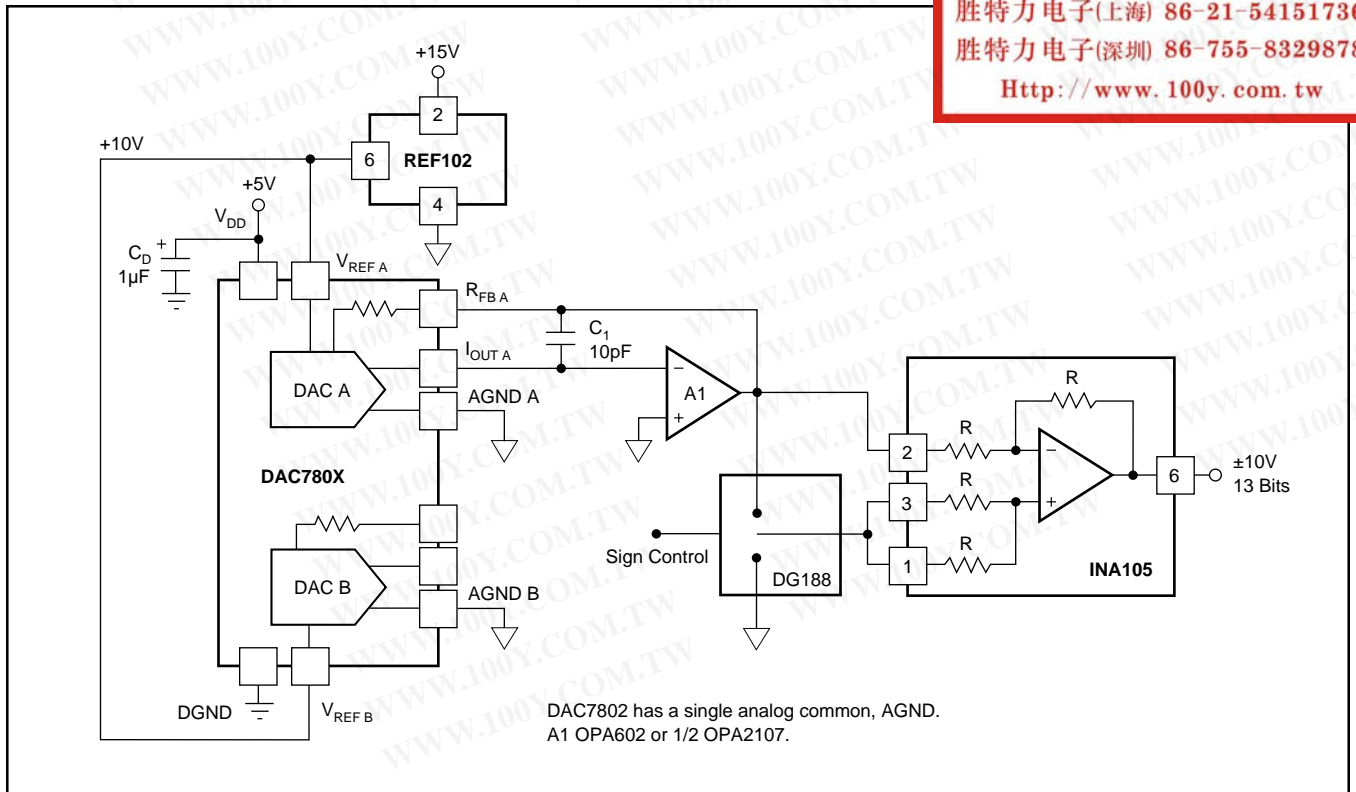


FIGURE 7. 12-Bit Plus Sign DAC.

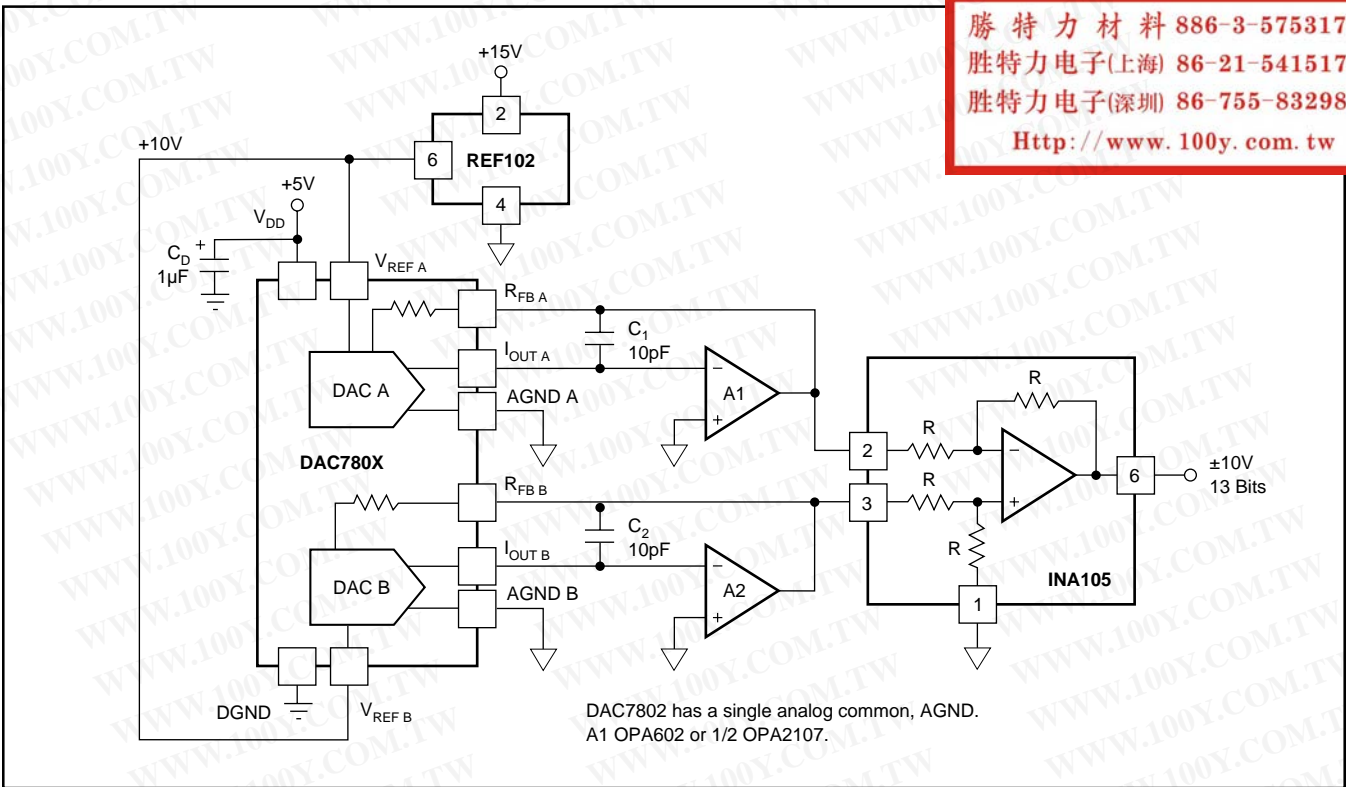


FIGURE 8. 13-Bit Bipolar DAC.

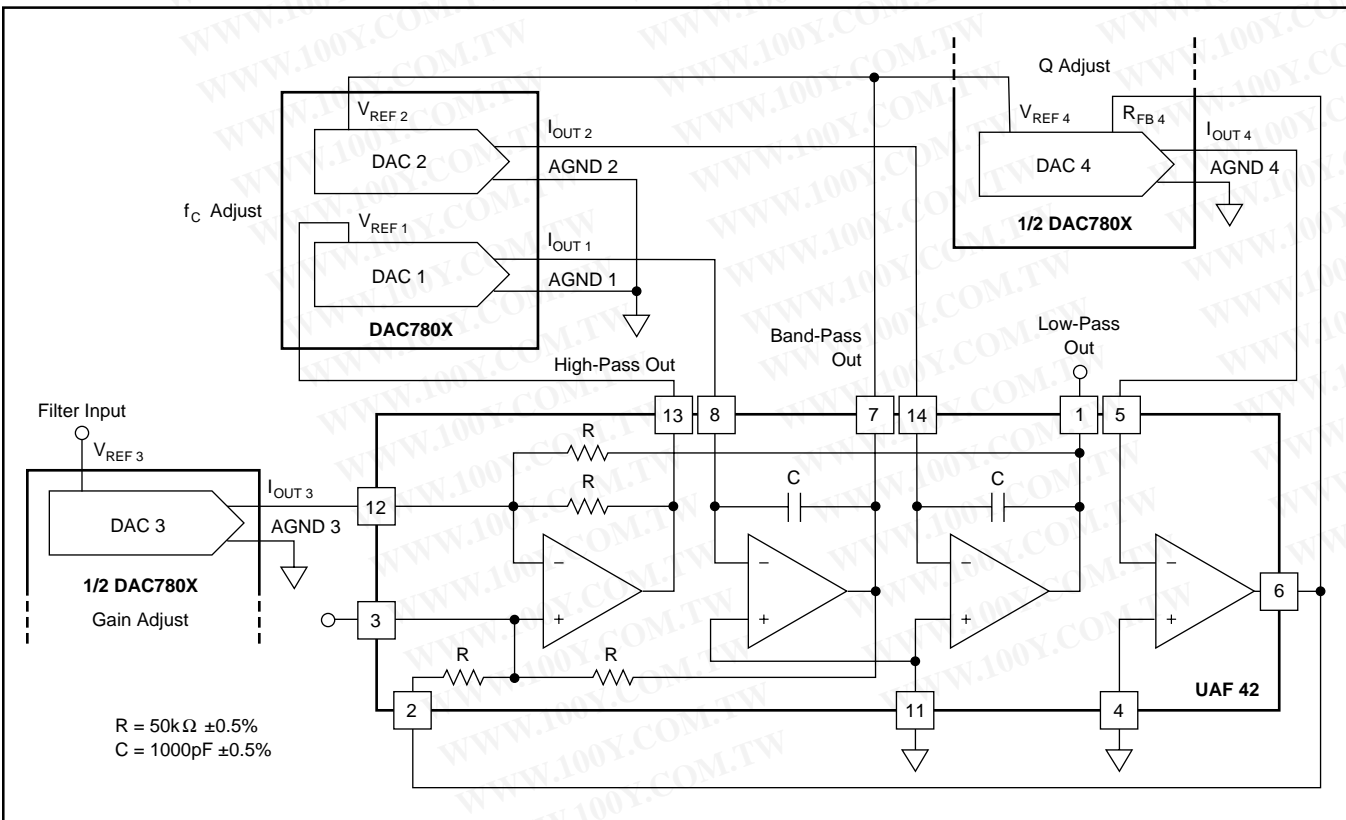
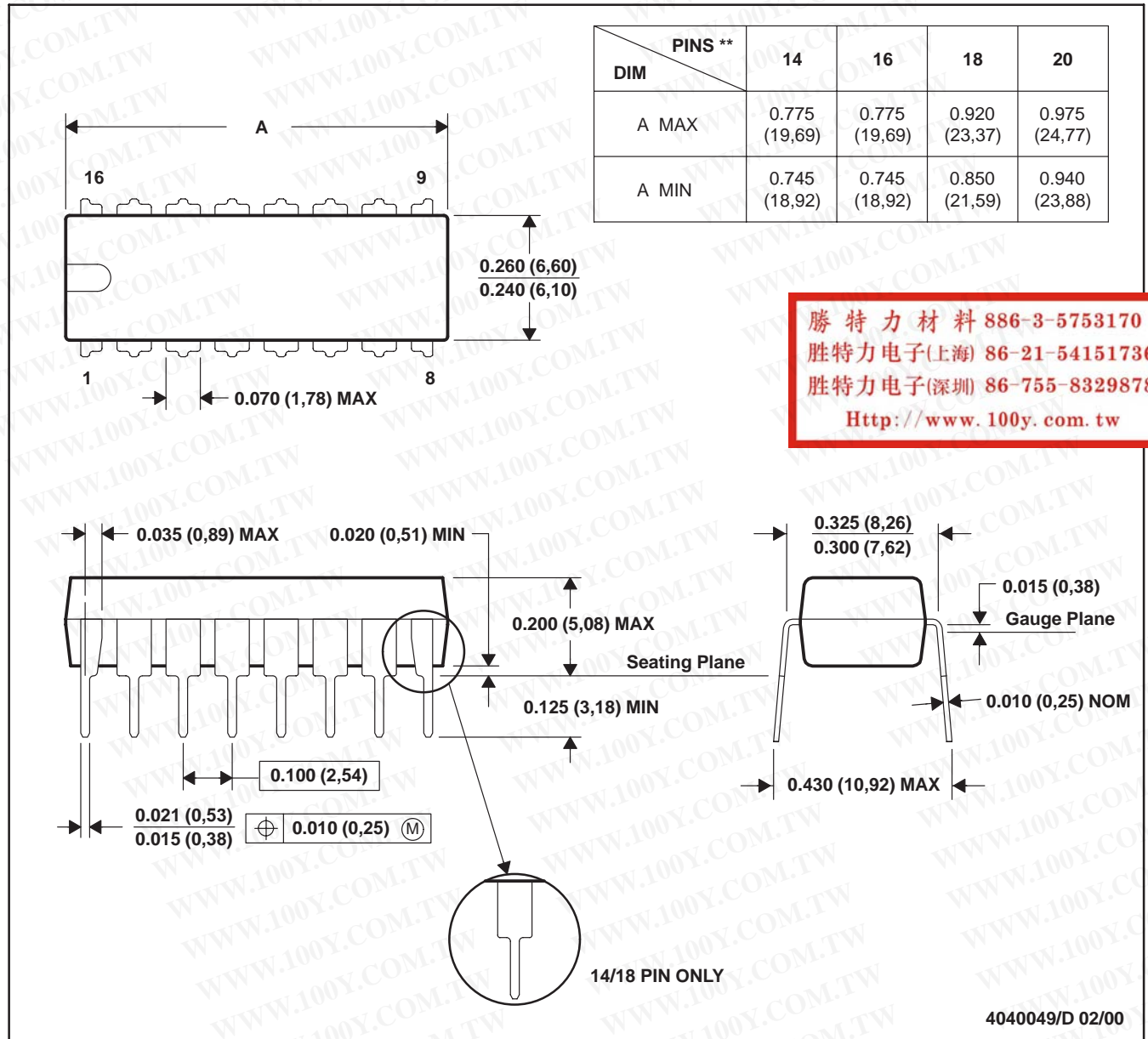


FIGURE 9. Digitally Programmable Universal Active Filter.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

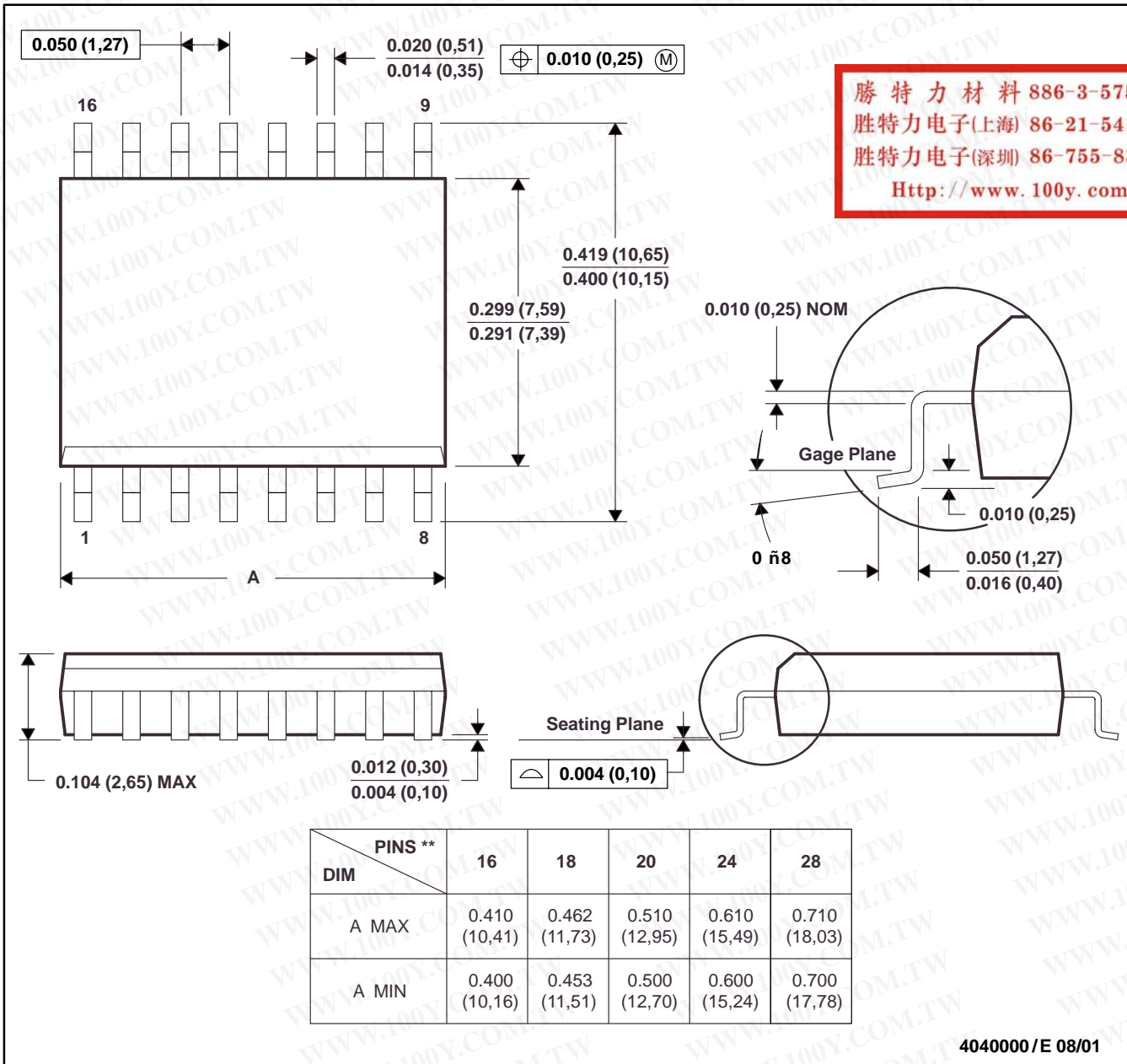


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN

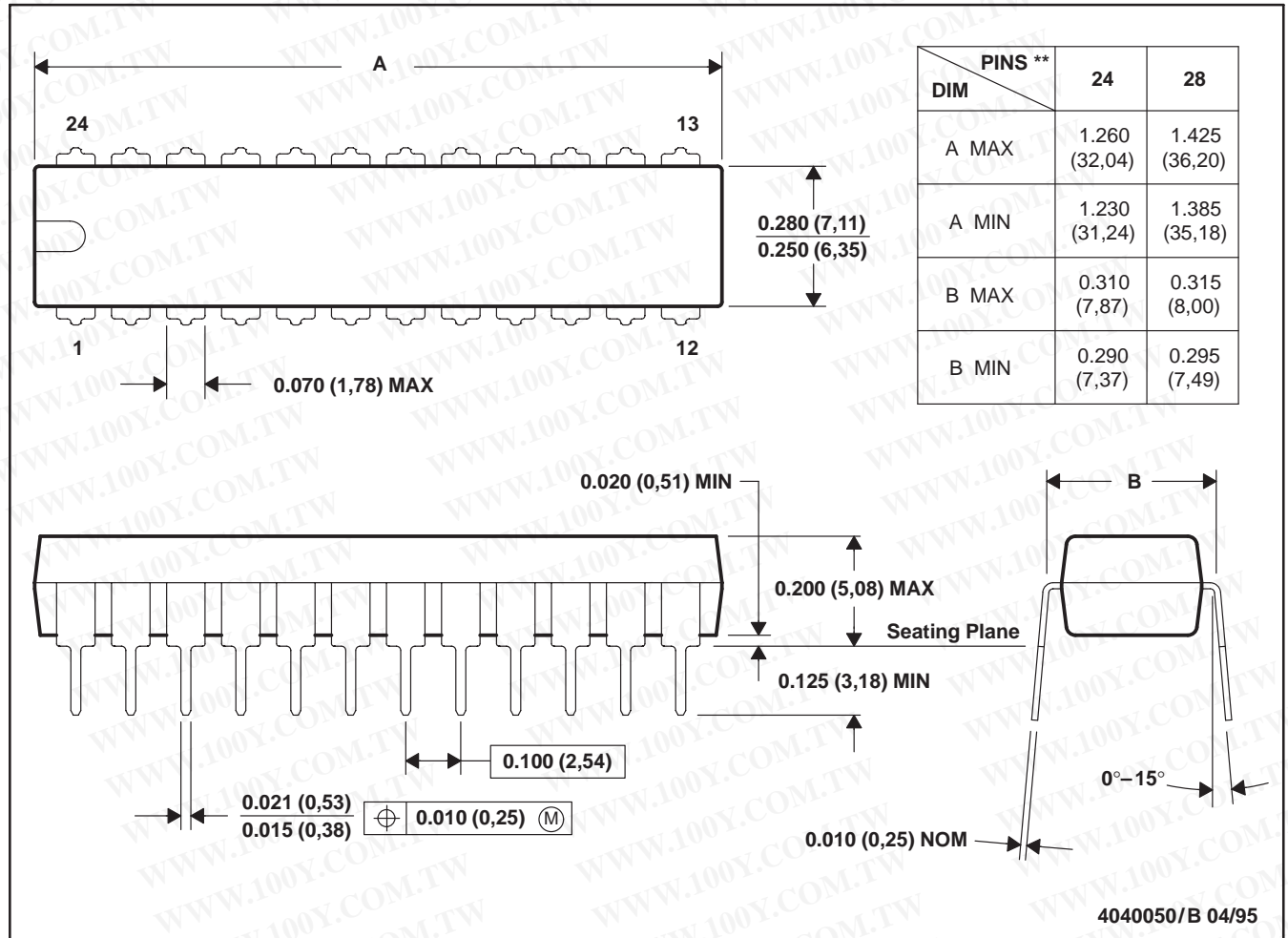


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN

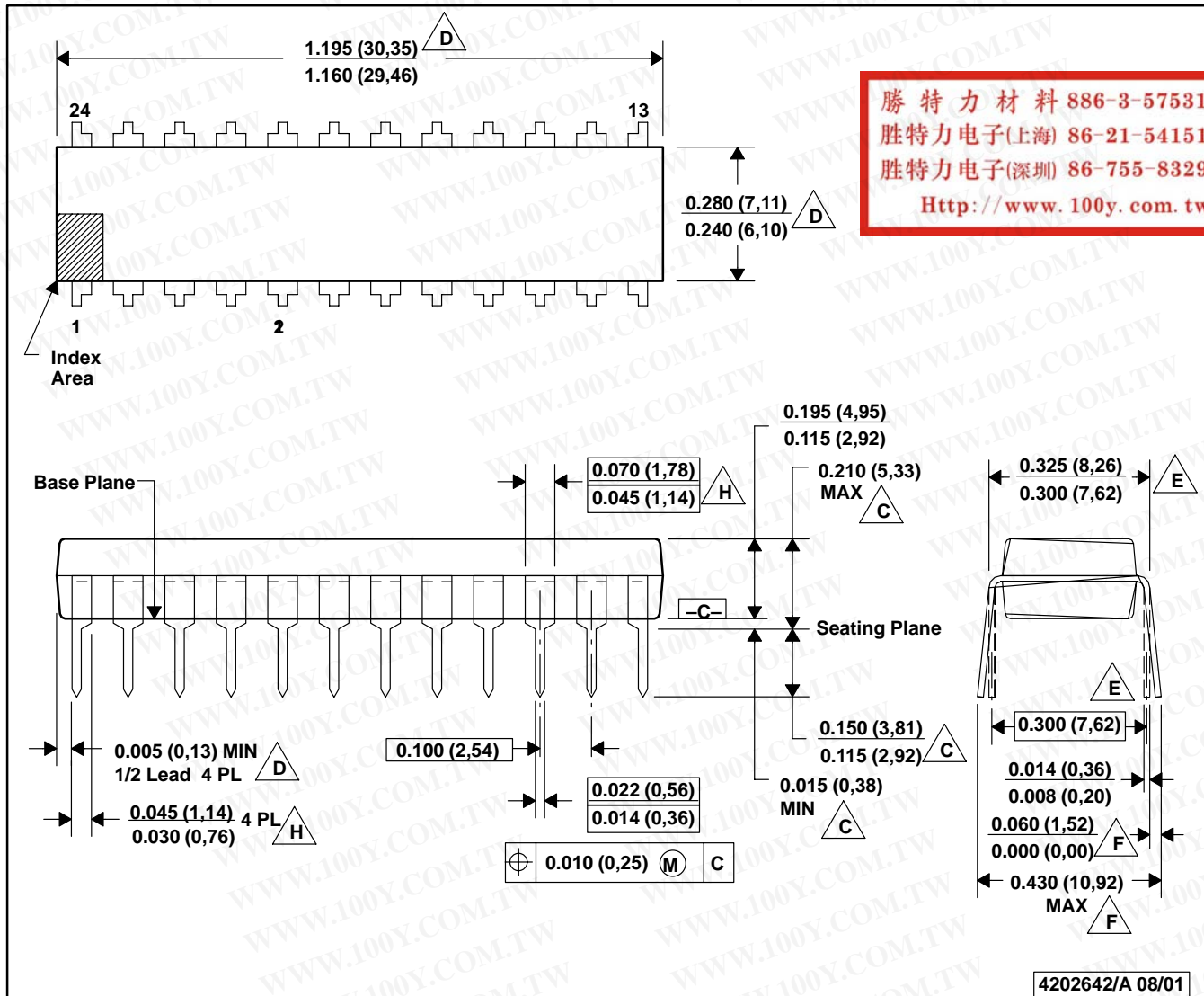


NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

NTG (R-PDIP-T24)

PLASTIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.
 - D. Dimensions do not include mold flash or protrusions.
 - E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
 - F. Dimensions are measured at the lead tips with the leads unconstrained.
 - G. Pointed or rounded lead tips are preferred to ease insertion.
 - H. Maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
 - I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
 - J. A visual index feature must be located within the cross-hatched area.
 - K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
 - L. Controlling dimension in inches.
 - M. Falls within JEDEC MS-011-AB.

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2001, Texas Instruments Incorporated