DS1220AB/AD
16k Nonvolatile SRAM

DALLAS SEMICONDUCTOR **MAXIM**

www.maxim-ic.com

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 2k x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 24-pin DIP package
- Read and write access times as fast as 100 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1220AD)
- Optional ±5% V_{CC} operating range (DS1220AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT

A7	1		24	VCC
A6	2		23	A8
A5	3		22	$\overline{A9}$
A4	4		21	$\overline{WE}$
A3	5		20	$\overline{OE}$
A2	6		19	A10
A1	7		18	$\overline{CE}$
A0	8		17	DQ7
DQ0	9		16	DQ6
DQ1	10		15	DQ5
DQ2	11		14	DQ4
GND	12		13	DQ3

24-Pin ENCAPSULATED PACKAGE
720-mil EXTENDED

PIN DESCRIPTION

A0-A10	- Address Inputs
DQ0-DQ7	- Data In/Data Out
$\overline{CE}$	- Chip Enable
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
V_{CC}	- Power (+5V)
GND	- Ground

DESCRIPTION

The DS1220AB and DS1220AD 16k Nonvolatile SRAMs are 16,384-bit, fully static, nonvolatile SRAMs organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAMs can be used in place of existing 2k x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The devices also match the pinout of the 2716 EPROM and the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

121907

READ MODE

The DS1220AB and DS1220AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 11 address inputs (A0-A10) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{CE}$ and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later-occurring signal and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1220AB and DS1220AD execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1220AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5V. The DS1220AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1220AB and 4.5 volts for the DS1220AD.

FRESHNESS SEAL

Each DS1220 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	+260°C for 10 seconds
Caution: Do Not Reflow	(Wave or Hand Solder Only)

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS   (T_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1220AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1220AD Power Supply Voltage	V_{CC}	4.50	5.0	5.50	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

(T_A: See Note 10)
(V_{CC} =5V $\pm$ 5% for DS1220AB)

DC ELECTRICAL CHARACTERISTICS   (V_{CC} =5V $\pm$ 10% for DS1220AD)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	μA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	μA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current (Commercial)	I_{CC01}			75	mA	
Operating Current (Industrial)	I_{CCO1}			85	mA	
Write Protection Voltage (DS1220AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1220AD)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE   (T_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

(T$_A$: See Note 10)

(V$_{CC}$ =5.0V $\pm$ 5% for DS1220AB)

AC ELECTRICAL CHARACTERISTICS

(V$_{CC}$ =5.0V $\pm$ 10% for DS1220AD)

PARAMETER	SYMBOL	DS1220AB-100 DS1220AD-100		DS1220AB-120 DS1220AD-120		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t$_{RC}$	100		120		ns	
Access Time	t$_{ACC}$		100		120	ns	
$\overline{OE}$ to Output Valid	t$_{OE}$		50		60	ns	
$\overline{CE}$ to Output Valid	t$_{CO}$		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t$_{COE}$	5		5		ns	5
Output High Z from Deselection	t$_{OD}$		35		35	ns	5
Output Hold from Address Change	t$_{OH}$	5		5		ns	
Write Cycle Time	t$_{WC}$	100		120		ns	
Write Pulse Width	t$_{WP}$	75		90		ns	3
Address Setup Time	t$_{AW}$	0		0		ns	
Write Recovery Time	t$_{WR1}$	0		0		ns	12
	t$_{WR2}$	10		10		ns	13
Output High from $\overline{WE}$	t$_{ODW}$		35		35	ns	5
Output Active from $\overline{WE}$	t$_{OEW}$	5		5		ns	4
Data Setup Time	t$_{DS}$	40		50		ns	4
Data Hold Time	t$_{DH1}$	0		0		ns	12
	t$_{DH2}$	10		10		ns	13

AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	SYMBOL	DS1220AB-150 DS1220AD-150		DS1220AB-200 DS1220AD-200		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		150		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1}	0		0		ns	12
	t_{WR2}	10		10		ns	13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	4
Data Setup Time	t_{DS}	60		50		ns	4
Data Hold Time	t_{DH1}	0		0		ns	12
	t_{DH2}	10		10		ns	13

READ CYCLE
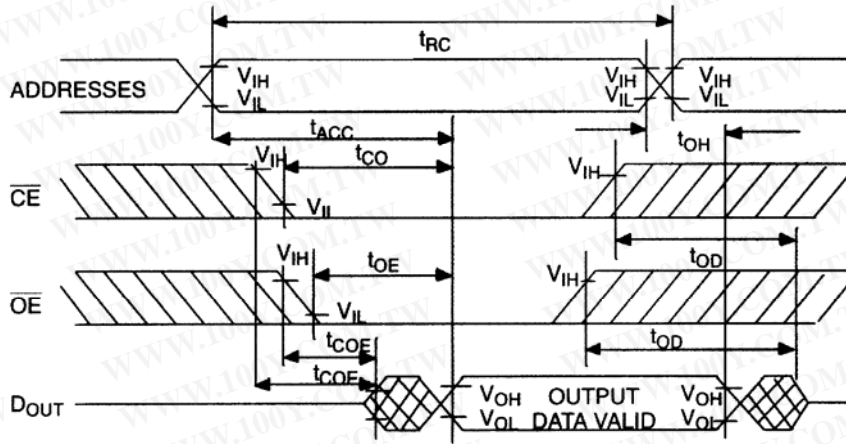
SEE NOTE 1

WRITE CYCLE 1
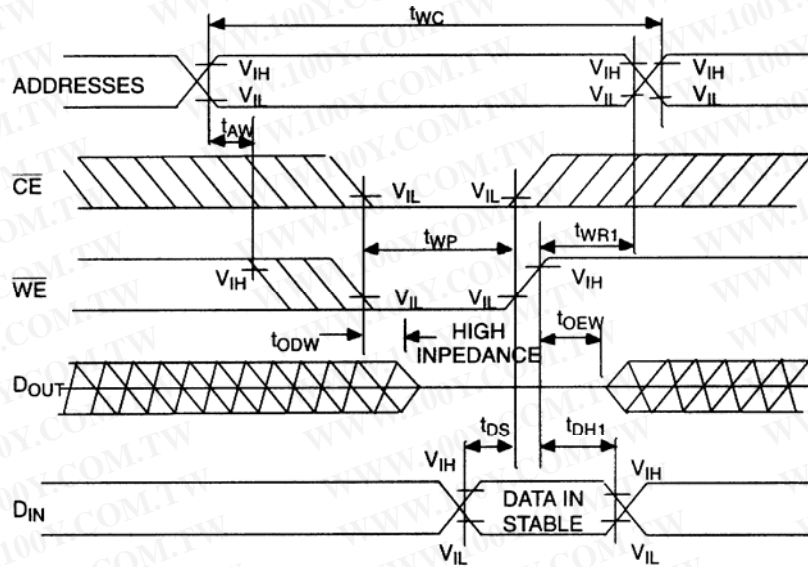
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2
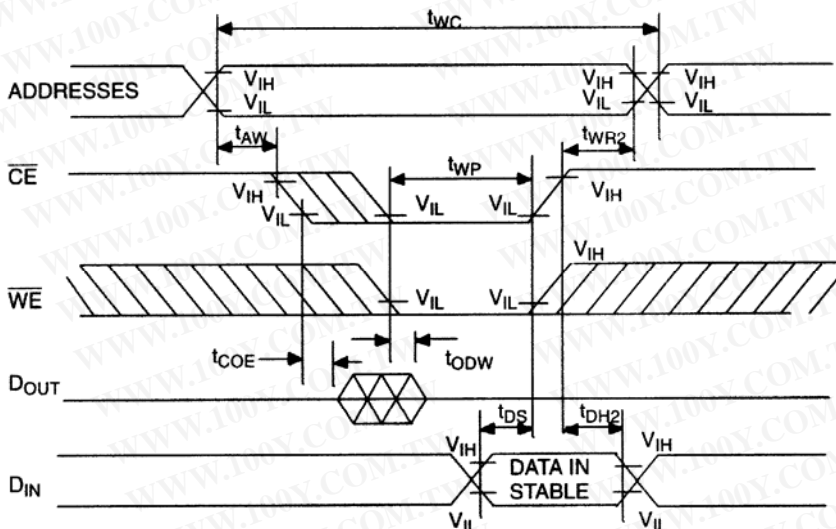
SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION
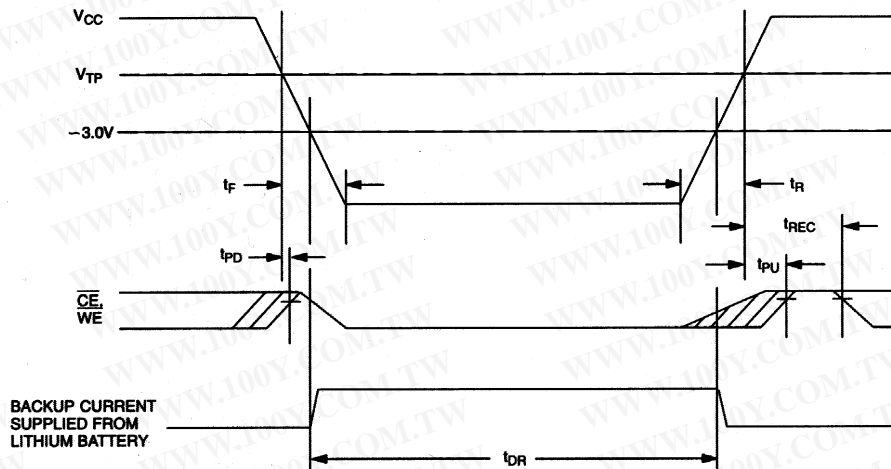
SEE NOTE 11

POWER-DOWN/POWER-UP TIMING $\qquad$ (T$_A$: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V$_{CC}$ Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive	t$_{PD}$			1.5	µs	11
V$_{CC}$ slew from V$_{TP}$ to 0V	t$_F$	300			µs	
V$_{CC}$ slew from 0V to V$_{TP}$	t$_R$	300			µs	
V$_{CC}$ Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	t$_{PU}$			2	ms	
V$_{CC}$ Valid to End of Write Protection	t$_{REC}$			125	ms	

(T$_A$ =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t$_{DR}$	10			years	9

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in the battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V$_{IH}$ or V$_{IL}$. If $\overline{OE}$ = V$_{IH}$ during write cycle, the output buffers remain in a high-impedance state.
3. t$_{WP}$ is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t$_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{CE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t$_{DS}$ is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.

8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.

9. Each DS1220AB and each DS1220AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user. This parameter is guaranteed by design and is not 100% tested.

10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.

11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

12. t_{WR1} , t_{DH1} are measured from $\overline{WE}$ going high.

13. t_{WR2} , t_{DH2} are measured from $\overline{CE}$ going high.

14. DS1220 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

DC TEST CONDITIONS
Outputs Open
Cycle = 200ns for Operating Current
All Voltages Are Referenced to Ground

AC TEST CONDITIONS
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	SUPPLY TOLERANCE	PIN/PACKAGE	SPEED GRADE
DS1220AB-100	0°C to +70°C	5V ± 5%	24 / 720 EMOD	100ns
DS1220AB-100+	0°C to +70°C	5V ± 5%	24 / 720 EMOD	100ns
DS1220AB-100IND	-40°C to +85°C	5V ± 5%	24 / 720 EMOD	100ns
DS1220AB-100IND+	-40°C to +85°C	5V ± 5%	24 / 720 EMOD	100ns
DS1220AB-120	0°C to +70°C	5V ± 5%	24 / 720 EMOD	120ns
DS1220AB-120+	0°C to +70°C	5V ± 5%	24 / 720 EMOD	120ns
DS1220AB-150	0°C to +70°C	5V ± 5%	24 / 720 EMOD	150ns
DS1220AB-150+	0°C to +70°C	5V ± 5%	24 / 720 EMOD	150ns
DS1220AB-200	0°C to +70°C	5V ± 5%	24 / 720 EMOD	200ns
DS1220AB-200+	0°C to +70°C	5V ± 5%	24 / 720 EMOD	200ns
DS1220AB-200IND	-40°C to +85°C	5V ± 5%	24 / 720 EMOD	200ns
DS1220AB-200IND+	-40°C to +85°C	5V ± 5%	24 / 720 EMOD	200ns
DS1220AD-100	0°C to +70°C	5V ± 10%	24 / 720 EMOD	100ns
DS1220AD-100+	0°C to +70°C	5V ± 10%	24 / 720 EMOD	100ns
DS1220AD-100IND	-40°C to +85°C	5V ± 10%	24 / 720 EMOD	100ns
DS1220AD-100IND+	-40°C to +85°C	5V ± 10%	24 / 720 EMOD	100ns
DS1220AD-120	0°C to +70°C	5V ± 10%	24 / 720 EMOD	120ns
DS1220AD-120+	0°C to +70°C	5V ± 10%	24 / 720 EMOD	120ns
DS1220AD-150	0°C to +70°C	5V ± 10%	24 / 720 EMOD	150ns
DS1220AD-150+	0°C to +70°C	5V ± 10%	24 / 720 EMOD	150ns
DS1220AD-200	0°C to +70°C	5V ± 10%	24 / 720 EMOD	200ns
DS1220AD-200+	0°C to +70°C	5V ± 10%	24 / 720 EMOD	200ns
DS1220AD-200IND	-40°C to +85°C	5V ± 10%	24 / 720 EMOD	200ns
DS1220AD-200IND+	-40°C to +85°C	5V ± 10%	24 / 720 EMOD	200ns

+ *Denotes lead-free/RoHS-compliant product.*

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

PACKAGE INFORMATION

(For the latest package outline information, go to **http://www.maxim-ic.com/DallasPackInfo**.)

PACKAGE TYPE	DOCUMENT NO.
24 DIP	**56-G0002-001**

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
121907	Added package information table. Removed the DIP module package drawing and dimension table.	9

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw