

54LS109/DM54LS109A/DM74LS109A Dual Positive-Edge-Triggered J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

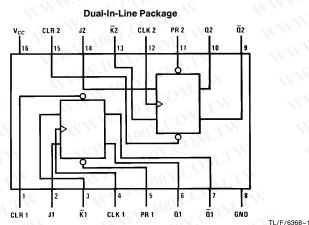
This device contains two independent positive-edge-triggered J-K flip-flops with complementary outputs. The J and \overline{K} data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and \overline{K} inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or

clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

Alternate Military/Aerospace device (54LS109) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications

Connection Diagram



Order Number 54LS109DMQB, 54LS109FMQB, DM54LS109AJ, DM54LS109AW, DM74LS109AM or DM74LS109AN See NS Package Number J16A, M16A, N16E or W16A

Function Table

© 1995 National Semiconductor Corporation

	144.1	Outputs				
PR	CLR	CLK	J	ĸ	Q	Q
L	н	X	Х	X	Н	L
н	- E	Х	X	X	_ L <	н
L	L	X	X	X	H*	H*
н	H	↑	L	CL.	L	🔨 Н 👘
н	н	1	Н	L.,	То	ggle
н	H at	1	L	τ H	Q ₀	ggle Q ₀
н	н	1	H	н	H.) - L
Н	н	Ĺ	X	X	Q ₀	\overline{Q}_0

TL/F/6368

н	÷	High	Lc	gic	Lev	el

ow Logic Leve X = Either Low or High Logic Level

 \uparrow = Rising Edge of Pulse

= This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) state.

 $Q_0 =$ The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse

RRD-B30M105/Printed in U. S. A

料 886-3-5753170 カ 材 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www. 100y. com. tw

with Preset, 4LS109/DM54LS Clear, and 109A/DM74LS109A Dua **Complementary Outputs** Positive-Edge-Triggered J-K Flip-Flops

June 1989

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

OX.COM.T

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature	Range
DM54LS and 54LS	-55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

WWW.100Y.CC

WWW.100Y.COM.TW

Recommended Operating Conditions

Symbol	Para	meter	0 Y . [OM54LS109	A		DM74LS109	Α	Units
o y inizor			Min	Nom	Max	Min	Nom	Max	onite (
Vcc	Supply Voltage	.WW.	4.5	5	5.5	4.75	5	5.25	v
VIH	High Level Input	Voltage	2	M		2	TAN.	100	V
VIL	Low Level Input	Low Level Input Voltage			0.7	~		0.8	v
Іон	High Level Outp	ut Current	1.10-		-0.4		WWW	-0.4	mA
IOL	Low Level Outpu	ut Current	W.100	CO	4			8	mA
fCLK	Clock Frequency	Clock Frequency (Note 2)		N	25	0	N.	25	MHz
fCLK	Clock Frequency	(Note 3)	0	N.CL	20	0	WV	20	MHz
tw	Pulse Width	Clock High	18		011.	18		NN.L	ns
	(Note 2)	Preset Low	15	1001.	- Mo-	15		WIN.	
111	NY.COM	Clear Low	15	100%		15	V		
W	Pulse Width	Clock High	25		COm	25		NN NY	ns
	(Note 3)	Preset Low	20	N.100		20		W	
111	1001.00	Clear Low	20	- NI 100		20			N.100
tsu	Setup Time	Data High	30↑		N.C	30↑		A W	ns
TAN	(Notes 1 & 2)	Data Low	20 ↑	NN.L	V.C	20 ↑	N.	NV.	
t _{SU}	Setup Time	Data High	35 ↑	.W.		35↑			ns
(Notes 1 & 3)	(Notes 1 & 3)	Data Low	25 ↑		1001.	25 ↑	C.V.	N	113
t _H	Hold Time (Note	4)	0↑	NNN	Yan	0↑	WT.		ns
T _A	Free Air Operatii	ng Temperature	-55	IN	125	0	N	70	°C

Note 1: The symbol (1) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 2 k\Omega, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 k\Omega, T_A = 25°C and V_{CC} = 5V.

Note 4: $T_A = 25^{\circ}C$ and $V_{CC} = 5V$.

勝特力材料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www. 100y. com. tw WWW.100Y.COM

WW.100X.COM.TW

WWW.100Y.COM

WWW.100Y.COM.TW

WWW.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)										
Symbol	Parameter	Conditions	N WW	Min	Typ (Note 1)	Max	Units			
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$	N. IN	1.100 -	COM	-1.5	V			
VOH	High Level Output	$V_{CC} = Min, I_{OH} = Max$	DM54	2.5	3.4	TN	- V			
` ≪1	Voltage	$V_{IL} = Max, V_{IH} = Min$	DM74	2.7	3.4	W				
VOL	Low Level Output	$V_{CC} = Min, I_{OL} = Max$	DM54	N.10	0.25	0.4	v			
	Voltage	$V_{IL} = Max, V_{IH} = Min$	DM74		0.35	0.5				
		$I_{OL} = 4 \text{ mA}, V_{CC} = Min$	DM74	AN.	0.25	0.4]			
MITWOM.TW	Input Current @ Max Input Voltage	$V_{CC} = Max$ $V_I = 7V$	J, K		100 2	0.1	- mA			
			Clock		1001.0	0.1				
			Preset			0.2				
			Clear		N.100 X	0.2				
Чн	High Level Input	$V_{CC} = Max$ $V_1 = 2.7V$	J, K	N.V.	1001	20	μA			
	Current		Clock	N.	N.	20				
COM.		100X. ON.	Preset		-N.100	40				
		VV. COM	Clear	N	10	40				
$\mu_{\rm C} 0^{\rm M}$	Low Level Input Current	$V_{CC} = Max$ $V_1 = 0.4V$	J, K	×	WW.	-0.4	mA			
N.C.			Clock			-0.4				
V.CO			Preset		NN .	-0.8				
			Clear		ANN.	-0.8				
I _{OS}	Short Circuit Output Current	V _{CC} = Max	DM54	-20		-100	CON			
		(Note 2)	DM74	-20	N.	-100	mA			
Icc	Supply Current	V _{CC} = Max (Note 3)	O	 1	4	8	mA			

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	WTW	From (Input) To (Output)		00 x.			
	Parameter		CL =	15 pF	C _L =	Units	
			Min	Max	Min	Max	
fMAX	Maximum Clock Frequency	WWW	25	ON.IT	20	WW	MHz
t _{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or \overline{Q}	100Y	25	W	35	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or \overline{Q}	100	30	TW.	35	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	Clear to \overline{Q}	N.10	25	I.TW	35 🔨	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q	WW.1	30	M.TW	35	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q	WWW.	25	OWL	35	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Preset to Q	WWW	30	CONF	35	ns

N.COM.TW JOY.COM.TW 100Y.COM.TW

Note 1: All typicals are at V_{CC} = 5V, T_A = 25^{\circ}C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where $V_0 = 2.25V$ and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

3

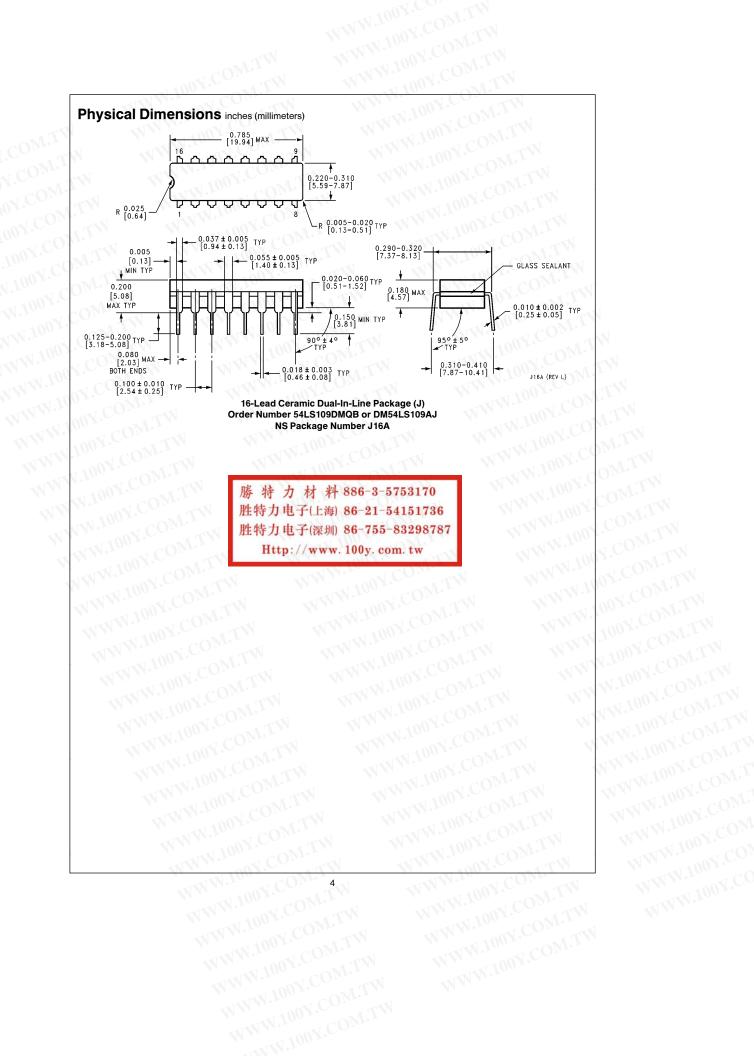
100X.CO

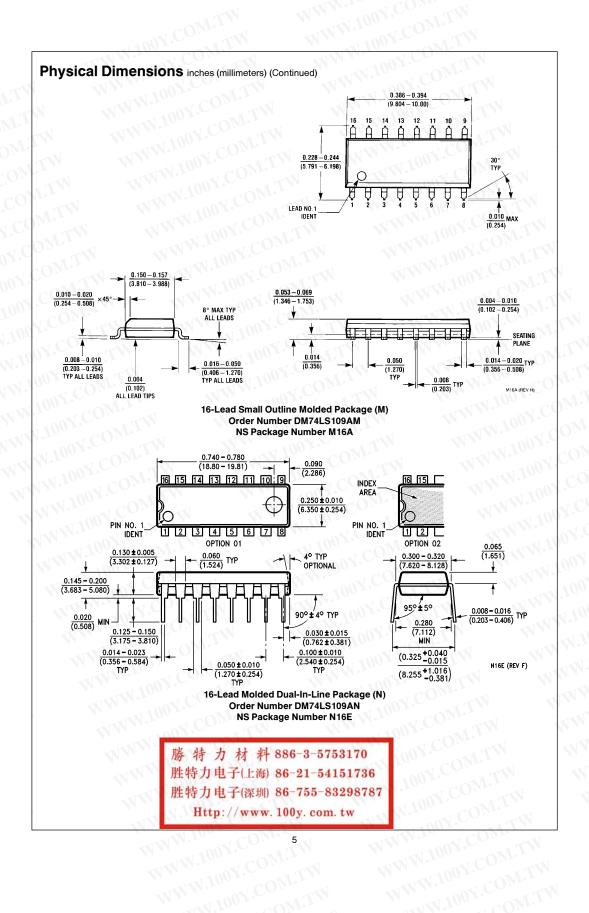
100Y.COM.TW

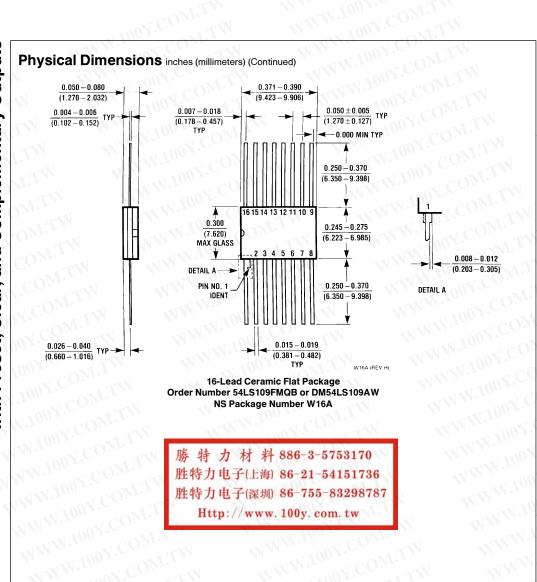
Note 3: I_{CC} is measured with all outputs open, with CLOCK grounded after setting the Q and \overline{Q} outputs high in turn.

WWW.100Y.C

勝特力材料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www. 100y. com. tw







LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

R