

PROGRAM TIMING

I. General Description

The EM78PXXX is a series of 8-bit microcontrollers with low-power and high-speed CMOS technology. They are equipped with Electrical One Time Programmable Read Only Memory (OTP-ROM). The OTP memory provides not only the security bit to protect the memory itself from intruding, but also the option bits to meet users' requirements.

The OTP EPROM is embedded inside EM78PXXX 8-bit microcontrollers instead of the mask memory. Users' developed programs can be easily programmed into or verify from this OTP memory by using EMC EPROM Writer.

II. Feature

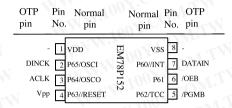
- \diamond Available in temperature range: 0°~70°C (commercial), or -40°~85°C (industrial).
- Optional instruction cycle periods:
 - * Two oscillator clocks, or
 - * Four oscillator clocks.
- Low power consumption:
 - * < 2mA, at 5V / 4MHz, or
 - * 15mA typical, at 3V / 32KHz.
- One Security Register is provided to protect the OTP memory code.
- One Configuration Register is provided to meet the user's options.
- 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges, and with overflow interrupt.
- ♦ Programmable free running on-chip watchdog timer.
- Power-down mode.
- ♦ Input port changed interrupt (wake-up), and external interrupt available.
- \$\display 99.9\% signal instruction cycle commands.
- Power on voltage detector.



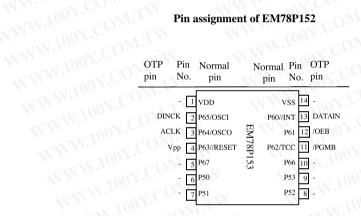
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III. Pin Configurations

1. Pin Assignments of EM78P152 and EM78P153



Pin assignment of EM78P152



Pin assignment of EM78P153

2. Pin Assignment of EM78P156E

f EM78	8P156E					
OTP pin	Pin No.	Normal pin	I	Normal Pi pin N		OTP pin
	. 1	P52	•	P51	18	DINCK
	2	P53		P52	17	DATAIN
	- 3	TCC	E	OSCI	16	/PGMB
	Vpp 4	/RESET	EM78P156E	osco	15	ACLK
	5	VSS	P15	VDD	14	ī] -
	_ 6	P60,/INT	Œ	P67	13	OEB
	_ 7	P61		P66	12	<u>-</u>
	- 8	P62		P65	11] -
	- 9	P63		P64	10	<u>-</u>

Pin assignment of EM78P156E



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	in Io.	Normal pin	Norr pii	nal Pi 1 N	n OTP o. pin
1	T		OUT !		TW
Vpp	1	TCC	100	RESET	28 BS
=	2	VDD		OSCI	27 -
-	3	NC		osco	26 ACLK
	4	VSS		P77	25 -
N -	5	/INT	×₩ 10	P76	24 -
-	6	P50	EM78P447A	P75	23 -
L ' -≪1 =	7	P51	8P4	P74	22 -
/OE	8	P52	47,4	P73	21 -
/PGM	9	P53	1	P72	20 -
IO0,C0	10	P60		P71	19 -7 ()
IO1,C1	11	P61		P70	18 -
IO2,C2	12	P62		P67	17 -
IO3	13	P63		P66	16 IO6
IO4	14	P64		P65	15 105
	N	-		W	

Pin assignment of EM78P447A

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Pin assignmen	nt of EM78P447A
OTP Pin Normal pin No. pin	Normal Pin OTP pin No. pin
P55	P56 32 -
- 2 P54	P57 31 -
Vpp 3 TCC	/RESET 30 BS
- 4 VDD	OSCI 29
- 5 NC	OSCO 28 ACLK
- 6 vss	P77 27 -
- 7/INT	P77 27
- 8 P50	P75 25 -
- 9 P51	B P74 24 -
/OE 10 P52	P73 23 -
/PGM 11 P53	P72 22 -
IO0,C0 12 P60	P71 21 -
IO1,C1 13 P61	P70 20 -
IO2,C2 14 P62	P67 19 -
IO3 15 P63	P66 18 IO6
IO4 16 P64	P65 17 IO5

Pin assignment of EM78P447B



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OTP pin	Pin No.	Normal pin	Norma pin	al Pin No	
	No 1 - 2 - 3 - 4 - 5 - 6 - 7 - 8 - 9 - 10 - 11		pin /RE	No DOSCI DOSCO P77 P76 P75 P74 P73 P72 P71 P70	
	13	P63 P64	WWY	P66	17 - 16 - 15 -

Pin assignment of EM78P447SA

	TW	103 13	ON: TW
	Pin assignment	of EM/8P447	SA
OTI pin	Pin Normal No. pin	Normal Pin pin No.	OTP pin
	- 1 P55 - 2 P54	P56 32 P57 31	W.100Y.COM.TW
	- 3 TCC	/RESET 30	M.M. TOOX. COM. T.M.
	- 4 VDD - 5 NC	OSCI 29 OSCO 28 P77 27	VPP
	- 6 VSS M - 7 /INT - 8 P50 + 9 P51 B	P76 26	ACLK DINCK
	01 J	P75 25 P74 24 P73 23	DATAIN
	- 11 P53	P72 22	PGMB OEB
	- 13 P61	P71 21 P70 20	
	- 14 P62 - 15 P63	P67 19 P66 18	
	- 16 P64	P65 17	-

Pin assignment of EM78P447SB



VW.100

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OTP pin	Pin No) Y •	Normal pin	Pin No.	OTP pin	<u> </u>	
V .	- 1	VSS		osco	40	ACLK		
Vpp	2	/INT		R-OSC	I 39	- 1		
<	- 3	DATA		VDI		77.		
	- 4	CLK		P70	-	OM^{-}		
-	=	P90		P7	_	BS		
-		P91		P7:	.⊏			
-	- 7	P92		P6'	-	100		
-	- 8	P93 P94	EM78P45	P66		IO6 IO5		
		P94 P95	78P4	P6:		104		
		P50	51	P6:	-	103		
-T		P51		P6:		102		
/OEE		P52		P6	-	IO1		
/PGME	´ <u>=</u>	P53		P60	27	100		
71 GIVIL	_	P54		P8'	26	00 r.		
TW.	16	P55		P86	25	= 003		
	17	P56		P8:	24	700		
	18	P57		P84	1 23	- 100		
17.	19	P80		P8:	3 22	1.1		
$\pi \Lambda T$	20	P81		P8:	2 21	at 10		
P458	Pin	assign	mer	it of E	М7	8P451		

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WWW.100Y.CO Pin Assignment of EM78P458 5. WWW.100

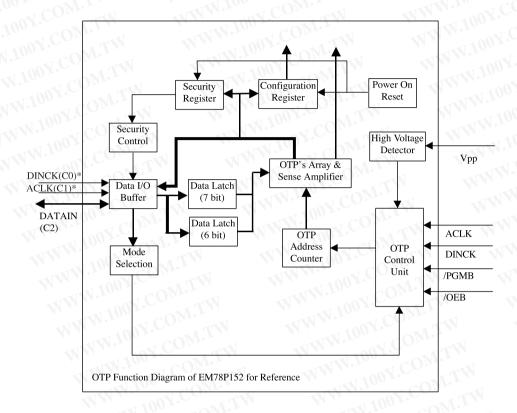
ssignment of EM78P458		
	in Normal Io. pin	Normal Pin OTP pin No. pin
WW.1007	1 P56 2 P57	P55 20 - P54 19 -
M.M.1001	3 P60 4 P61	osci 18 - osco 17 -
WWW.100	4 P61 XX	VDD 16 - P53 15 -
DATAIN	7 P63 8 P64	P52 14 - P51 13 /OEB
DINCK ACLK	9 P65 10 P66	P50 12 Vpp P67 11 /PGMB

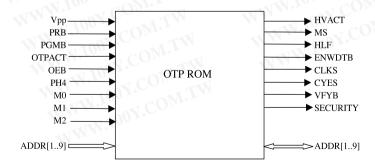
Pin assignment of EM78P458



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IV. Functional Block Diagram





OTP ROM input/output signals



PROGRAM TIMING

V. Pin Descriptions

. Pin Des	scription	ıs	
. EM78P152/ Symbol	3-OTP Pin Pin No.	Descriptions Type	Function
Vpp	4	I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	3	I	CLK for OTP memory address increment.
DATAIN	7/13	I/O	ROM code series input and series output pin.
DINCK	2 0	I	ROM code series input and output clock.
/PGMB	5/11	I	Program write enable. Active low.
/OEB	6/12	I	Output enable, Active low.

2. EM78P156E-OTP Pin Descriptions

WWW	1007.CO	OM.TW	WWW.100Y.COM.TW WWW.101
. EM78P156l Symbol	E-OTP Pin I Pin No.	Descriptions Type	Function
Vpp	4	COL	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	15	d	CLK for OTP memory address increment.
DATAIN	17	I/O	ROM code series input and series output pin.
DINCK	18	V. Clops	ROM code series input and output clock.
/PGMB	16	LOM	Program write enable. Active low.
/OEB	13	00 I	Output enable. Active low.

3. EM78P447 A/B-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp	1	I I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	26	1	CLK for OTP memory address increment.
IO0~IO6	10~16	I/O	7-bit Data Bus pins.
C0~C2	10~12	I	Mode code input pins. They are the secondary function of IO0~IO2.
BS	28	WY.10	High/Low byte selected pin. High byte (6-bit) is selected when BS is hit Low byte (7-bit) is selected when BS is low.
/PGM	9	I	Program write enable. Active low.
/OE	8	I	Output enable. Active low.



4. EM78P447SA/SB-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp C	28/30	I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	28/26	I	CLK for OTP memory address increment.
DATAIN	26/24	I/O	ROM code series input and series output pin.
DINCK	27/25	I	ROM code series input and output clock.
/PGMB	25/23	I	Program write enable. Active low.
/OEB	24/22	I	Output enable. Active low.

5. EM78P451-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp	2	I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	40	I	CLK for OTP memory address increment.
IO0~IO6	27~33	I/O	7-bit Data Bus pins.
C0~C2	27~29	I	Mode code input pins. They are the secondary function of IO0~IO2.
BS	36	COL	High/Low byte selected pin. High byte (6-bit) is selected when BS is high
1	W.100	COM.	Low byte (7-bit) is selected when BS is low.
/PGM	14	I	Program write enable. Active low.
/OE	13	Y Y	Output enable. Active low.

6. EM78P458-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp 12 I		I I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	10	110	CLK for OTP memory address increment.
DATAIN	8	I/O	ROM code series input and series output pin.
DINCK	9	I	ROM code series input and output clock.
/PGMB	11	I	Program write enable. Active low.
/OEB	OEB 13 I		Output enable. Active low.

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VI. Function Description

VI.1 OTP ROM

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The OTP ROM is consisted of two parts, Program ROM and Option ROM. The width of each part is 13 bits that are accessible to program in normal mode and in option. The address and data lines of OTP ROM, for instance, EM78P156E, are listed below:

- * ADDR[1:9]: input, address lines for ROM
- * DATAR [0:12]: input/output, data lines for ROM

VI.2 Table of Operation Mode

MODE	C2(DATAIN)	C1(ACLK)	C0(DINCK)
REGULAR	0	0 1	0
OPTION	0	111	0
SECURITY	1	0	

VI.3 Description of Operation Modes

1. Regular Mode

This mode is provided to program and verify the regular OTP EPROM memory only. This mode is defined as default. OTP memory can be read during the read operation.

2. OPTION Mode (Configuration Register)

This mode provides a user a special mode for selecting type of oscillator, instruction cycle, or others.

3. Security Mode (Security Register)

This mode is particularly provided to protest the programmed code from external access. The default state has no protection. Once this security is programmed, the data path from OTP memory is disabled from any external pins. It still allows the internal access from on-chip microcontroller. Note that the programming of this security bit should be arranged at very last step.

VI.4 Registers of Operation Mode

1. EM78P152/3

The EM78P152/3 has one CODE option word which is not a part of the normal program memory. The option bits can not be accessed during normal program execution.

12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	/ENWDT	CLK	OSC1	OCS2	CS	SUT1	SUT0	TYPE	RCOUT	C2	C1	C0

Bit 12 (/RESET): Define pin4 as a reset pin.

0: /RESET enable

1: /RESET disable

Bit 11 (/ENWTDB): Watchdog Timer enabled.

0: Enable

1: Disable



Bit 10 (CLK): Instruction period option bit.

0: two oscillator periods

1: four oscillator periods

Refer to the section of Instruction Set.

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Bit 9 and Bit 8 (OSC1 and OSC2): Oscillator Modes Selection bits.

Table 1 Oscillator Modes defined by OSC1 and OSC2

Mode	OSC1	OSC2
IRC(Internal RC oscillator mode)	11	1
ERC(External RC oscillator mode)	1	0
HXT(High XTAL oscillator mode)	0	× 1100 1
LXT(Low XTAL oscillator mode)	0	0

<Note> The transient point of system frequency between HXT and LXY is around 400 KHz.

Bit 7(CS): Code Security Bit

0: Security Off

Bit 6 and Bit 5 (SUT1 and SUT0): Set-up Time of device bits.

Table 2 Set-up Time of device programming

SUT1	SUT0	*Set-up Time
1	1	18 ms
1	0	36 ms
0	1	4.5 ms
0	0	72 ms

^{*}The theoretical values are for reference only

Bit 4(Type): Type selection for EM78P152 or EM78P153.

TYPE	Series
0	EM78P153
1	EM78P152

Bit 3(RCOUT): A selecting bit of High or Low frequency for internal RC Oscillator.

RCOUT	Pin Function
0	P64
1	OSCO

Bit 2, Bit 1, and Bit 0 (CAL2, CAL1, CAL 0): Calibrator of internal RC mode bits



Table 3 Calibration Selection for Internal RC N

C2	C1	C0	*Cycle Time (ns)	*Frequency (MHz)
1	1	1	248.5	4.02
0	0	0	236	4.24
1	0	0	223	4.48
0	-1	0	211.4	4.73
1	1	0	199.1	5.02
0	1	1	260.8	3.83
1	0	1	273	3.66
0	0	₇ 1	285.3	3.51

2. EM78P156E

The EM78P156E has one CODE option word which is not a part of the normal program memory. The option bits can not be accessed during normal program execution.

12	11	10	9	8	7.0	6	5~0
MS	HLF	HLP	ENWDTB1	CLKS	IRCEN	PTB	

Bit 12 (MS): Oscillator type selection

0: RC type

1: XTAL type

Bit 11 (HLF): XTAL frequency selection

0: Low frequency (32.768KHz)

1: High frequency

This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0".

Bit 10 (HLP): Power consumption selection

0: Low power

1: High power

Bit 9 (ENWDTB1): Watchdog Timer enabled

0: Enable

1: Disable

Bit 8 (CLKS): Clocks of each instruction cycle

0: Two clocks

1: Four clocks

Bit 7 (IRCEN): RC Oscillator Selection

0: Internal RC

1: External RC

Bit 6 (PTB): Protect bit

0: Protect enabled

1: Protect disabled

^{* 1.} The theoretical values, an instance of the high frequency mode, are for reference only

^{* 2.} The similar ways are also for the low frequency mode.



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Bits 5~0: Not used. (default "000000b")

3. EM78P447A/B

In the option mode, the data are accessed through P60~P66, that is the data are located in OTP ROM. The data written into OTP ROM in Option mode are loaded into Configuration register after power-on reset. In the test mode, the 6 option bits of Configuration register can also be read by ALU through data bus DBUS[0..5] and its address is 0E (Register RE).

12	11	10	9	8	7	6	5	4~0
MS	ENWDTB	CLKS	/PT	HLF	HLP	TYP	reserved	VV

Bit 12 (MS): Oscillator type selection

0: RC type

1: XTAL type

Bit 11 (ENWDTB): Watchdog Timer enabled

0: Enable

1: Disable

Bit 10 (CLKS): Clocks of each instruction cycle

0: Two clocks

1: Four clocks

Bit 9 (/PT): Protect bit

0: Protect enabled

1: Protect disabled

Bit 8 (HLF): XTAL frequency selection

0: Low frequency (32.768KHz)

1: High frequency

This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0".

Bit 7 (HLP): Power consumption selection

0: Low power

1: High power

Bits 6 (TYP): EM78447A/B selection

0: EM78P447B

1: EM78P447A

Bit5~0: Not used. (default "000000b")

4. EM78P447SA/SB

The EM78P447S has one CODE option word which is not a part of the normal program memory. The option bits can not be accessed during normal program execution.

12	11	10	9	8	7	6	5	4	3~0
MS	ENWDTB	CLKS	/PT	HLF	HLP	TYP	EN_447	EMI_EN	ID[3~0]

Bit 12 (MS): Oscillator type selection

0: RC type

1: XTAL type

* This specification is subject to be changed without notice. 1.26.1999

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Bit 11 (ENWDTB): Watchdog Timer enabled

0: Enable

1: Disable

Bit 10 (CLKS): Clocks of each instruction cycle

0: Two clocks

1: Four clocks

Bit 9 (/PT): Protect bit

0: Protect enabled

1: Protect disabled

Bit 8 (HLF): XTAL frequency selection

0: Low frequency (32.768KHz)

1: High frequency

This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0".

Bit 7 (HLP): Power consumption selection

0: Low power

1: High power

Bits 6 (TYP): EM78447SA/SB selection

0: EM78P447SB

1: EM78P447SA

Bit5 (EN 447): Selection wake-up function

- 0: Any one of pins from P60 to P67, and both of P74 and P75 can be defined to have the function of waking up from SLEEP.
- 1: All the pins of P60~P67, P74 and P75 can be defined to be equipped with the function of waking up from SLEEP.

Bit3~0: Code for user ID use.

5. EM78P451

Sequence of bits for option mode is as follows:

Address	12	11	10	9	8	7	6	5	4	3	2	1	0
FFF	MS	ENWDTB	CLKS	PTB	HLF	RCT	HLP	DELI	DELO	ID[3]	ID[2]	ID[1]	ID[0]

Bit 12 (MS): Oscillator type selection

0: RC type

1: XTAL type

Bit 11 (ENWDTB): Watchdog Timer enabled

0: Enable

1: Disable

Bit 10 (CLKS): Clocks of each instruction cycle

0: Two clocks

1: Four clocks

Bit 9 (PTB): Protect bit

0: Protect enabled

1: Protect disabled

Bit 8 (HLF): XTAL frequency selection

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0: Low frequency (32.768KHz)

1: High frequency

This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0"

Bit 7 (RCT) Resistor Capacitor

0: internal RC

1: external RC

Bit 6 (HLP): Power consumption selection

0: Low power

1: High power

Bit 5 ~ Bit 4 : DEL1 and DEL0 input delay time options.

DEL 1	DEL 0	Delay time
1	1	0 ns
0		50 ns
-11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0	100ns

Bit $3 \sim \text{Bit } 0 : \text{ID}[3] \sim \text{ID}[0] \text{ ID code.}$

6. EM78P458

ſ	Address	12	111	10	9	8	7	6	5	4	3	2	1	0
	000	MS	ENWDTB	CLKS	PTB	HLF	RCT	HLP	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]

Bit 12 (MS): Oscillator type selection

0: RC type

1: XTAL type

Bit 11 (ENWDTB): Watchdog Timer enabled

0: Enable

1: Disable

Bit 10 (CLKS): Clocks of each instruction cycle

0: Two clocks

1: Four clocks

Bit 9 (PTB): Protect bit

0: Protect enabled

1: Protect disabled

Bit 8 (HLF): XTAL frequency selection

0: Low frequency (32.768KHz)

1: High frequency

This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0".

Bit 7 (RCT) Resistor Capacitor

0: internal RC

1: external RC

Bit 6 (HLP): Power consumption selection

0: Low power

1: High power

Bit $5 \sim Bit\ 0 : ID[5] \sim ID[0]\ ID\ code$.



Address	12	11	10	9	8	7	6	5	4~0
001	SIGN2	VOF2[2]	VOF2[1]	VOF2[0]	SIGN1	VOF1[2]	VOF1[1]	VOF1[0]	TALL

Bit 12: SIGN2

1 : Positive voltage

0: Negative voltage

Bit 11 ~ Bit 9 : VOF2[2] ~ VOF2[0]

Bit 8: SIGN1

1 : Positive voltage

0 : Negative voltage

Bit 7 ~ Bit 5 : VOF1[2] ~ VOF1[0]

VII. Absolute Maximum Ratings

Items	Sym.	Condition	Rating
Temperature under bias	T_{OPR}	MINIM.	0°C to 70°C
Storage temperature	T _{STR}	100 x 0.W.1	-65°C to 150°C
Input voltage	V _{IN}	MW 41 ON CO	-0.3V to +6.0V
Output voltage	V _o	M.Ing. COM.	-0.3V to +6.0V

VIII. DC Electrical Characteristic (EM78P156E for Reference) (Ta=0°C~70°C, VDD=5.0V±5%, VSS=0V)

Sym.	Parameter	Condition	Min.	Тур.	Max.	Unit
Vpp	Programming voltage	Vpp pin active	10.5	-7	12.5	V
IIL1	Input Leakage Current for input pins	VIN=VDD,VSS			±1	μΑ
IIL2	Input Leakage Current for	VIN=VDD,VSS	O_{Mr}	-1	±1	μΑ
	bidirectional pins	1 1 100%		TW		
VIH	Input High Voltage	Ports5,6	2.0			V
VIL	Input Low Voltage	Port 5,6		1.7	0.8	V
VIHT	Input High Threshold Voltage	/RESET, TCC	2.0		N	V
VILT	Input Low Threshold Voltage	/RESET, TCC	46	11.	0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5) -		V
VILX	Clock Input Low Voltage	OSCI	3		1.5	V
VOH1	Output High Voltage	Ports 5,6 (IOH=-12.0 mA)	2.4			V
VOL1	Output Low Voltage	P50~P53, P60~P63, P66~P67			0.4	V
	MM, 100X.C	(IOL=12.0 mA)				
VOL2	Output Low Voltage	P64~P65 (IOL=16.0 mA)			0.4	V
IPH	Pull-high current	Pull-high active input pin at VSS	-50	-100	-240	μΑ
IPD	Pull-down current	Pull-down active, input pin at VDD	25	50	120	μΑ
ISB	Power-down current (VDD=3V)	All input and I/O pins at VDD,				
		output pin floating, WDT enabled			3	μΑ
ICC	Operating supply current	/RESET='High', Fosc=4MHz				
	(VDD=5V)	(Crystal type, CLKS='0') output				
	at two cycles/two clocks	pin floating			2	mA
ICCL	Low frequency operating supply	/RESET='High', Fosc=32KHz				
	current (VDD=3V)	(Crystal type, CLKS='0') output				
	at two cycles/two clocks	pin floating, WDT disabled		15	30	μΑ

^{*} This specification is subject to be changed without notice. 1.26.1999



PROGRAM TIMING

IX. Voltage Detector Electrical Characteristic (Ta=25°C)

Sym.	Parameter	Condition	Min.	Тур.	Max.	Unit
Vdet	Detect voltage	-1001. W.I.	2.0	2.2	2.4	V
Vrel	Release voltage	MAN COPY	N .	Vdet x 1.05	anv.	V
Iss	Current consumption	VDD=5V		-131	20	μΑ
Vop	Operating voltage	W. Co.	0.7*	41/1/	5.5	V
ΔVdet/	Temperature	0°C≤ Ta≤70°C		-111	-2	MV/°C
ΔTa	Characteristic of Vdet	NA CONTRACT		MAN.	- 100	Y.C

^{*} When the voltage of VDD rises between Vop=0.7V and Vdet, the output of voltage detector must be "low".

X. AC Electrical Characteristic (EM78P156E for Reference)

 $(Ta=0^{\circ}C \sim 70^{\circ}C, VDD=5.0V\pm5\%, VSS=0V)$

Sym.	Parameter	Condition	Min.	Тур.	Max.	Unit
Dclk	Input clock duty cycle	MANN.	45	50	55	%
44	TinsInstruction time (CLKS='0')	Crystal type	125		DC	ns
	TW.	RC type	500		DC	ns
Tdr	Device reset hold time	Ta=25°C	- N	18	-TIN	ms
Twdt	Watchdog Timer period	Ta=25°C	I. A.	18	4	ms

XI. Switching Programming AC Electrical Characteristic

Symbol	Parameter	Min.	Max.	Unit
Trs	Vpp to VDD level setup time	2	Mr.	μs
Tcsu	Mode code setup time	1002	W.TW	μs
Tchd	Mode code hold time	2	WIT	μs
Tdsu	Mode hold time	2	\sim $O_{M^{**}}$	μs
Tdhd	Data hold time	2	TILL	μs
Tip	Program enable setup time	4	COB	μs
Tdb	Data to byte select change	20	COM.	ns
Tpwd	Program pulse width	100	1.00	μs
Toes	Output enable setup time	2	- 41 COMP	μs
Tod	Data select change from output enable	20	0 x.	ns
Thz	Output disable to data in High-Z	W. W.	100	ns
Tph	Address clock pulse width	25		ns
Tso	Data(byte) select to output delay time		200	ns
Tsh	Data(byte) select to output change	50		ns
Toda	Output disable to ACLK setup time	2		μs
Tadb	ACLK to data(byte) select delay time	2		μs
Tsa	Data(byte) select to ACLK setup time	2		μs

Note:

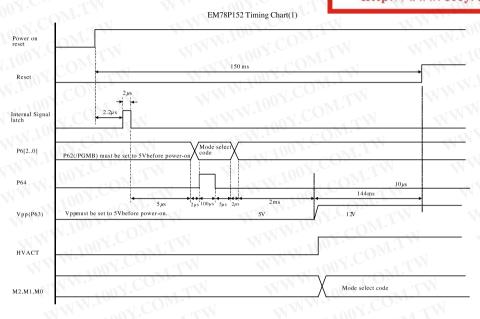
- 1. VDD must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. A separate capacitor of 0.1 µF should be connected to Vpp and VDD to avoid any overshoot and power line noise.
- 2. All timing reference voltage levels are 0.9 of 6V or 12.5V for high level and 0.1 of 6V or 12.5V for low level respectively.
- 3. Tpwd 100µs is the programming pulse.
- 4. Vpp voltage can be varied from 10.5V to 12.5V.

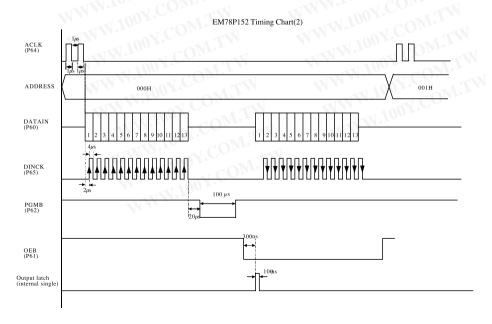


XII. Timing Diagrams

1. EM78P152/3 Timing Chart

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw



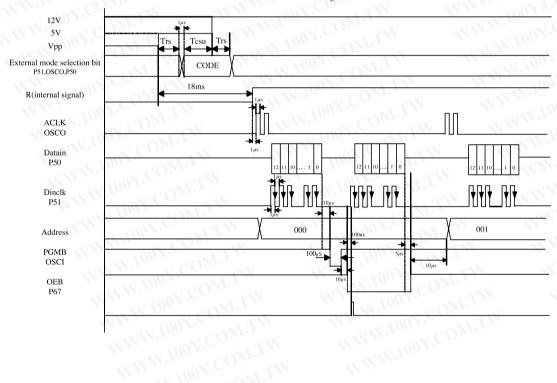




2. EM78P156E Timing Chart

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

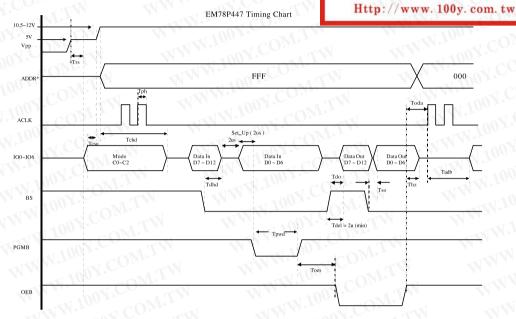
EM78P156E Timing Chart



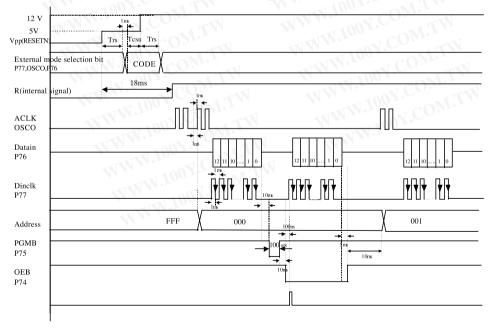
PROGRAM TIMING

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4. EM78P447 A/B & EM78P447S Timing Chart



EM78P447S Timing Chart



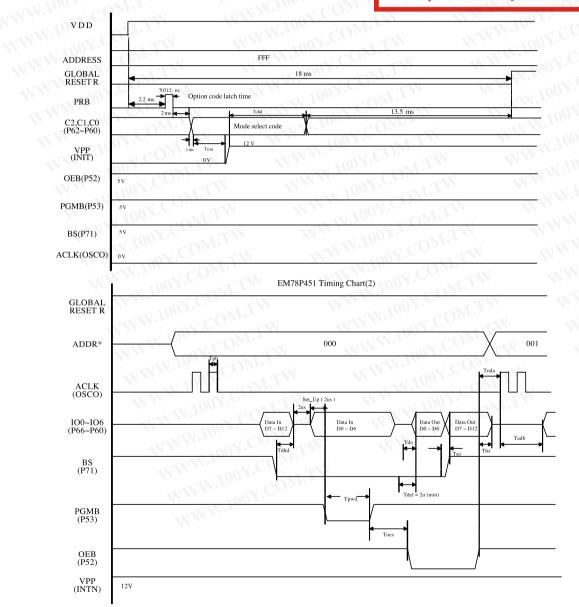


5. EM78P451 Timing Chart

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EM78P451 Timing Chart(1)

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PROGRAM TIMING

6. EM78P458 Timing Chart

EM78P458 Timing Chart(1)

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