I. General Description

The EM78PXXX is a series of 8-bit microcontrollers with low-power and high-speed CMOS technology. They are equipped with Electrical One Time Programmable Read Only Memory (OTP-ROM). The OTP memory provides not only the security bit to protect the memory itself from intruding, but also the option bits to meet users' requirements.

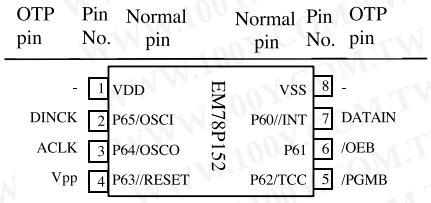
The OTP EPROM is embedded inside EM78PXXX 8-bit microcontrollers instead of the mask memory. Users' developed programs can be easily programmed into or verify from this OTP memory by using EMC EPROM Writer.

II. Feature

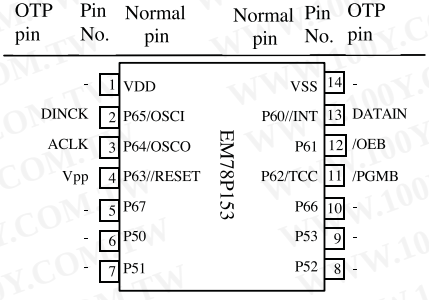
- ✧ Available in temperature range: 0°~70°C (commercial), or
  -40°~85°C(industrial).
- ✧ Optional instruction cycle periods:
  * Two oscillator clocks, or
  * Four oscillator clocks.
- ✧ Low power consumption:
  * < 2mA, at 5V / 4MHz, or
  * 15mA typical, at 3V / 32KHz.
- ✧ One Security Register is provided to protect the OTP memory code.
- ✧ One Configuration Register is provided to meet the user's options.
- ✧ 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges, and with overflow interrupt.
- ✧ Programmable free running on-chip watchdog timer.
- ✧ Power-down mode.
- ✧ Input port changed interrupt (wake-up), and external interrupt available.
- ✧ 99.9% signal instruction cycle commands.
- ✧ Power on voltage detector.

III. Pin Configurations

1. Pin Assignments of EM78P152 and EM78P153

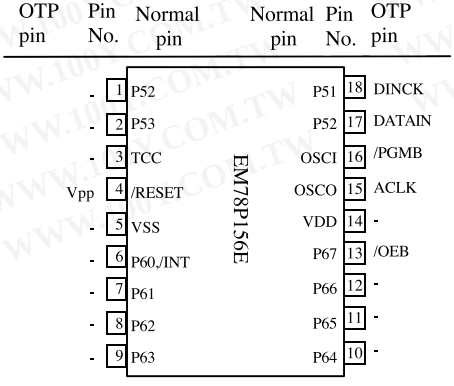


Pin assignment of EM78P152



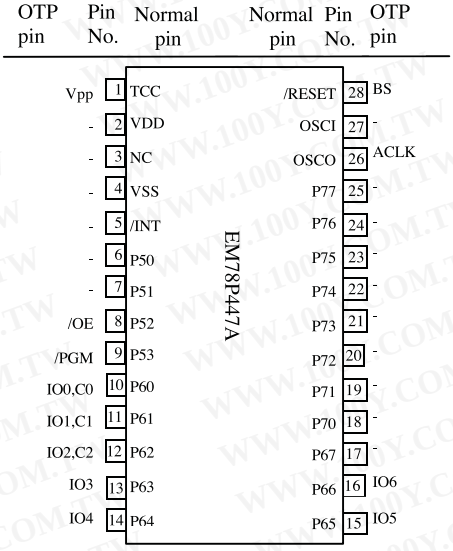
Pin assignment of EM78P153

2. Pin Assignment of EM78P156E

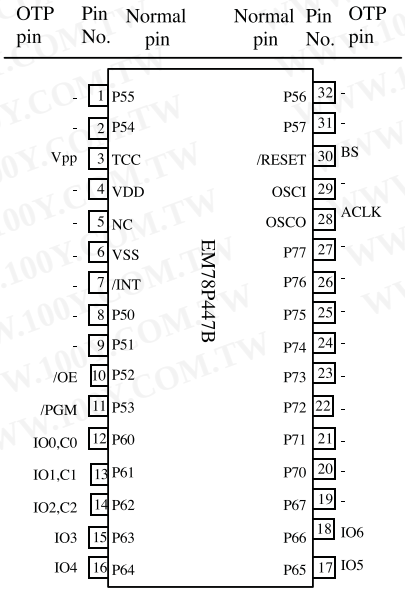


Pin assignment of EM78P156E

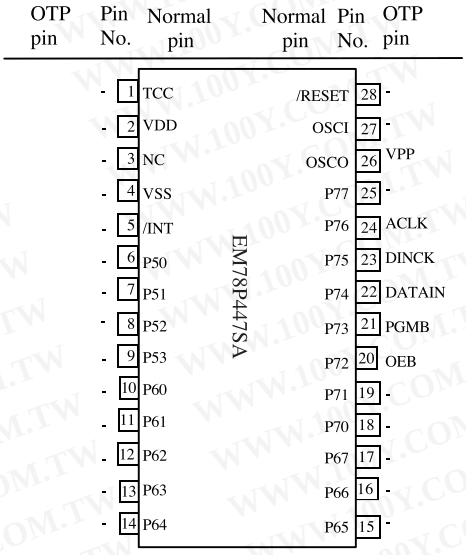
3. Pin Assignments of EM78P447A, EM78P447B, EM78P447SA and EM78P447SB



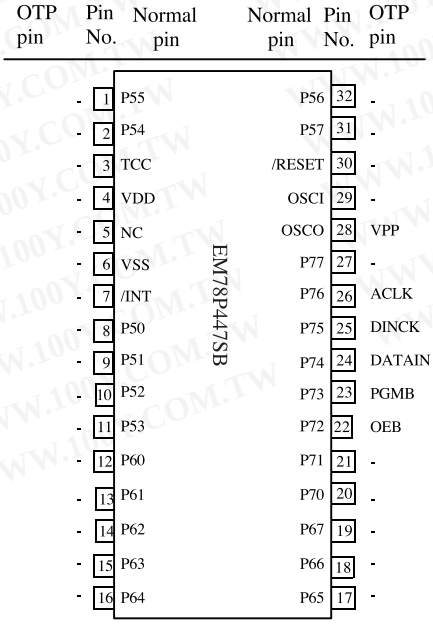
Pin assignment of EM78P447A



Pin assignment of EM78P447B

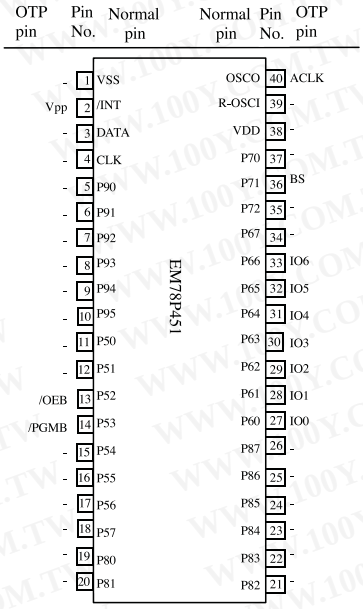


Pin assignment of EM78P447SA



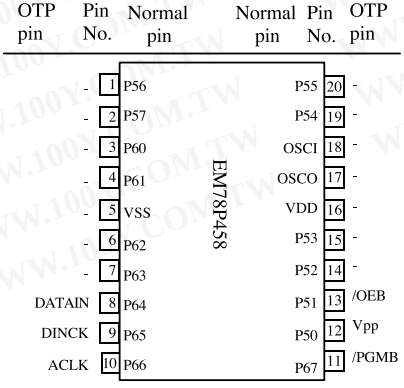
Pin assignment of EM78P447SB

4. Pin Assignment of EM78P451



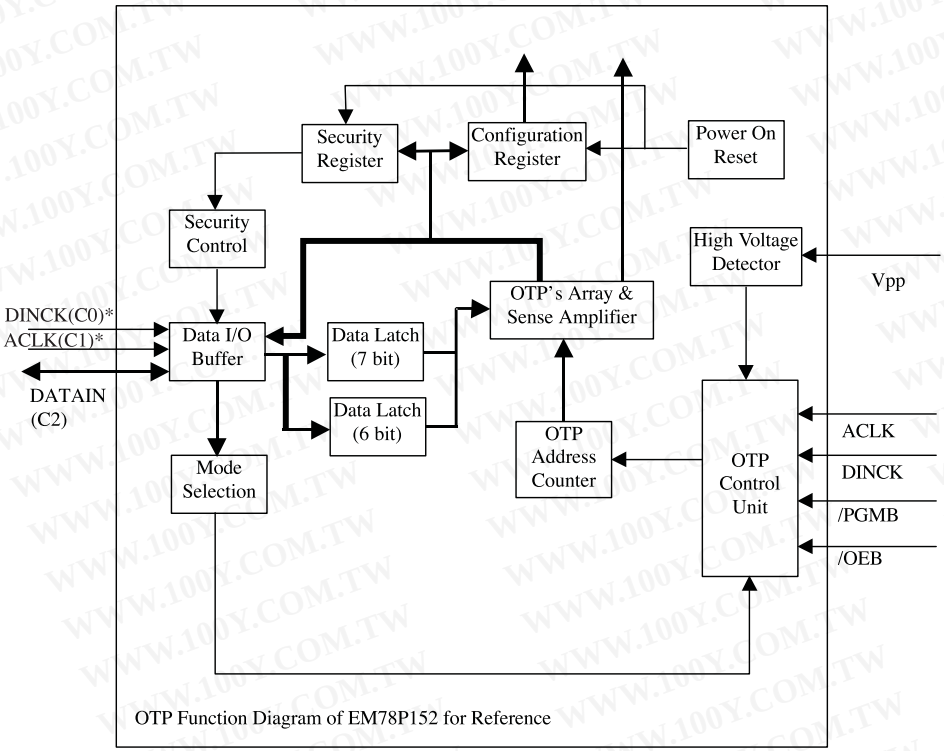
Pin assignment of EM78P451

5. Pin Assignment of EM78P458

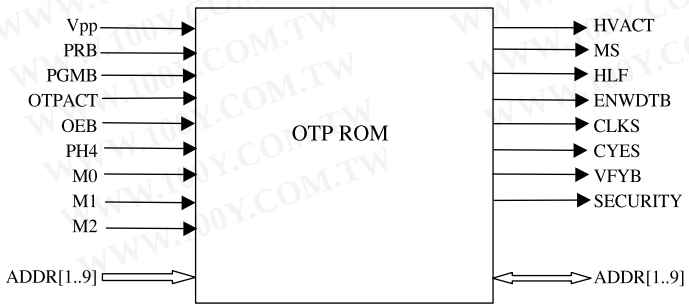


Pin assignment of EM78P458

IV. Functional Block Diagram



OTP Function Diagram of EM78P152 for Reference



OTP ROM input/output signals

V. Pin Descriptions

1. EM78P152/3-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp	4	I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	3	I	CLK for OTP memory address increment.
DATAIN	7/13	I/O	ROM code series input and series output pin.
DINCK	2	I	ROM code series input and output clock.
/PGMB	5/11	I	Program write enable. Active low.
/OEB	6/12	I	Output enable. Active low.

2. EM78P156E-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp	4	I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	15	I	CLK for OTP memory address increment.
DATAIN	17	I/O	ROM code series input and series output pin.
DINCK	18	I	ROM code series input and output clock.
/PGMB	16	I	Program write enable. Active low.
/OEB	13	I	Output enable. Active low.

3. EM78P447 A/B-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp	1	I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	26	I	CLK for OTP memory address increment.
IO0~IO6	10~16	I/O	7-bit Data Bus pins.
C0~C2	10~12	I	Mode code input pins. They are the secondary function of IO0~IO2.
BS	28	I	High/Low byte selected pin. High byte (6-bit) is selected when BS is high. Low byte (7-bit) is selected when BS is low.
/PGM	9	I	Program write enable. Active low.
/OE	8	I	Output enable. Active low.

4. EM78P447SA/SB-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp	28/30	I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	28/26	I	CLK for OTP memory address increment.
DATAIN	26/24	I/O	ROM code series input and series output pin.
DINCK	27/25	I	ROM code series input and output clock.
/PGMB	25/23	I	Program write enable. Active low.
/OEB	24/22	I	Output enable. Active low.

5. EM78P451-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp	2	I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	40	I	CLK for OTP memory address increment.
IO0~IO6	27~33	I/O	7-bit Data Bus pins.
C0~C2	27~29	I	Mode code input pins. They are the secondary function of IO0~IO2.
BS	36	I	High/Low byte selected pin. High byte (6-bit) is selected when BS is high. Low byte (7-bit) is selected when BS is low.
/PGM	14	I	Program write enable. Active low.
/OE	13	I	Output enable. Active low.

6. EM78P458-OTP Pin Descriptions

Symbol	Pin No.	Type	Function
Vpp	12	I	Programming voltage input. Vpp can be varied from 10.5 to 12.5V
ACLK	10	I	CLK for OTP memory address increment.
DATAIN	8	I/O	ROM code series input and series output pin.
DINCK	9	I	ROM code series input and output clock.
/PGMB	11	I	Program write enable. Active low.
/OEB	13	I	Output enable. Active low.

VI. Function Description

VI.1 OTP ROM

The OTP ROM is consisted of two parts, Program ROM and Option ROM. The width of each part is 13 bits that are accessible to program in normal mode and in option. The address and data lines of OTP ROM, for instance, EM78P156E, are listed below:

* ADDR[1:9]: input, address lines for ROM
* DATAR [0:12]: input/output, data lines for ROM

VI.2 Table of Operation Mode

MODE	C2(DATAIN)	C1(ACLK)	C0(DINCK)
REGULAR	0	0	0
OPTION	0	1	0
SECURITY	1	0	1

VI.3 Description of Operation Modes

1. Regular Mode
   This mode is provided to program and verify the regular OTP EPROM memory only. This mode is defined as default. OTP memory can be read during the read operation.

2. OPTION Mode (Configuration Register)
   This mode provides a user a special mode for selecting type of oscillator, instruction cycle, or others.

3. Security Mode (Security Register)
   This mode is particularly provided to protest the programmed code from external access. The default state has no protection. Once this security is programmed, the data path from OTP memory is disabled from any external pins. It still allows the internal access from on-chip microcontroller. Note that the programming of this security bit should be arranged at very last step.

VI.4 Registers of Operation Mode

1. EM78P152/3

The EM78P152/3 has one CODE option word which is not a part of the normal program memory. The option bits can not be accessed during normal program execution.

12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	/ENWDT	CLK	OSC1	OCS2	CS	SUT1	SUT0	TYPE	RCOUT	C2	C1	C0

Bit 12 (/RESET): Define pin4 as a reset pin.
0: /RESET enable
1: /RESET disable

Bit 11 (/ENWTDB): Watchdog Timer enabled.
0: Enable
1: Disable

Bit 10 (CLK): Instruction period option bit.

0: two oscillator periods

1: four oscillator periods

Refer to the section of Instruction Set.

Bit 9 and Bit 8 (OSC1 and OSC2): Oscillator Modes Selection bits.

Table 1 Oscillator Modes defined by OSC1 and OSC2

Mode	OSC1	OSC2
IRC(Internal RC oscillator mode)	1	1
ERC(External RC oscillator mode)	1	0
HXT(High XTAL oscillator mode)	0	1
LXT(Low XTAL oscillator mode)	0	0

<Note> The transient point of system frequency between HXT and LXY is around 400 KHz.

Bit 7(CS): Code Security Bit

0: Security Off

1: Security On

Bit 6 and Bit 5 (SUT1 and SUT0): Set-up Time of device bits.

Table 2 Set-up Time of device programming

SUT1	SUT0	*Set-up Time
1	1	18 ms
1	0	36 ms
0	1	4.5 ms
0	0	72 ms

*The theoretical values are for reference only

Bit 4(Type): Type selection for EM78P152 or EM78P153.

TYPE	Series
0	EM78P153
1	EM78P152

Bit 3(RCOUT): A selecting bit of High or Low frequency for internal RC Oscillator.

RCOUT	Pin Function
0	P64
1	OSCO

Bit 2, Bit 1, and Bit 0 (CAL2, CAL1, CAL 0): Calibrator of internal RC mode bits

Table 3 Calibration Selection for Internal RC Mode

C2	C1	C0	*Cycle Time (ns)	*Frequency (MHz)
1	1	1	248.5	4.02
0	0	0	236	4.24
1	0	0	223	4.48
0	1	0	211.4	4.73
1	1	0	199.1	5.02
0	1	1	260.8	3.83
1	0	1	273	3.66
0	0	1	285.3	3.51

* 1. The theoretical values, an instance of the high frequency mode, are for reference only

* 2. The similar ways are also for the low frequency mode.

2. EM78P156E

The EM78P156E has one CODE option word which is not a part of the normal program memory. The option bits can not be accessed during normal program execution.

12	11	10	9	8	7	6	5~0
MS	HLF	HLP	ENWDTB1	CLKS	IRCEN	PTB	- - - - - -

Bit 12 (MS) : Oscillator type selection
- 0: RC type
- 1: XTAL type

Bit 11 (HLF): XTAL frequency selection
- 0: Low frequency (32.768KHz)
- 1: High frequency
- This bit is useful only when Bit 12 (MS) is “1”. When MS is “0”, HLF must be “0”.

Bit 10 (HLP): Power consumption selection
- 0: Low power
- 1: High power

Bit 9 (ENWDTB1): Watchdog Timer enabled
- 0: Enable
- 1: Disable

Bit 8 (CLKS): Clocks of each instruction cycle
- 0: Two clocks
- 1: Four clocks

Bit 7 (IRCEN): RC Oscillator Selection
- 0: Internal RC
- 1: External RC

Bit 6 (PTB): Protect bit
- 0: Protect enabled
- 1: Protect disabled

Bits 5~0: Not used. (default "000000b")

3. EM78P447A/B

In the option mode, the data are accessed through P60~P66, that is the data are located in OTP ROM. The data written into OTP ROM in Option mode are loaded into Configuration register after power-on reset. In the test mode, the 6 option bits of Configuration register can also be read by ALU through data bus DBUS[0..5] and its address is 0E (Register RE).

12	11	10	9	8	7	6	5	4~0
MS	ENWDTB	CLKS	/PT	HLF	HLP	TYP	reserved	- - - - -

Bit 12 (MS) : Oscillator type selection
0: RC type
1: XTAL type
Bit 11 (ENWDTB): Watchdog Timer enabled
0: Enable
1: Disable
Bit 10 (CLKS): Clocks of each instruction cycle
0: Two clocks
1: Four clocks
Bit 9 (/PT): Protect bit
0: Protect enabled
1: Protect disabled
Bit 8 (HLF): XTAL frequency selection
0: Low frequency (32.768KHz)
1: High frequency
This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0".
Bit 7 (HLP): Power consumption selection
0: Low power
1: High power
Bits 6 (TYP): EM78447A/B selection
0: EM78P447B
1: EM78P447A
Bit5~0: Not used. (default "000000b")

4. EM78P447SA/SB

The EM78P447S has one CODE option word which is not a part of the normal program memory. The option bits can not be accessed during normal program execution.

12	11	10	9	8	7	6	5	4	3~0
MS	ENWDTB	CLKS	/PT	HLF	HLP	TYP	EN_447	EMI_EN	ID[3~0]

Bit 12 (MS) : Oscillator type selection
0: RC type
1: XTAL type

Bit 11 (ENWDTB): Watchdog Timer enabled
- 0: Enable
- 1: Disable

Bit 10 (CLKS): Clocks of each instruction cycle
- 0: Two clocks
- 1: Four clocks

Bit 9 (/PT): Protect bit
- 0: Protect enabled
- 1: Protect disabled

Bit 8 (HLF): XTAL frequency selection
- 0: Low frequency (32.768KHz)
- 1: High frequency

This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0".

Bit 7 (HLP): Power consumption selection
- 0: Low power
- 1: High power

Bits 6 (TYP): EM78447SA/SB selection
- 0: EM78P447SB
- 1: EM78P447SA

Bit5 (EN_447): Selection wake-up function
- 0: Any one of pins from P60 to P67, and both of P74 and P75 can be defined to have the function of waking up from SLEEP.
- 1: All the pins of P60~P67, P74 and P75 can be defined to be equipped with the function of waking up from SLEEP.

Bit3~0: Code for user ID use.

5. EM78P451

Sequence of bits for option mode is as follows:

Address	12	11	10	9	8	7	6	5	4	3	2	1	0
FFF	MS	ENWDTB	CLKS	PTB	HLF	RCT	HLP	DELI	DELO	ID[3]	ID[2]	ID[1]	ID[0]

Bit 12 (MS) : Oscillator type selection
- 0: RC type
- 1: XTAL type

Bit 11 (ENWDTB): Watchdog Timer enabled
- 0: Enable
- 1: Disable

Bit 10 (CLKS): Clocks of each instruction cycle
- 0: Two clocks
- 1: Four clocks

Bit 9 (PTB): Protect bit
- 0: Protect enabled
- 1: Protect disabled

Bit 8 (HLF): XTAL frequency selection

0: Low frequency (32.768KHz)
1: High frequency
This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0".

Bit 7 (RCT) Resistor Capacitor
0: internal RC
1: external RC

Bit 6 (HLP): Power consumption selection
0: Low power
1: High power

Bit 5 ~ Bit 4 : DEL1 and DEL0 input delay time options.

DEL 1	DEL 0	Delay time
1	1	0 ns
0	1	50 ns
1	0	100ns

Bit 3 ~ Bit 0 : ID[3] ~ ID[0] ID code.

6. EM78P458

Address	12	11	10	9	8	7	6	5	4	3	2	1	0
000	MS	ENWDTB	CLKS	PTB	HLF	RCT	HLP	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]

Bit 12 (MS) : Oscillator type selection
0: RC type
1: XTAL type

Bit 11 (ENWDTB): Watchdog Timer enabled
0: Enable
1: Disable

Bit 10 (CLKS): Clocks of each instruction cycle
0: Two clocks
1: Four clocks

Bit 9 (PTB): Protect bit
0: Protect enabled
1: Protect disabled

Bit 8 (HLF): XTAL frequency selection
0: Low frequency (32.768KHz)
1: High frequency
This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0".

Bit 7 (RCT) Resistor Capacitor
0: internal RC
1: external RC

Bit 6 (HLP): Power consumption selection
0: Low power
1: High power

Bit 5 ~ Bit 0 : ID[5] ~ ID[0] ID code.

Address	12	11	10	9	8	7	6	5	4~0
001	SIGN2	VOF2[2]	VOF2[1]	VOF2[0]	SIGN1	VOF1[2]	VOF1[1]	VOF1[0]	-

Bit 12 : SIGN2

1 : Positive voltage

0 : Negative voltage

Bit 11 ~ Bit 9 : VOF2[2] ~ VOF2[0]

Bit 8 : SIGN1

1 : Positive voltage

0 : Negative voltage

Bit 7 ~ Bit 5 : VOF1[2] ~ VOF1[0]

VII. Absolute Maximum Ratings

Items	Sym.	Condition	Rating
Temperature under bias	T_{OPR}		0°C to 70°C
Storage temperature	T_{STR}		-65°C to 150°C
Input voltage	V_{IN}		-0.3V to +6.0V
Output voltage	V_O		-0.3V to +6.0V

VIII. DC Electrical Characteristic (EM78P156E for Reference) (Ta = 0°C ~ 70°C, VDD=5.0V±5%, VSS=0V)

Sym.	Parameter	Condition	Min.	Typ.	Max.	Unit
Vpp	Programming voltage	Vpp pin active	10.5		12.5	V
IIL1	Input Leakage Current for input pins	VIN=VDD,VSS			±1	µA
IIL2	Input Leakage Current for bidirectional pins	VIN=VDD,VSS			±1	µA
VIH	Input High Voltage	Ports5,6	2.0			V
VIL	Input Low Voltage	Port 5,6			0.8	V
VIHT	Input High Threshold Voltage	/RESET, TCC	2.0			V
VILT	Input Low Threshold Voltage	/RESET, TCC			0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5			V
VILX	Clock Input Low Voltage	OSCI			1.5	V
VOH1	Output High Voltage	Ports 5,6 (IOH=-12.0 mA)	2.4			V
VOL1	Output Low Voltage	P50~P53, P60~P63, P66~P67 (IOL=12.0 mA)			0.4	V
VOL2	Output Low Voltage	P64~P65 (IOL=16.0 mA)			0.4	V
IPH	Pull-high current	Pull-high active input pin at VSS	-50	-100	-240	µA
IPD	Pull-down current	Pull-down active, input pin at VDD	25	50	120	µA
ISB	Power-down current (VDD=3V)	All input and I/O pins at VDD, output pin floating , WDT enabled			3	µA
ICC	Operating supply current (VDD=5V) at two cycles/two clocks	/RESET='High', Fosc=4MHz (Crystal type, CLKS='0') output pin floating			2	mA
ICCL	Low frequency operating supply current (VDD=3V) at two cycles/two clocks	/RESET='High', Fosc=32KHz (Crystal type, CLKS='0') output pin floating, WDT disabled		15	30	µA

IX. Voltage Detector Electrical Characteristic (Ta=25°C)

Sym.	Parameter	Condition	Min.	Typ.	Max.	Unit
Vdet	Detect voltage		2.0	2.2	2.4	V
Vrel	Release voltage			Vdet x 1.05		V
Iss	Current consumption	VDD=5V			20	μA
Vop	Operating voltage		0.7*		5.5	V
ΔVdet/ ΔTa	Temperature Characteristic of Vdet	0°C≤ Ta≤70°C			-2	MV/°C

* When the voltage of VDD rises between Vop=0.7V and Vdet, the output of voltage detector must be “low”.

X. AC Electrical Characteristic(EM78P156E for Reference)

(Ta=0°C ~ 70°C, VDD=5.0V±5%, VSS=0V)

Sym.	Parameter	Condition	Min.	Typ.	Max.	Unit
Dclk	Input clock duty cycle		45	50	55	%
	TinsInstruction time (CLKS=’0’)	Crystal type	125		DC	ns
		RC type	500		DC	ns
Tdr	Device reset hold time	Ta=25°C		18		ms
Twdt	Watchdog Timer period	Ta=25°C		18		ms

XI. Switching Programming AC Electrical Characteristic

Symbol	Parameter	Min.	Max.	Unit
Trs	Vpp to VDD level setup time	2		μs
Tcsu	Mode code setup time	2		μs
Tchd	Mode code hold time	2		μs
Tdsu	Mode hold time	2		μs
Tdhd	Data hold time	2		μs
Tip	Program enable setup time	4		μs
Tdb	Data to byte select change	20		ns
Tpwd	Program pulse width	100		μs
Toes	Output enable setup time	2		μs
Tod	Data select change from output enable	20		ns
Thz	Output disable to data in High-Z		100	ns
Tph	Address clock pulse width	25		ns
Tso	Data(byte) select to output delay time		200	ns
Tsh	Data(byte) select to output change	50		ns
Toda	Output disable to ACLK setup time	2		μs
Tadb	ACLK to data(byte) select delay time	2		μs
Tsa	Data(byte) select to ACLK setup time	2		μs

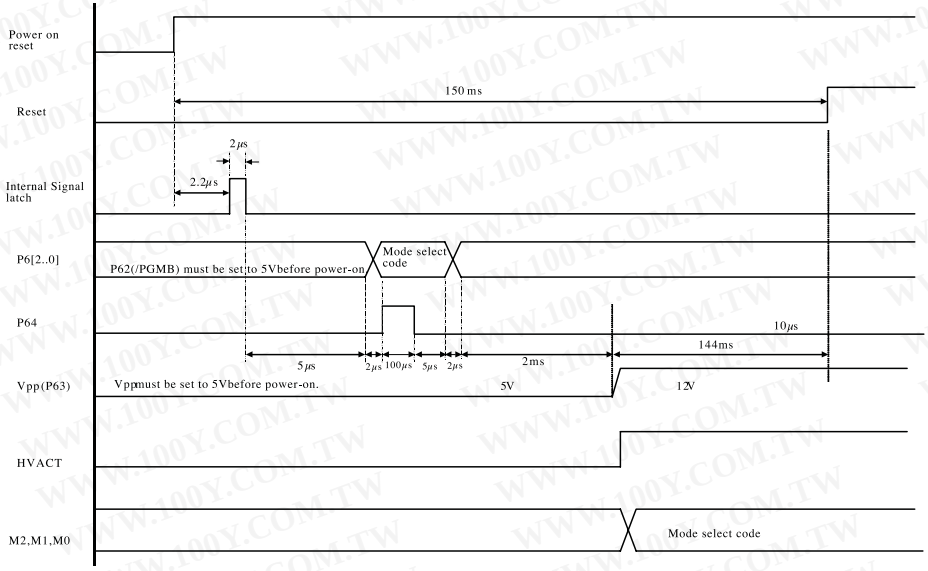
Note:

1. VDD must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. A separate capacitor of 0.1 μF should be connected to Vpp and VDD to avoid any overshoot and power line noise.
2. All timing reference voltage levels are 0.9 of 6V or 12.5V for high level and 0.1 of 6V or 12.5V for low level respectively.
3. Tpwd 100μs is the programming pulse.
4. Vpp voltage can be varied from 10.5V to 12.5V.

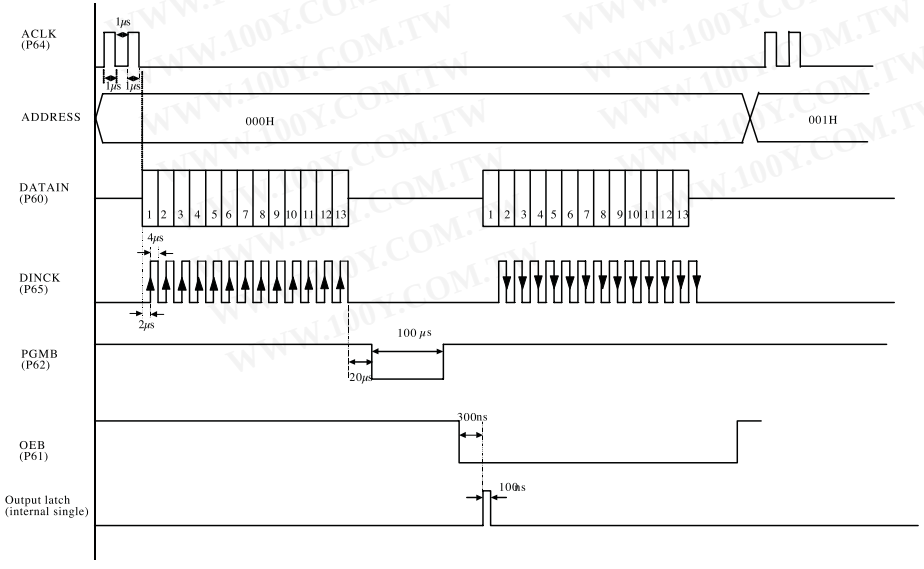
XII. Timing Diagrams

1. EM78P152/3 Timing Chart

EM78P152 Timing Chart(1)

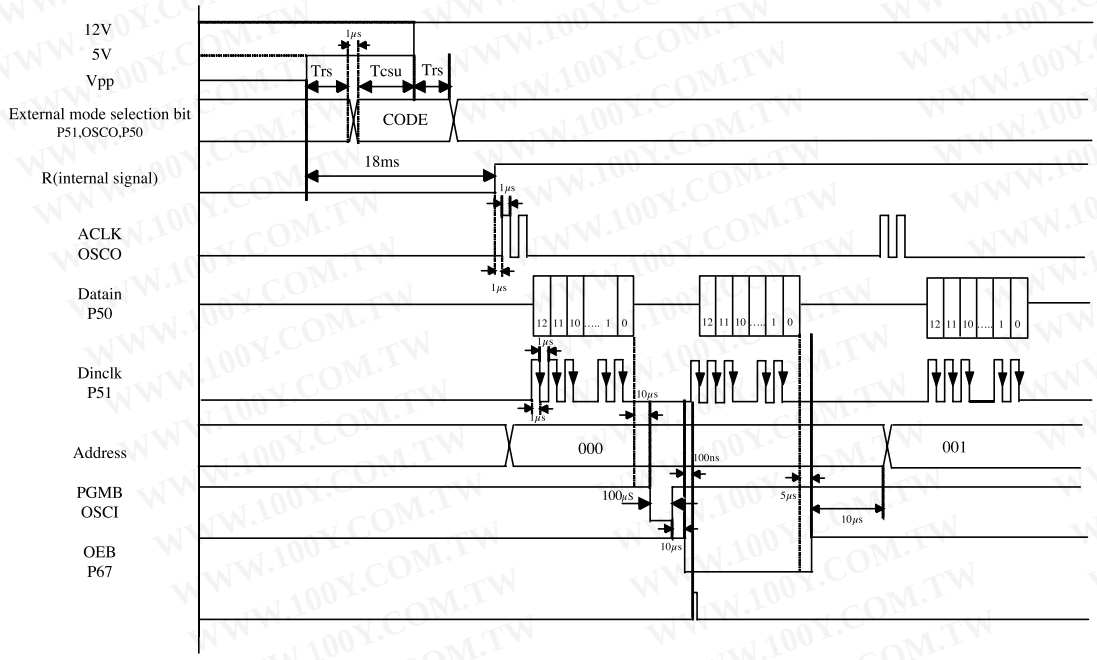


EM78P152 Timing Chart(2)



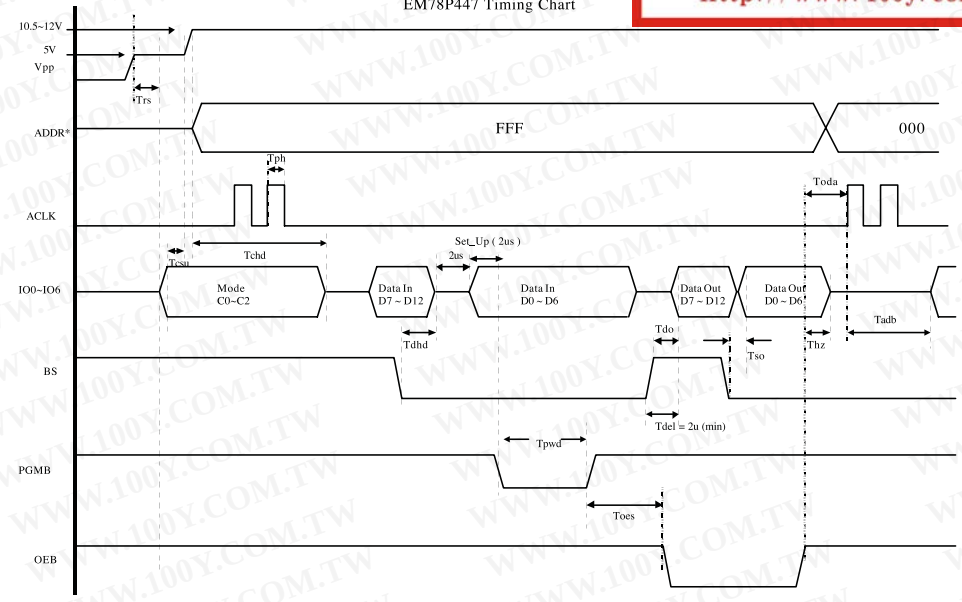
2. EM78P156E Timing Chart

EM78P156E Timing Chart

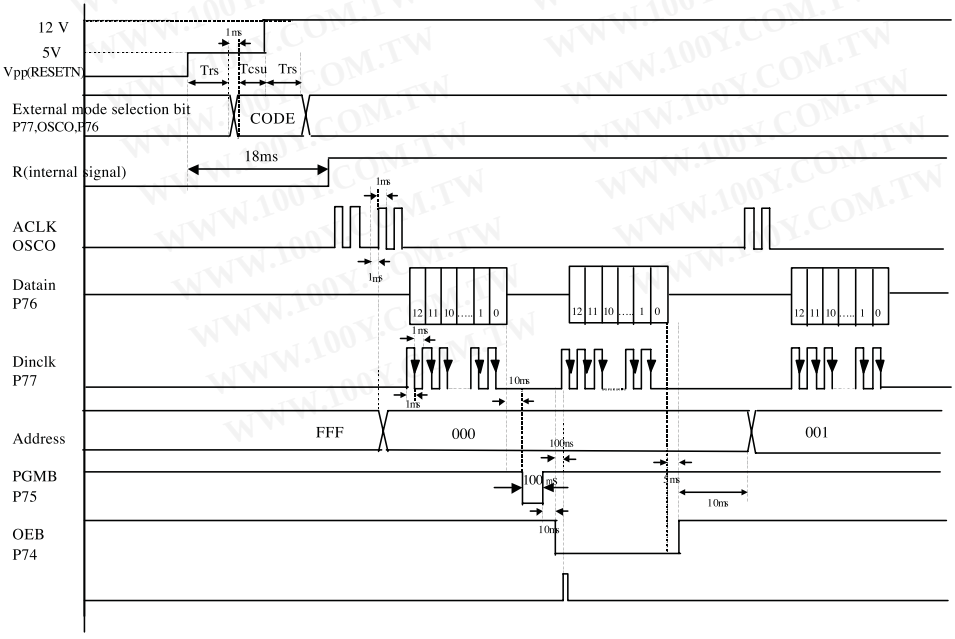


4. EM78P447 A/B & EM78P447S Timing Chart

EM78P447 Timing Chart

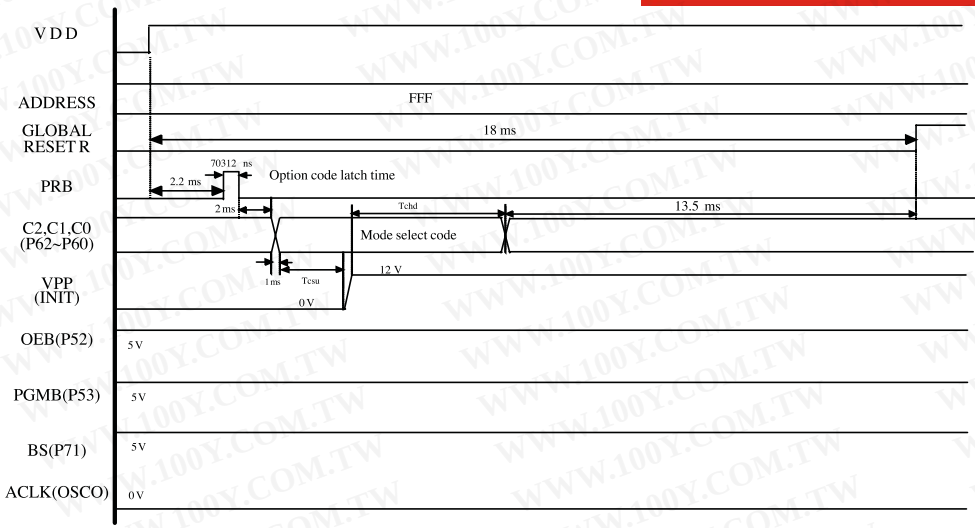


EM78P447S Timing Chart

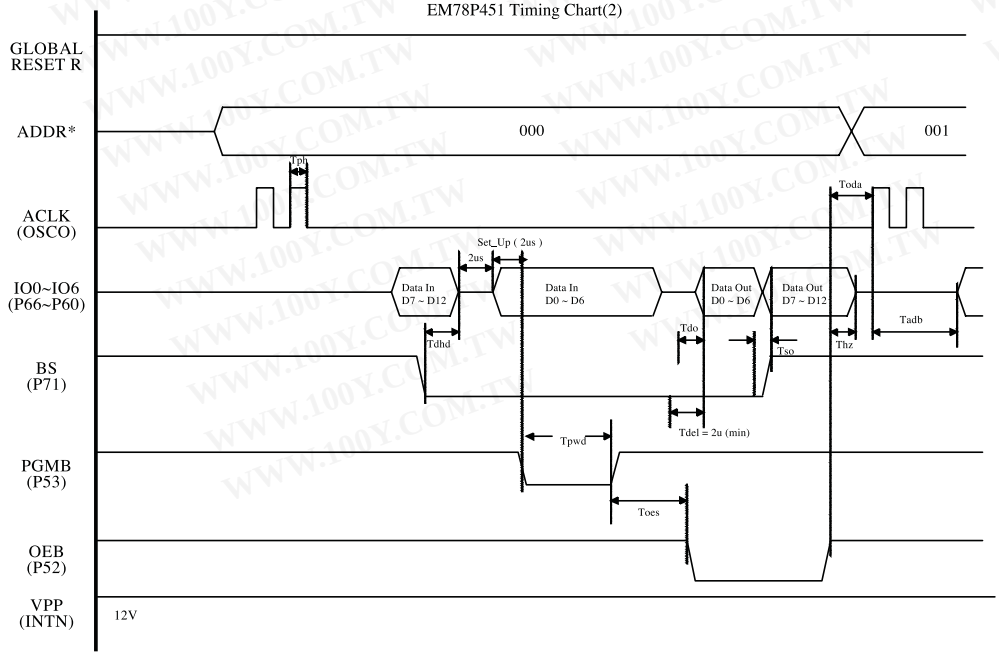


5. EM78P451 Timing Chart

EM78P451 Timing Chart(1)

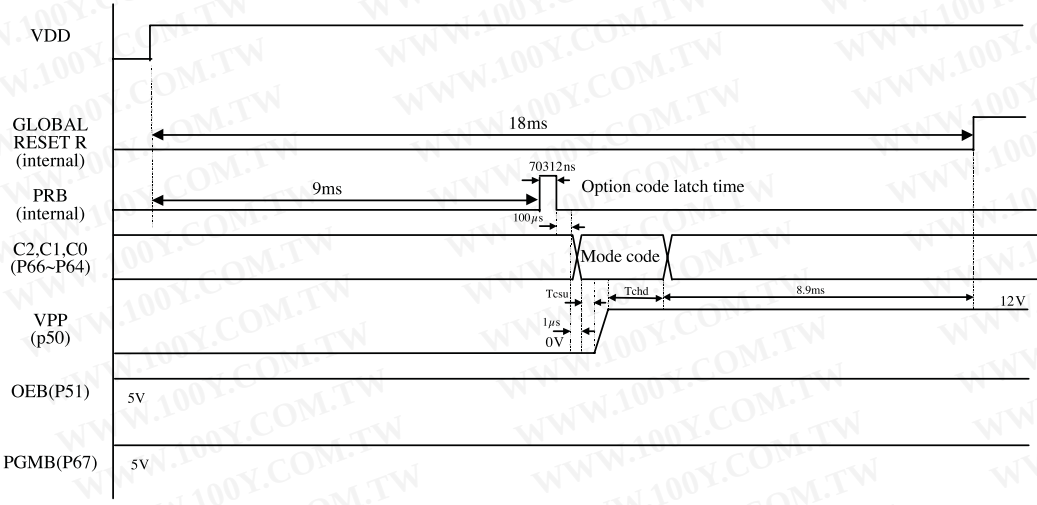


EM78P451 Timing Chart(2)



6. EM78P458 Timing Chart

EM78P458 Timing Chart(1)



EM78P458Timing Chart(2)