élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2075C

2GHz GBWP Gain-of-10 Stable Operational Amplifier

Features

- 2GHz gain-bandwidth product
- Gain-of-10 stable
- Conventional voltage-feedback topology
- Low offset voltage = 200µV
- Low bias current = 2µA
- Low offset current = 0.1µA
- Output current = 50mA over temperature
- Fast settling = 13ns to 0.1%

Applications

- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2075CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2075CS	0°C to +75°C	8-Lead SO	MDP0027

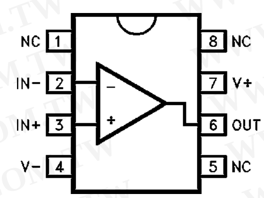
General Description

The EL2075C is a precision voltage-feedback amplifier featuring a 2GHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50mA output current drive over temperature.

The EL2075C is gain-of-10 stable with a -3dB bandwidth of 400MHz at $A_V = +10$. It has a very low 200µV of input offset voltage, only 2µA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2075C allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2075C the ideal choice for all op-amp applications at a gain of 10 or greater requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2075C an ideal amplifier for signal-processing and digitizing systems.

Connection Diagrams

DIP and SO Package



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Absolute Maximum Ratings ($T_A = 25°C$)

Supply Voltage (V_S)	±7V
Output Current Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70mA.	
Common-Mode Input	$\pm V_S$
Differential Input Voltage	5V
Thermal Resistance	θ_{JA} = 95°C/W P-DIP
	θ_{JA} = 175°C/W SO-8
Operating Temperature	0°C to +75°C
Junction Temperature	175°C
Storage Temperature	-60°C to +150°C

Note: See EL2071/EL2171 for Thermal Impedance curves.

Important Note:
All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Unit
V_{OS}	Input Offset Voltage	V_{CM} = 0V	25°C		0.2	1	mV
			T_{MIN}, T_{MAX}			2.5	mV
TCV_{OS}	Average Offset Voltage Drift	[1]	All		8		µV/°C
I_B	Input Bias Current	V_{CM} = 0V	All		2	6	µA
I_{OS}	Input Offset Current	V_{CM} = 0V	25°C		0.1	1	µA
			T_{MIN}, T_{MAX}			2	µA
PSRR	Power Supply Rejection Ratio	[2]	All	70	90		dB
CMRR	Common Mode Rejection Ratio	[3]	All	70	90		dB
I_S	Supply Current—Quiescent	No Load	25°C		21	25	mA
			T_{MIN}, T_{MAX}			25	mA
R_{IN} (diff)	R_{IN} (Differential)	Open-Loop	25°C		15		kΩ
C_{IN} (diff)	C_{IN} (Differential)	Open-Loop	25°C		1		pF
R_{IN} (cm)	R_{IN} (Common-Mode)		25°C		1		MΩ
C_{IN} (cm)	C_{IN} (Common-Mode)		25°C		1		pF
R_{OUT}	Output Resistance		25°C		50		mΩ
CMIR	Common-Mode Input Range		25°C	±3	±3.5		V
			T_{MIN}, T_{MAX}	±2.5			V
I_{OUT}	Output Current		All	50	70		mA
V_{OUT}	Output Voltage Swing	No Load	All	±3.5	±4		V
V_{OUT} 100	Output Voltage Swing	100Ω	All	±3	±3.6		V
V_{OUT} 50	Output Voltage Swing	50Ω	All	±2.5	±3.4		V
A_{VOL} 100	Open-Loop Gain	100Ω	25°C	1000	2800		V/V
			T_{MIN}, T_{MAX}	800			V/V
A_{VOL} 50	Open-Loop Gain	50Ω	25°C	800	2300		V/V
			T_{MIN}, T_{MAX}	600			V/V
eN@ > 1MHz	Noise Voltage 1–100MHz		25°C		2.3		nV/√Hz
iN@ > 100 kHz	Noise Current 100k–100MHz		25°C		3.2		pA/√Hz

1. Measured from T_{MIN}, T_{MAX}.
2. $\pm V_{CC}$ = ±4.5V to 5.5V.
3. $\pm V_{IN}$ = ±2.5V, V_{OUT} = 0V

Closed Loop AC Electrical Characteristics

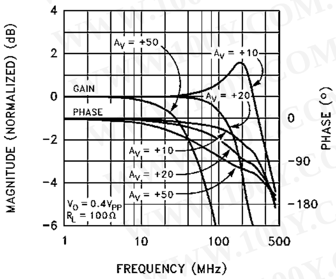
V_S = ±5V, A_V = +20, Rf = 1500Ω, R_L = 100Ω unless otherwise specified.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Unit
SSBW	-3dB Bandwidth (V_{OUT} = 0.4V_{PP})	A_V = +10	25°C		400		MHz
		A_V = +20	25°C	150	200		MHz
			T_{MIN}, T_{MAX}	125			MHz
		A_V = +50	25°C		40		MHz
GBWP	Gain-Bandwidth Product	A_V = +100	25°C		2.0		GHz
LSBWa	-3dB Bandwidth	V_{OUT} = 2V_{PP} [1]	All	80	128		MHz
LSBWb	-3dB Bandwidth	V_{OUT} = 5V_{PP} [1]	All	32	50		MHz
GFPL	Peaking (<50MHz)	V_{OUT} = 0.4V_{PP}	25°C		0	0.5	dB
			T_{MIN}, T_{MAX}			0.5	dB
GFPH	Peaking (>50MHz)	V_{OUT} = 0.4V_{PP}	25°C		0	1	dB
			T_{MIN}, T_{MAX}			1	dB
GFR	Rolloff (<100MHz)	V_{OUT} = 0.4V_{PP}	25°C		0.1	0.5	dB
			T_{MIN}, T_{MAX}			0.5	dB
LPD	Linear Phase Deviation (<100MHz)	V_{OUT} = 0.4V_{PP}	All		1	1.8	°
PM	Phase Margin	A_V = +10	25°C		60		°
tr1, tf1	Rise Time, Fall Time	0.4V Step, A_V = +10	25°C		1.2		ns
tr2, tf2	Rise Time, Fall Time	5V Step, A_V = +10	25°C		6		ns
ts1	Settling to 0.1% (A_V = -20)	2V Step	25°C		13		ns
ts2	Settling to 0.01% (A_V = -20)	2V Step	25°C		25		ns
OS	Overshoot	2V Step, A_V = +10	25°C		10		%
SR	Slew Rate	2V Step, A_V = +10	All	500	800		V/µs
DISTORTION [2]							
HD2	2nd Harmonic Distortion	@ 20MHz, A_V = +20	25°C		-40	-30	dBc
			T_{MIN}, T_{MAX}			-30	dBc
HD3	3rd Harmonic Distortion	@ 20MHz, A_V = +20	25°C		-65	-50	dBc
			T_{MIN}, T_{MAX}			-50	dBc

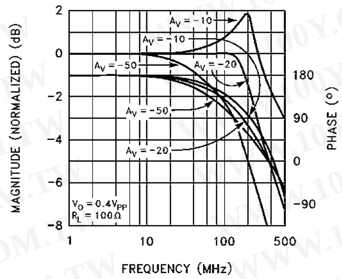
1. Large-signal bandwidth calculated using LSBW = Slew Rate / (2¼ • V_{PEAK}).
2. All distortion measurements are made with V_{OUT} = 2V_{PP}, R_L = 100¾.

Typical Performance Curves

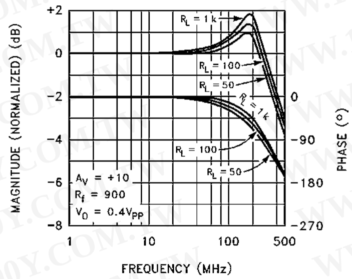
Non-Inverting Frequency Response



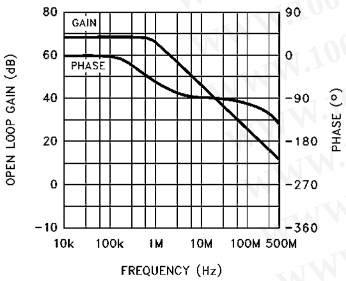
Inverting Frequency Response



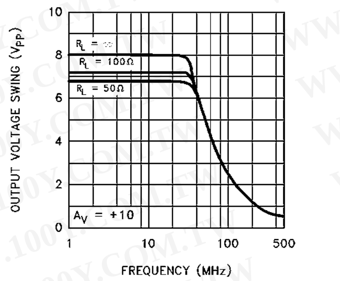
Frequency Response for Various R_Ls



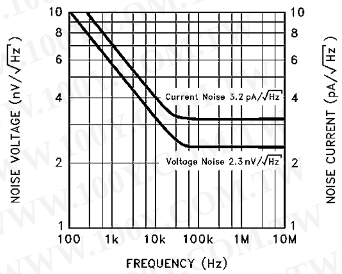
Open Loop Gain and Phase



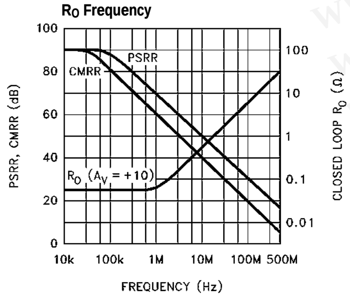
Output Voltage Swing vs Frequency



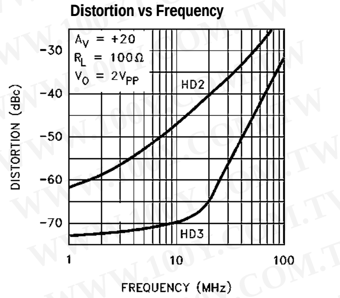
Equivalent Input Noise



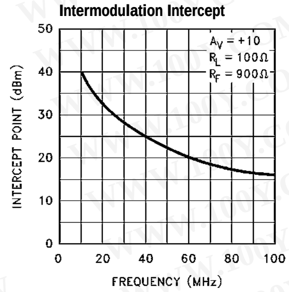
PSRR, CMRR, and Closed-Loop R_O Frequency



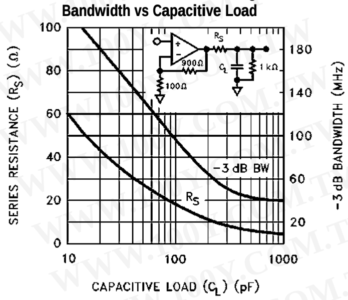
2nd and 3rd Harmonic Distortion vs Frequency



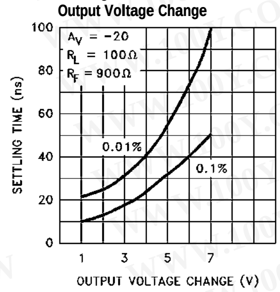
2-Tone, 3rd Order Intermodulation Intercept



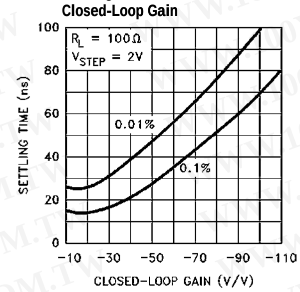
Series Resistor and Resulting Bandwidth vs Capacitive Load



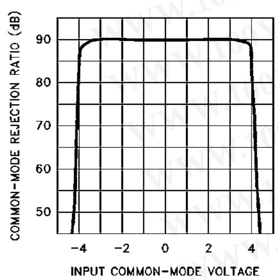
Settling Time vs Output Voltage Change



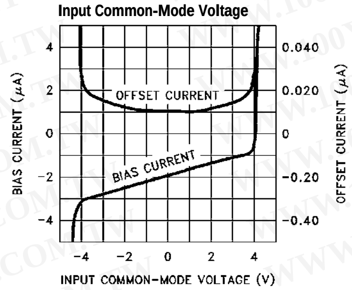
Settling Time vs Closed-Loop Gain



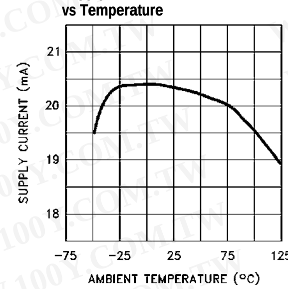
Common-Mode Rejection Ratio vs Input Common-Mode Voltage



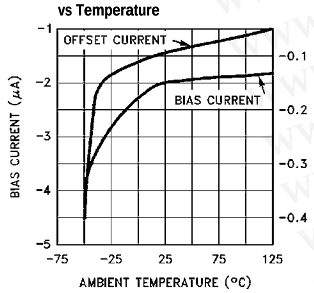
Bias and Offset Current vs Input Common-Mode Voltage



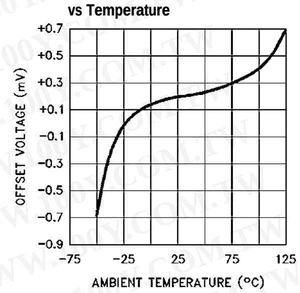
Supply Current vs Temperature



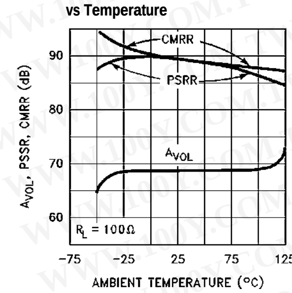
Bias and Offset Current vs Temperature



Offset Voltage vs Temperature



A_{VOL}, PSRR, and CMRR vs Temperature



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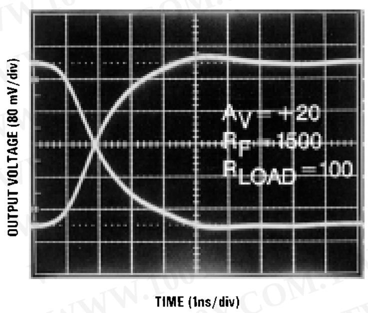
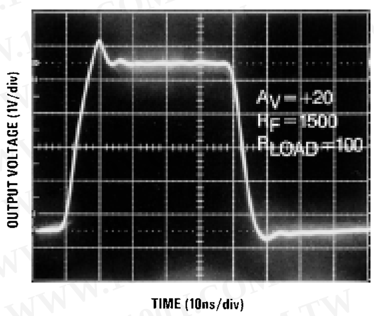
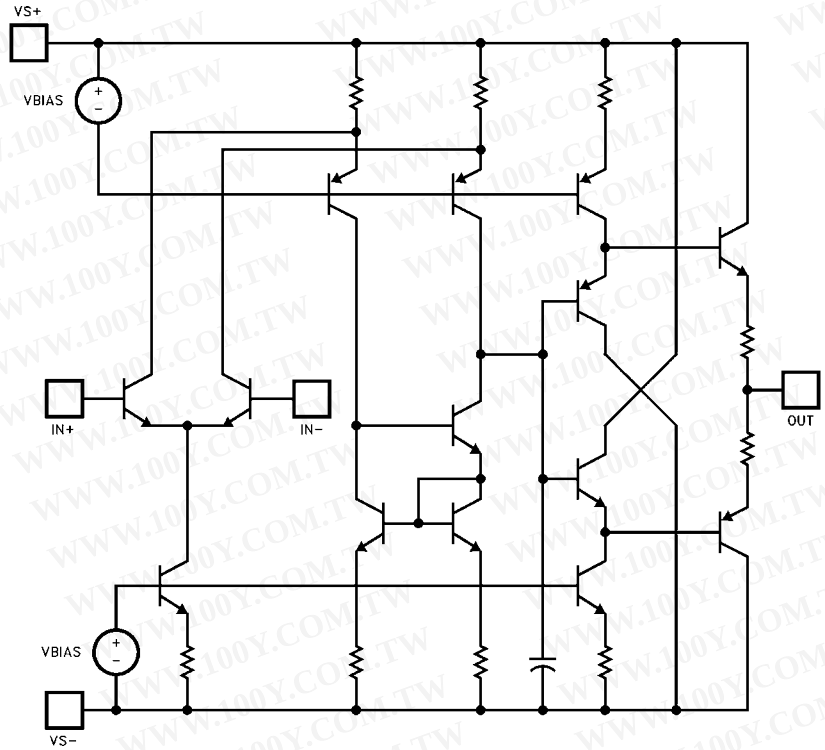
Small Signal Transient Response



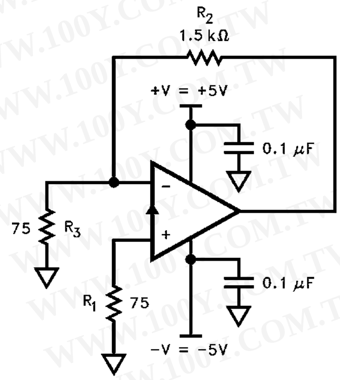
Large Signal Transient Response



Equivalent Circuit



Burn-In Circuit



All Packages Use The Same Schematic

Applications Information

Product Description

The EL2075C is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2075C uses a classical voltage-feedback topology which allows it to be used in a variety of applications requiring a noise gain ≥10 where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2075C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2075C is an excellent choice for applications such as log amplifiers.

The EL2075C also has excellent DC specifications: 200µV, V_{OS}, 2µA I_B, 0.1µA I_{OS}, and 90dB of CMRR. These specifications allow the EL2075C to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2075C is only 3.2 pA/√Hz, making it an excellent choice for high-sensitivity transimpedance amplifier configurations.

Gain-Bandwidth Product

The EL2075C has a gain-bandwidth product of 2GHz. For gains greater than 40, its closed-loop -3dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 40, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2075C has a -3dB bandwidth of 400MHz at a gain of +10, dropping to 200MHz at a gain of +20. It is important to note that the EL2075C has been designed so that this “extra” bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2075C in a gain of +10 only exhibits 1.5dB of peaking with a 100Ω load.

Output Drive Capability

The EL2075C has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6V_{PP} into a 50Ω load. This high output drive capability makes the EL2075C an ideal choice for RF and IF applications. Furthermore, the current drive of the EL2075C remains a minimum of 50mA at low temperatures. The EL2075C is current-limited at the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2075C has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without additional peaking.

Printed-Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1µF–10µF tantalum capacitor is recommended in parallel with a 0.01µF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2075C directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.

EL2075C

2GHz GBWP Gain-of-10 Stable Operational Amplifier

EL2075C Macromodel

```
*
* Connections: input
*            |    -input
*            |    |    +Vsupply
*            |    |    |    -Vsupply
*            |    |    |    |    output
*            |    |    |    |    |
.subckt M2075C 3    2    7    4    6
*
*Input Stage
*
ie 37 4 1mA
r6 36 37 15
r7 38 37 15
rc1 7 30 200
rc2 7 39 200
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1 Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 0.4 pF
rc 34 40 50
cc 40 0 0.05 pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 250
cpa 42 0 0.8 pF
rpb 42 43 50
cpb 43 0 0.5 pF
*
* Output Stage
*
ios1 7 50 3.0mA
ios2 51 4 3.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2
*
* Power Supply Current
*
ips 7 4 11.4mA
*
* Models
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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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