

HD74HC109

Dual J- $\bar{K}$ Flip-Flops (with Preset and Clear)

HITACHI

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Description

Each flip-flop has independent J, $\bar{K}$, preset, clear and clock inputs and Q and $\bar{Q}$ outputs. This device is edge sensitive to the clock input and changes state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 15 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 2 μ A max (T_a = 25°C)

Function Table

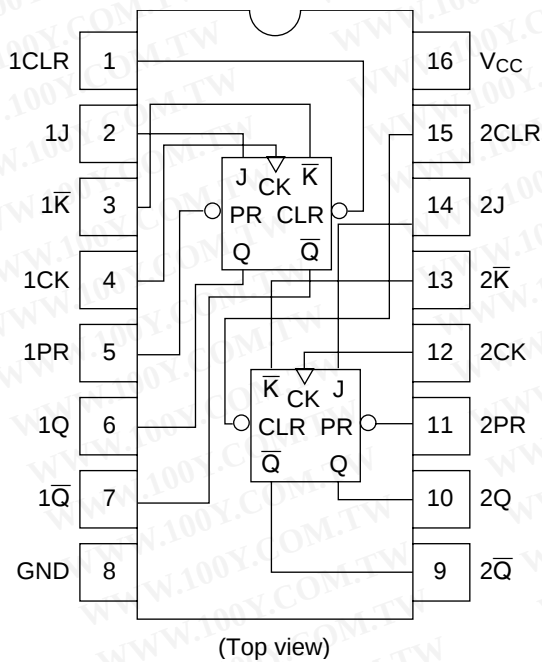
Inputs					Output	
Preset	Clear	Clock	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H ^{*1}	H ^{*1}
H	H	$\downarrow$	L	L	L	H
H	H	$\downarrow$	H	L	Toggle	
H	H	$\downarrow$	L	H	Q_0	$\bar{Q}_0$
H	H	$\downarrow$	H	H	H	L
H	H	L	X	X	Q_0	$\bar{Q}_0$

Note: 1. Q and $\bar{Q}$ will remain high as long as preset and clear input are low, but Q and $\bar{Q}$ are unpredictable if preset and clear input go high simultaneously.

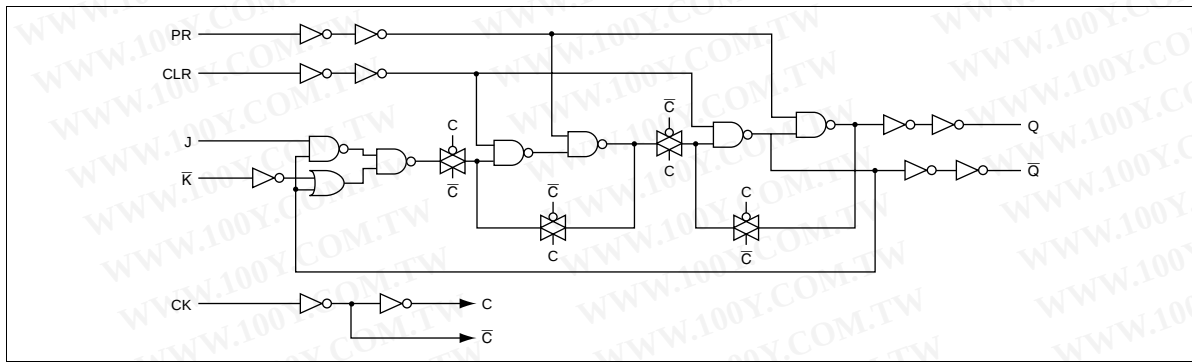
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Pin Arrangement

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Block Diagram (1/2)



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DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
		V _{OL}	2.0	—	0.0	0.1	—			0.1
	4.5		—	0.0	0.1	—	0.1			
	6.0		—	0.0	0.1	—	0.1			
	4.5		—	—	0.26	—	0.33	I _{OL} = 4 mA		
	6.0		—	—	0.26	—	0.33	I _{OL} = 5.2 mA		
	Input current		I _{in}	6.0	—	—	±0.1	—	±1.0	μA
	Quiescent supply current	I _{CC}	6.0	—	—	2.0	—	20	μA	Vin = V _{CC} or GND, I _{out} = 0 μA

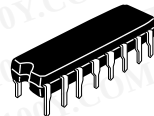
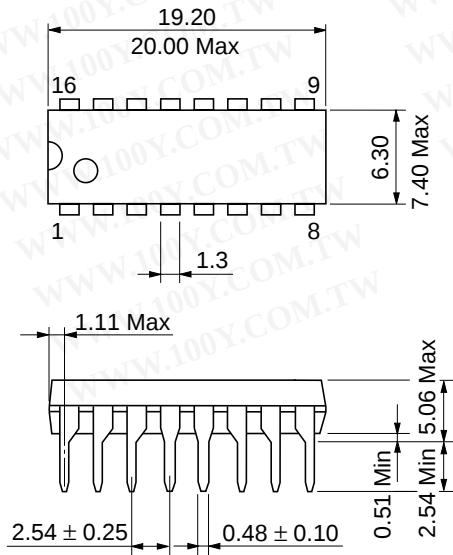
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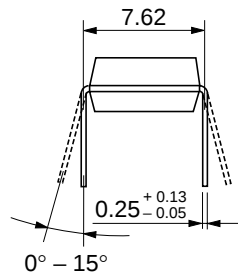
AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{\max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	175	—	220	ns	Clock to Q or $\bar{Q}$
		4.5	—	15	35	—	44		
		6.0	—	—	30	—	37		
		2.0	—	—	190	—	240	ns	Preset or Clear to Clock
		4.5	—	14	38	—	48		
		6.0	—	—	32	—	41		
Removal time	t_{rem}	2.0	25	—	—	32	—	ns	
		4.5	5	1	—	6	—		
		6.0	4	—	—	5	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	4	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	0	—	—	0	—	ns	
		4.5	0	-4	—	0	—		
		6.0	0	—	—	0	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	5	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	90	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

Unit: mm



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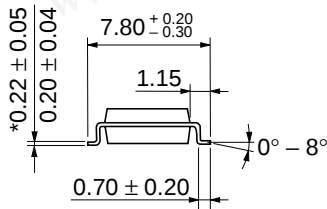
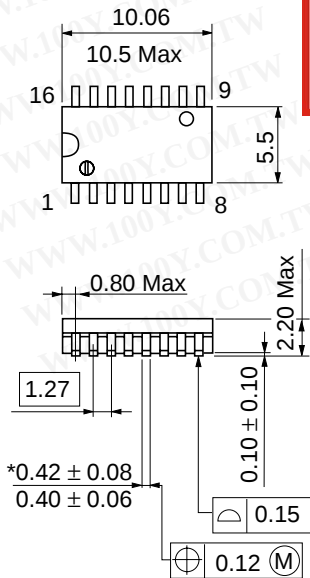
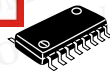
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm

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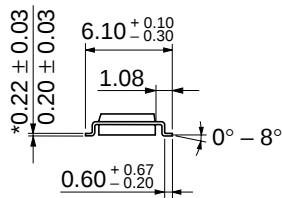
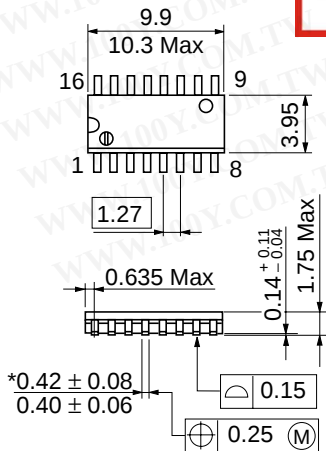
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*Dimension including the plating thickness
Base material dimension

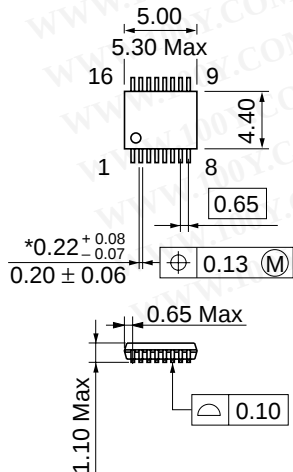
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

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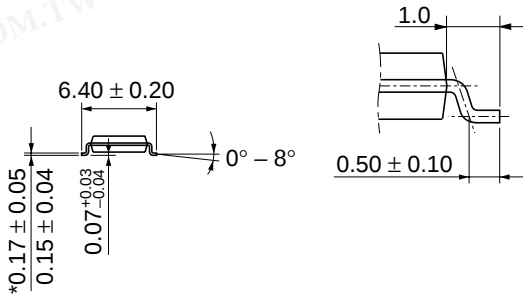


*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



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*Dimension including the plating thickness
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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