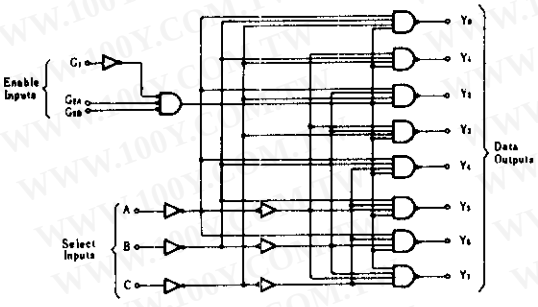
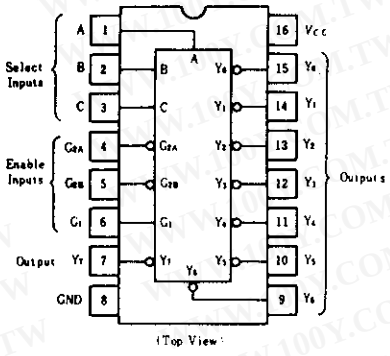
HD74LS138 ●3-Line-to-8-Line Decoders/Demultiplexers

The HD74LS138 decodes one-of-eight line dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■FUNCTION TABLE

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
×	H	×	×	×	H	H	H	H	H	H	H	H
L	×	×	×	×	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H; high level, L; low level, X; irrelevant
*; $G_2 = G_{2A} + G_{2B}$

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	–	–	V
	V_{IL}		–	–	0.8	V
Output voltage	V_{OH}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=−400μA	2.7	–	–	V
	V_{OL}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OL}=4mA	–	–	0.4	V
		V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OL}=8mA	–	–	0.5	
Input current	I_{IH}	V_{CC}=5.25V, V_I=2.7V	–	–	20	μA
	I_{IL}	V_{CC}=5.25V, V_I=0.4V	–	–	−0.4	mA
	I_I	V_{CC}=5.25V, V_I=7V	–	–	0.1	mA
Short-circuit output current	I_{OS}	V_{CC}=5.25V	−20	–	−100	mA
Supply current	I_{CC}	V_{CC}=5.25V, Outputs enabled and open	–	6.3	10	mA
Input clamp voltage	V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA	–	–	−1.5	V

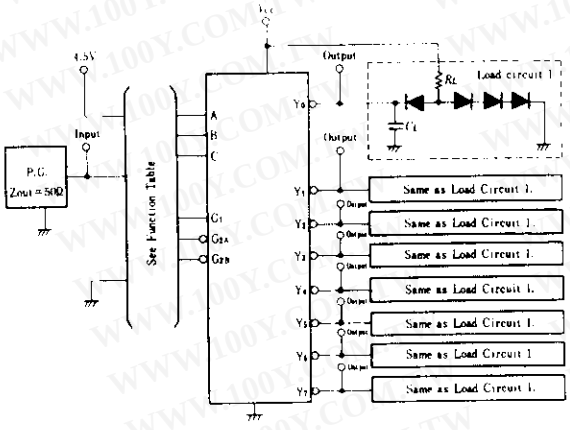
* V_{CC}=5V, Ta=25°C

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃)

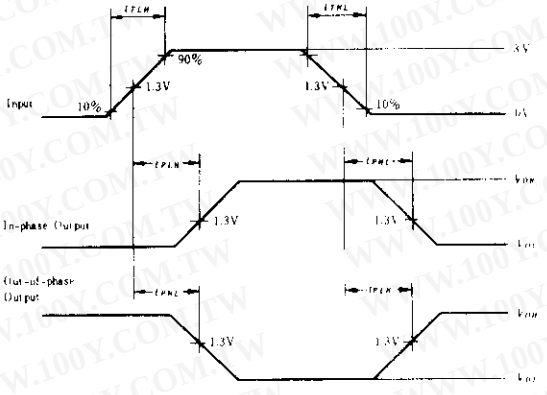
Item	Symbol	Inputs	Output	Levels of delay	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	Binary Select A, B, C	Y	2	C_L=15pF R_L=2kΩ	–	13	20	ns
	t_{PHL}					–	27	41	ns
	t_{PLH}			3		–	18	27	ns
	t_{PHL}					–	26	39	ns
	t_{PLH}	Enable G_{2A}, G_{2B}	Y	2		–	12	18	ns
	t_{PHL}					–	21	32	ns
	t_{PLH}	Enable G_1		3		–	17	26	ns
	t_{PHL}					–	25	38	ns

■TESTING METHOD

1) Test Circuit



Waveform

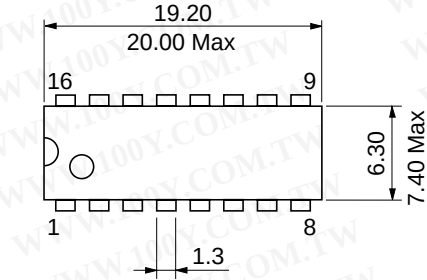


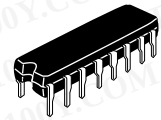
Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.
3. Input pulse: t_{TLH}≦15ns, t_{THL}≦6ns, PRR=1MHz, duty cycle 50%.

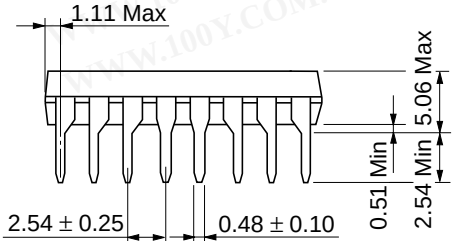
■RELATION BETWEEN INPUT AND OUTPUT TO LEVELS OF DELAY

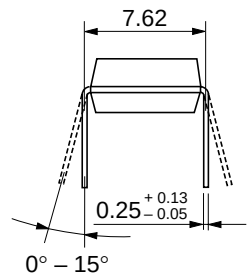
Inputs	Outputs							
	2 levels of delay				3 levels of delay			
A	Y_0	Y_2	Y_4	Y_6	Y_1	Y_3	Y_5	Y_7
B	Y_0	Y_1	Y_4	Y_5	Y_2	Y_3	Y_6	Y_7
C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
G_1					Y_0～Y_7			
G_{2A}, G_{2B}	Y_0～Y_7							

Unit: mm



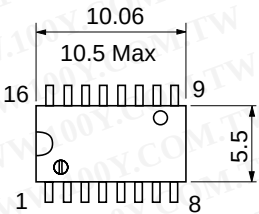


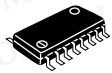


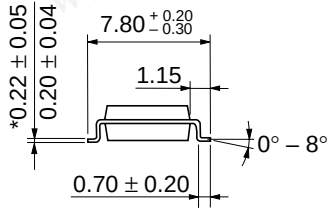


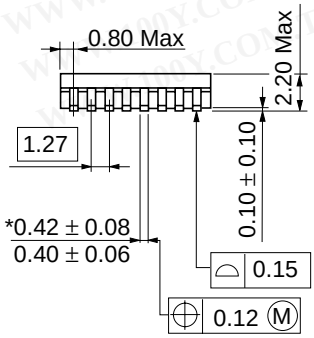
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





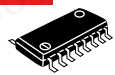


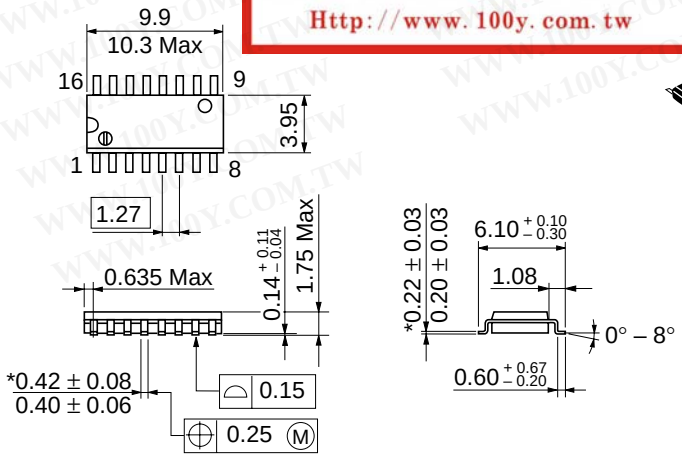


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm





*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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