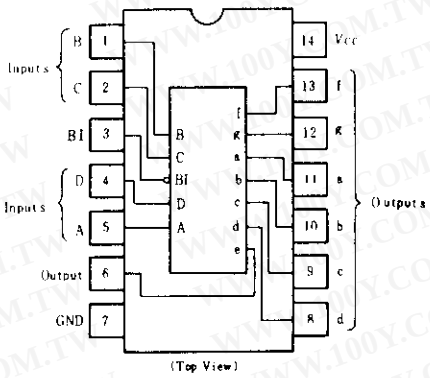
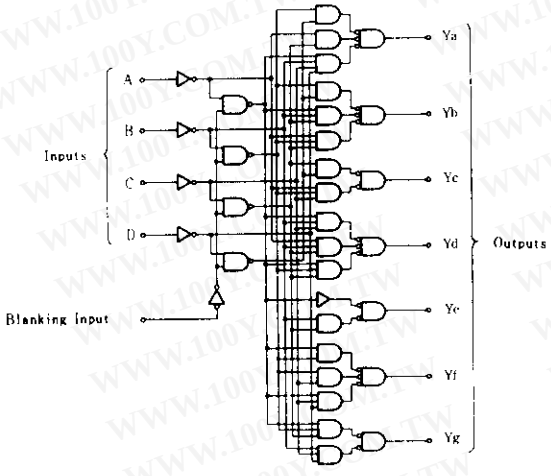
# HD74LS49 ●BCD-to-Seven Segment Decoder / Driver (with Open collector outputs)

The HD74LS49 features active-high outputs for driving lamp buffer. This circuit incorporates a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. It contains an over-riding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the output. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

## ■PIN ARRANGEMENT




## ■BLOCK DIAGRAM






## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{IN}$ | 7.0 | V |
| Output current (off state) | $I_{O(off)}$ | 1 | mA |
| Operating temperature range | $T_{opr}$ | − 20 ~ + 75 | ℃ |
| Storage temperature range | $T_{stg}$ | 65 ~ + 150 | ℃ |

## ■FUNCTION TABLE

| Decimal or Function | Inputs | | | | | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | BI | a | b | c | d | e | f | g | |
| 0 | L | L | L | L | H | H | H | H | H | H | H | L | |
| 1 | L | L | L | H | H | L | H | H | L | L | L | L | |
| 2 | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | L | H | H | L | H | L | L | H | H | H | H | H | |
| 7 | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | 1 |
| 9 | H | L | L | H | H | H | H | H | L | L | H | H | |
| 10 | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | × | × | × | × | L | L | L | L | L | L | L | L | 2 |

H; high level, L; low level, X; irrelevant

Notes: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

## ■ELECTRICAL CHARACTERISTICS ( $Ta = -20 \sim +75°C$ )

| Item | Symbol | Test Conditions | | min | typ* | max | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | | | 2.0 | – | – | V |
| | $V_{IL}$ | | | – | – | 0.8 | V |
| Output current | $I_{OH}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$ | | – | – | 250 | μA |
| Output voltage | $V_{OL}$ | $V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$ | $I_{OL}=4mA$ | – | – | 0.4 | V |
| | | | $I_{OL}=8mA$ | – | – | 0.5 | |
| Input current | $I_{IH}$ | $V_{CC}=5.25V$, $V_I=2.7V$ | | – | – | 20 | μA |
| | $I_{IL}$ | $V_{CC}=5.25V$, $V_I=0.4V$ | | – | – | −0.4 | mA |
| | $I_I$ | $V_{CC}=5.25V$, $V_I=7V$ | | – | – | 0.1 | mA |
| Supply current ** | $I_{CC}$ | $V_{CC}=5.25V$ | | – | 8 | 15 | mA |
| Input clamp voltage | $V_{IK}$ | $V_{CC}=4.75V$, $I_{IN}=-18mA$ | | – | – | −1.5 | V |

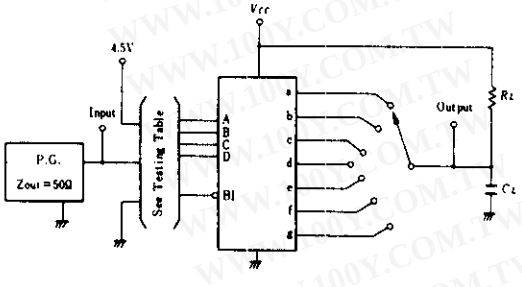
* $V_{CC}=5V$, $Ta=25°C$
** $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

## ■SWITCHING CHARACTERISTICS ( $V_{CC}=5V$, $Ta=25°C$ )

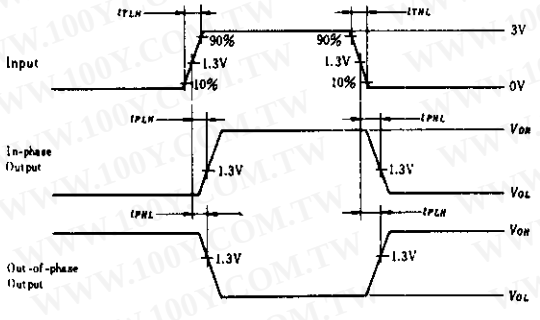
| Item | Symbol | Input | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PHL}$ | A | $C_L=15pF$, $R_L=2k\Omega$ | – | – | 100 | ns |
| | $t_{PLH}$ | | | – | – | 100 | |
| | $t_{PHL}$ | BI | $C_L=15pF$, $R_L=6k\Omega$ | – | – | 100 | ns |
| | $t_{PLH}$ | | | – | – | 100 | |

## ■TESTING METHOD

### 1) Test Circuit




### Waveform

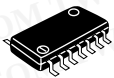


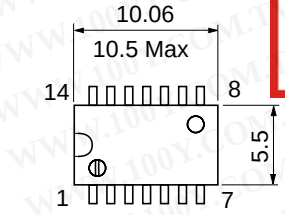

### 2) Testing Table

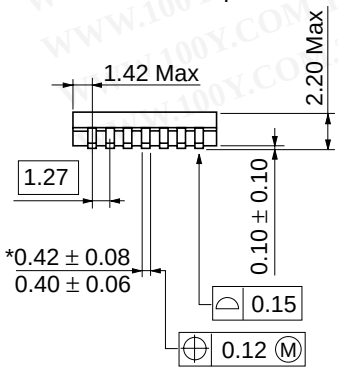
| Item | Inputs | | | | | Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BI | D | C | B | A | a | b | c | d | e | f | g |
| | 4.5V | GND | GND | GND | IN | OUT | – | – | OUT | OUT | OUT | – |
| $t_{PLH}$ | 4.5V | GND | GND | 4.5V | IN | – | – | OUT | – | OUT | – | – |
| $t_{PHL}$ | 4.5V | GND | 4.5V | 4.5V | IN | OUT | OUT | – | OUT | OUT | OUT | OUT |
| | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | OUT | – |

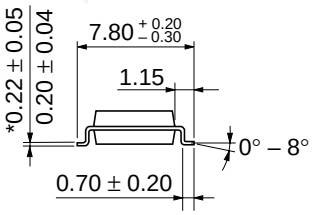
Unit: mm







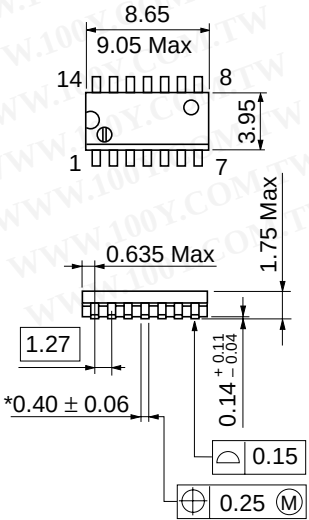



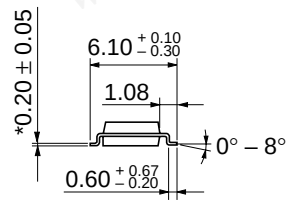



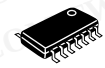

*Dimension including the plating thickness
Base material dimension

| | |
|---|---|
| Hitachi Code | FP-14DA |
| JEDEC | — |
| EIAJ | Conforms |
| Weight (reference value) | 0.23 g |

Unit: mm



| | |
|---|---|
| Hitachi Code | FP-14DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 0.13 g |

*Pd plating

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