

HD74HC93

4-bit Binary Counter

HITACHI

Description

The HD74HC93 is a 4-bit ripple type counter consisting of four master/slave flip-flops that are internally connected to provide separate divide-by-two and divide-by-eight sections. Each section has a separate clock input which initiates state changes of the counter on the high-to-low clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the clock of the HD74HC93. Q_A is the output of the divide-by-two section; Q_B , Q_C , and Q_D are the binary outputs of the divide-by-eight section.

A gated AND asynchronous reset is provided which resets all the flip-flops.

Because the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

1. A 4-bit ripple counter – The Q_A output must be externally connected to the clock B input. The input count pulses are applied to the clock A input. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_A , Q_B , Q_C and Q_D outputs.
2. A 3-bit ripple counter – The input count pulses are applied to the clock B input. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_B , Q_C and Q_D outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

Features

- High Speed Operation: t_{pd} (A to Q_A) = 13 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)

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Function Table

Reset/Count Function Table

Reset Inputs		Outputs			
R ₀₍₁₎	R ₀₍₂₎	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	×	Count			
×	L	Count			

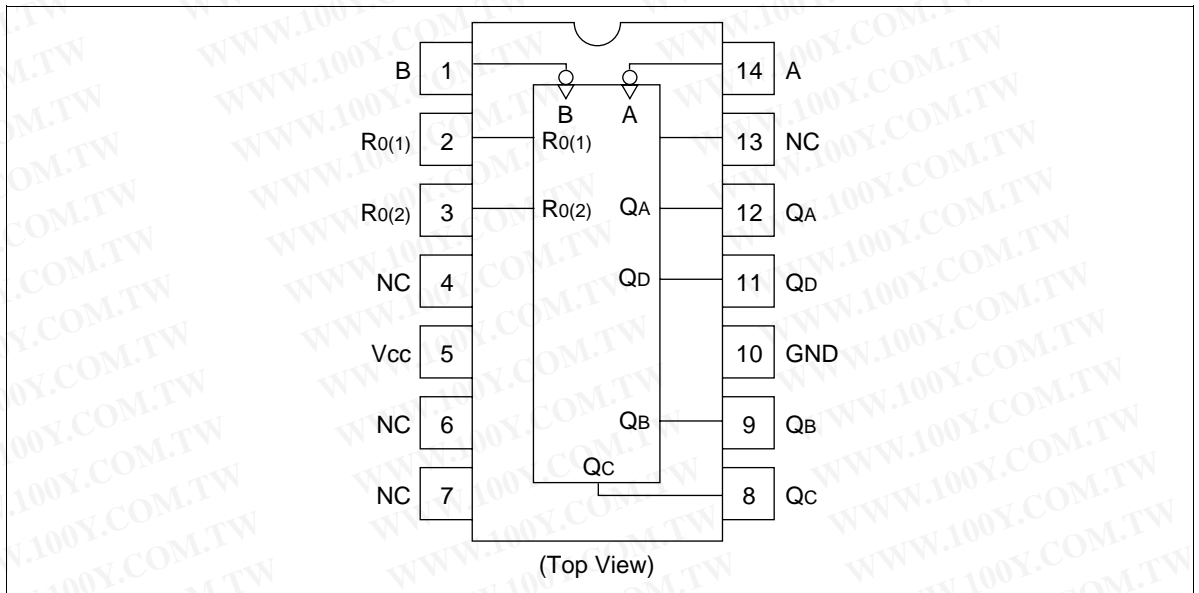
BCD Count Sequence

Count	Outputs			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes: Output Q_A is connected to input B for BCD count.

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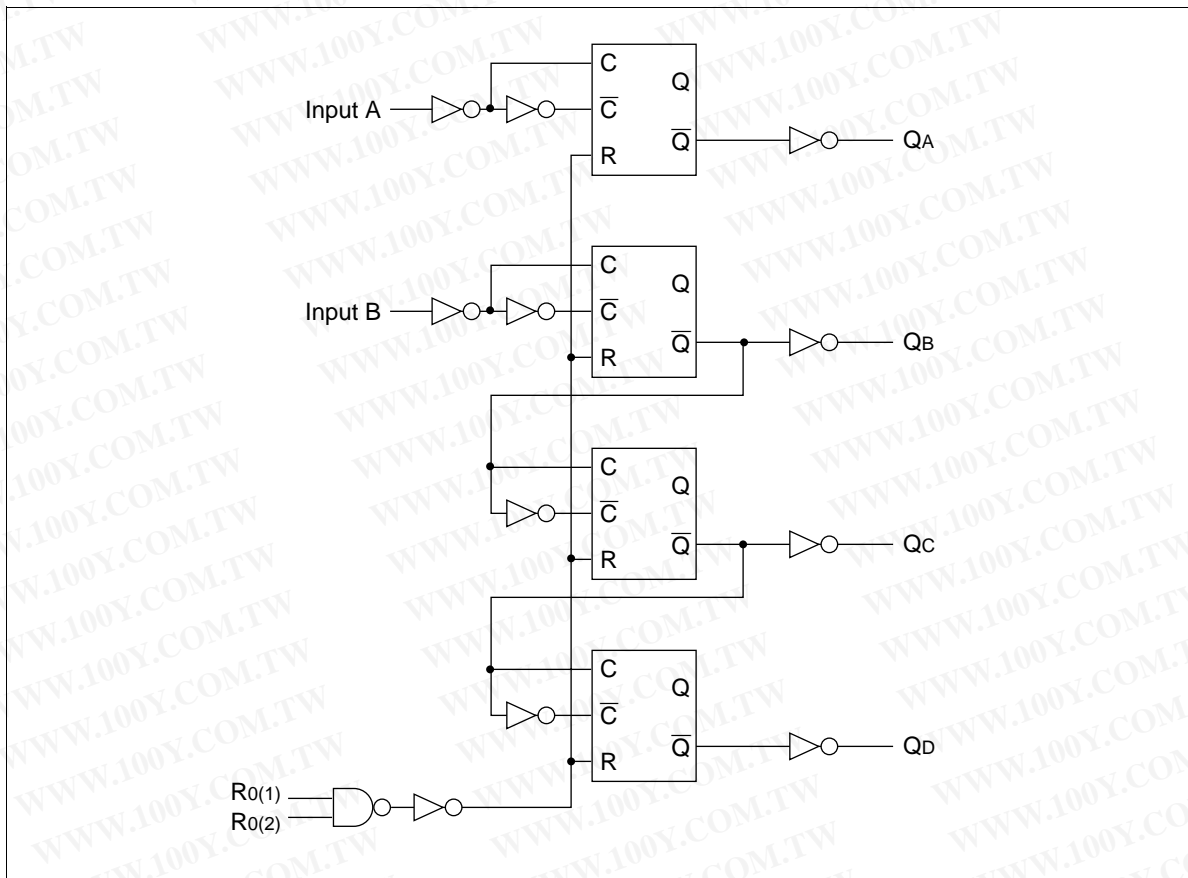
Pin Arrangement



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Block Diagram



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DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V			
		4.5	3.15	—	—	3.15	—				
		6.0	4.2	—	—	4.2	—				
	V _{IL}	2.0	—	—	0.5	—	0.5			V	
		4.5	—	—	1.35	—	1.35				
		6.0	—	—	1.8	—	1.8				
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA		
		4.5	4.4	4.5	—	4.4	—				
		6.0	5.9	6.0	—	5.9	—				
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA	
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA	
		6.0	—	0.0	0.1	—	0.1			V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA
	V _{OL}	4.5	—	0.0	0.1	—	0.1				
		6.0	—	0.0	0.1	—	0.1				
		4.5	—	—	0.26	—	0.33	I _{OL} = 4 mA			
		6.0	—	—	0.26	—	0.33	I _{OL} = 5.2 mA			
		Input current	I _{in}	6.0	—	—	±0.1	—	±1.0		
		Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA

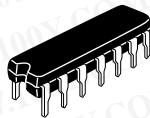
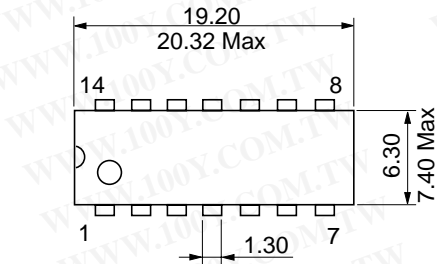
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AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

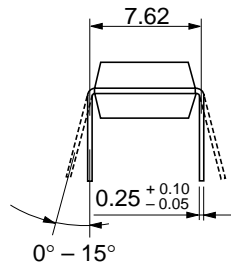
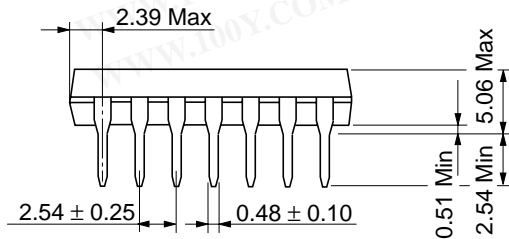
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH}	2.0	—	—	120	—	150	ns	A to Q_A
		4.5	—	13	24	—	30		
		6.0	—	—	20	—	26		
	t_{PHL}	2.0	—	—	340	—	425	ns	A to Q_D
		4.5	—	42	68	—	85		
		6.0	—	—	58	—	72		
	t_{PLH}	2.0	—	—	130	—	165	ns	B to Q_B
		4.5	—	13	26	—	33		
		6.0	—	—	22	—	28		
	t_{PHL}	2.0	—	—	185	—	230	ns	B to Q_C
		4.5	—	21	37	—	46		
		6.0	—	—	31	—	39		
	t_{PLH}	2.0	—	—	220	—	275	ns	B to Q_D
		4.5	—	27	44	—	55		
		6.0	—	—	37	—	47		
	t_{PHL}	2.0	—	—	175	—	220	ns	Set-to-0 to $Q_{A \text{ to } D}$
		4.5	—	13	35	—	44		
		6.0	—	—	30	—	37		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

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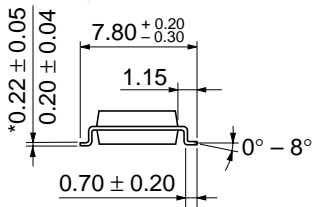
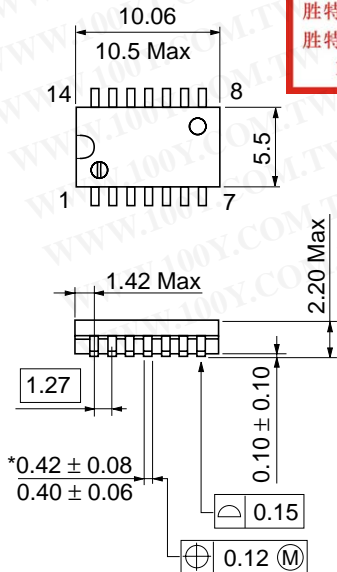
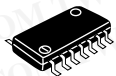


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Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

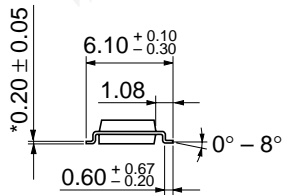
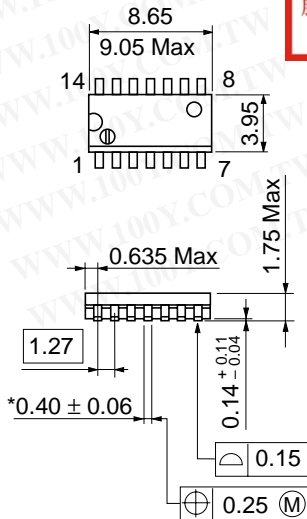
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*Dimension including the plating thickness
 Base material dimension

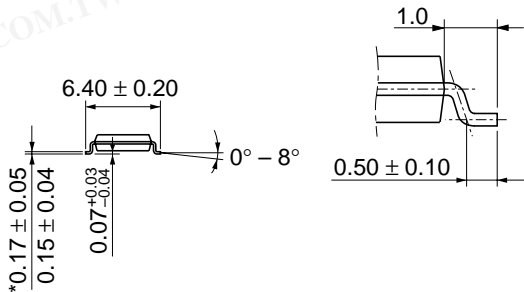
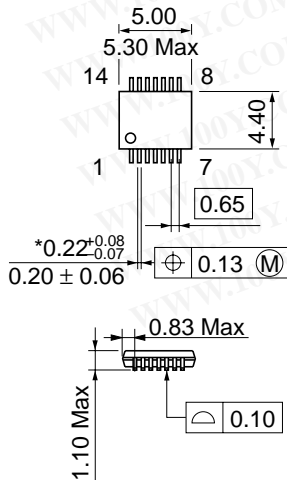
Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

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JEDEC	Conforms
EIAJ	Conforms
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*Dimension including the plating thickness
 Base material dimension

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JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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