

# HD74LS164

## 8-Bit Parallel-Out Serial-in Shift Register

REJ03D0448-0200

Rev.2.00

Feb.18.2005

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

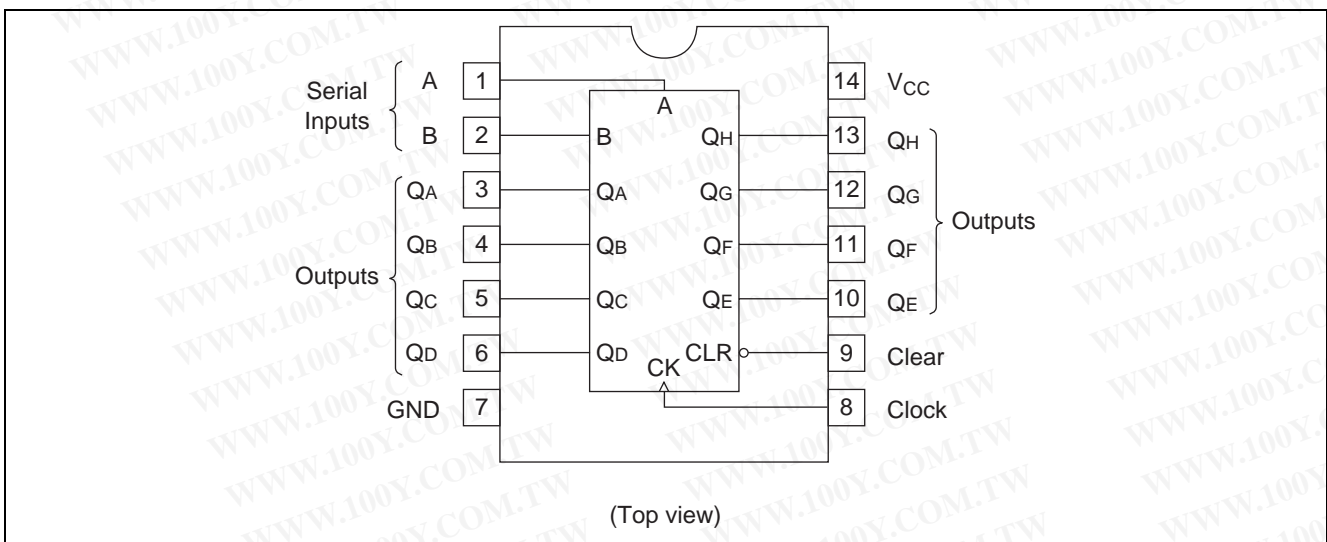
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS164P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS164FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74LS164RPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement



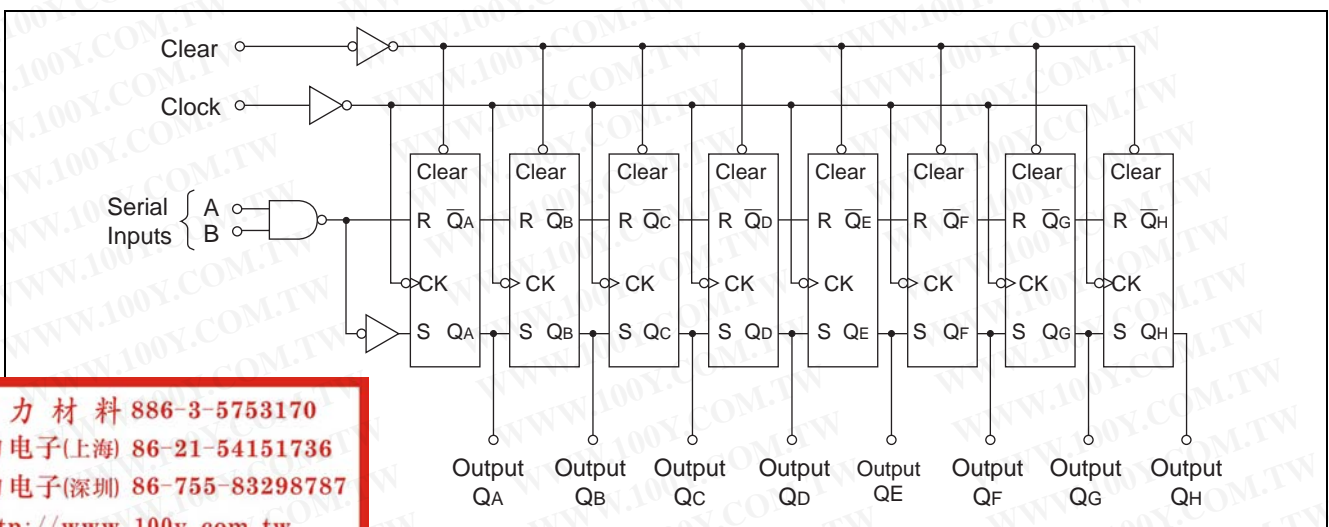
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Function Table

Inputs				Outputs		
Clear	Clock	A	B	Q <sub>A</sub>	Q <sub>B</sub> .....Q <sub>H</sub>	
L	X	X	X	L	L	L
H	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>
H	↑	H	H	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	↑	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	↑	X	L	L	Q <sub>An</sub>	Q <sub>Gn</sub>

- Notes:
1. H; high level, L; low level, X; irrelevant
  2. ↑; transition from low to high level
  3. Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>H0</sub>; the level of Q<sub>A</sub>, Q<sub>B</sub>, or Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established.
  4. Q<sub>An</sub>, Q<sub>Gn</sub>; the level of Q<sub>A</sub> or Q<sub>G</sub> before the most-recent ↑ transition of the clock; indicates a one-bit shift.

Block Diagram



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Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	7	V
Input voltage	V <sub>IN</sub>	7	V
Power dissipation	P <sub>T</sub>	400	mW
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output current	I <sub>OH</sub>	—	—	-400	μA
	I <sub>OL</sub>	—	—	8	mA
Operating temperature	T <sub>opr</sub>	-20	25	75	°C
Clock frequency	f <sub>clock</sub>	0	—	25	MHz
Clock pulse width	t <sub>w</sub> (CK)	20	—	—	ns
Clear pulse width	t <sub>w</sub> (CLR)	20	—	—	ns
Data setup time	t <sub>su</sub>	15	—	—	ns
Data hold time	t <sub>h</sub>	5	—	—	ns

## Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V <sub>IH</sub>	2.0	—	—	V	
	V <sub>IL</sub>	—	—	0.8	V	
Output voltage	V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA
	V <sub>OL</sub>	—	—	0.4	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V
—		—	0.5			
Input current	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V
Short-circuit output current	I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V
Supply current**	I <sub>CC</sub>	—	16	27	mA	V <sub>CC</sub> = 5.25 V
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA

Notes: \* V<sub>CC</sub> = 5 V, Ta = 25°C\*\* I<sub>CC</sub> is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary grounded, then 4.5 V applied to clear.

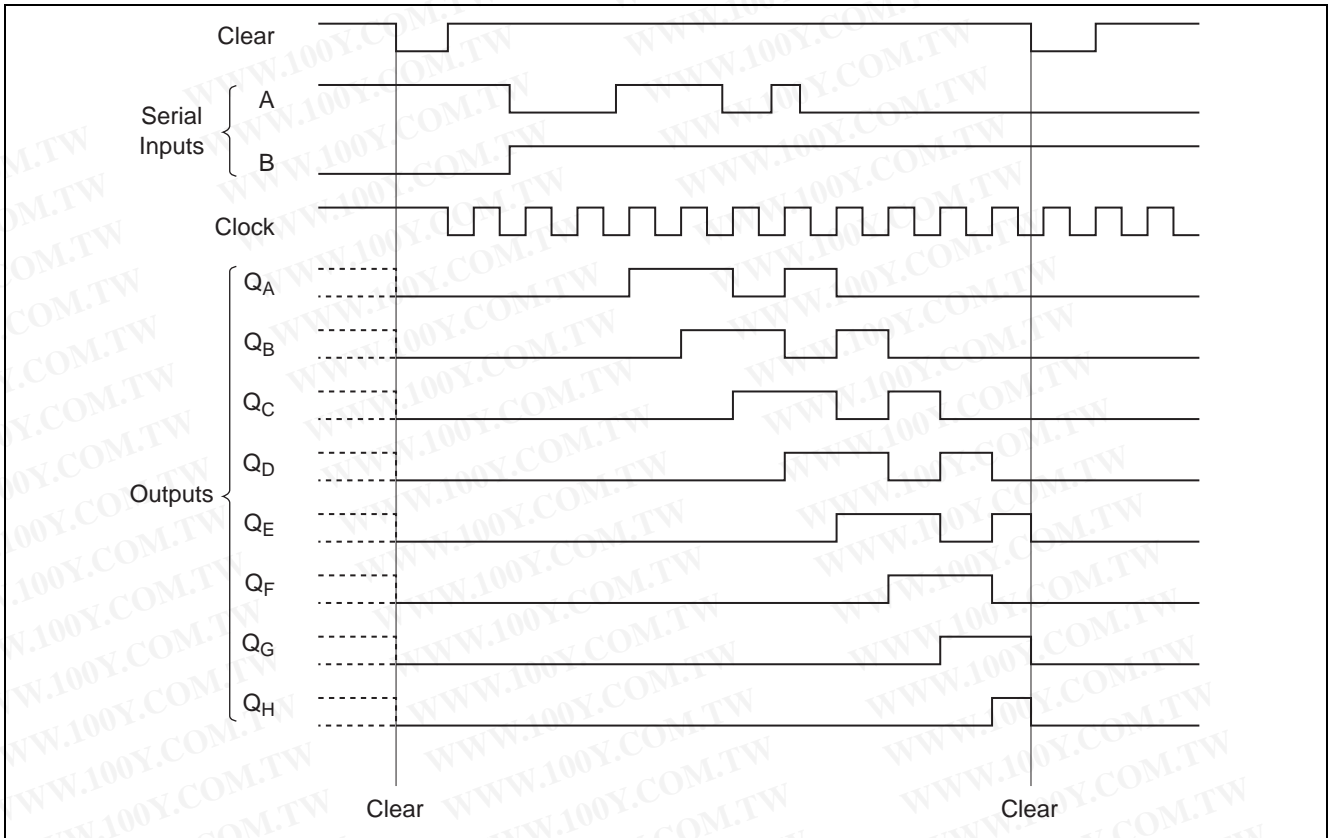
## Switching Characteristics

(V<sub>CC</sub> = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f <sub>max</sub>			25	36	—	MHz	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
Propagation delay time	t <sub>PHL</sub>	Clear	Q	—	24	36	ns	
	t <sub>PLH</sub>	Clock	Q	—	17	27	ns	
	t <sub>PHL</sub>	Clock	Q	—	21	32	ns	

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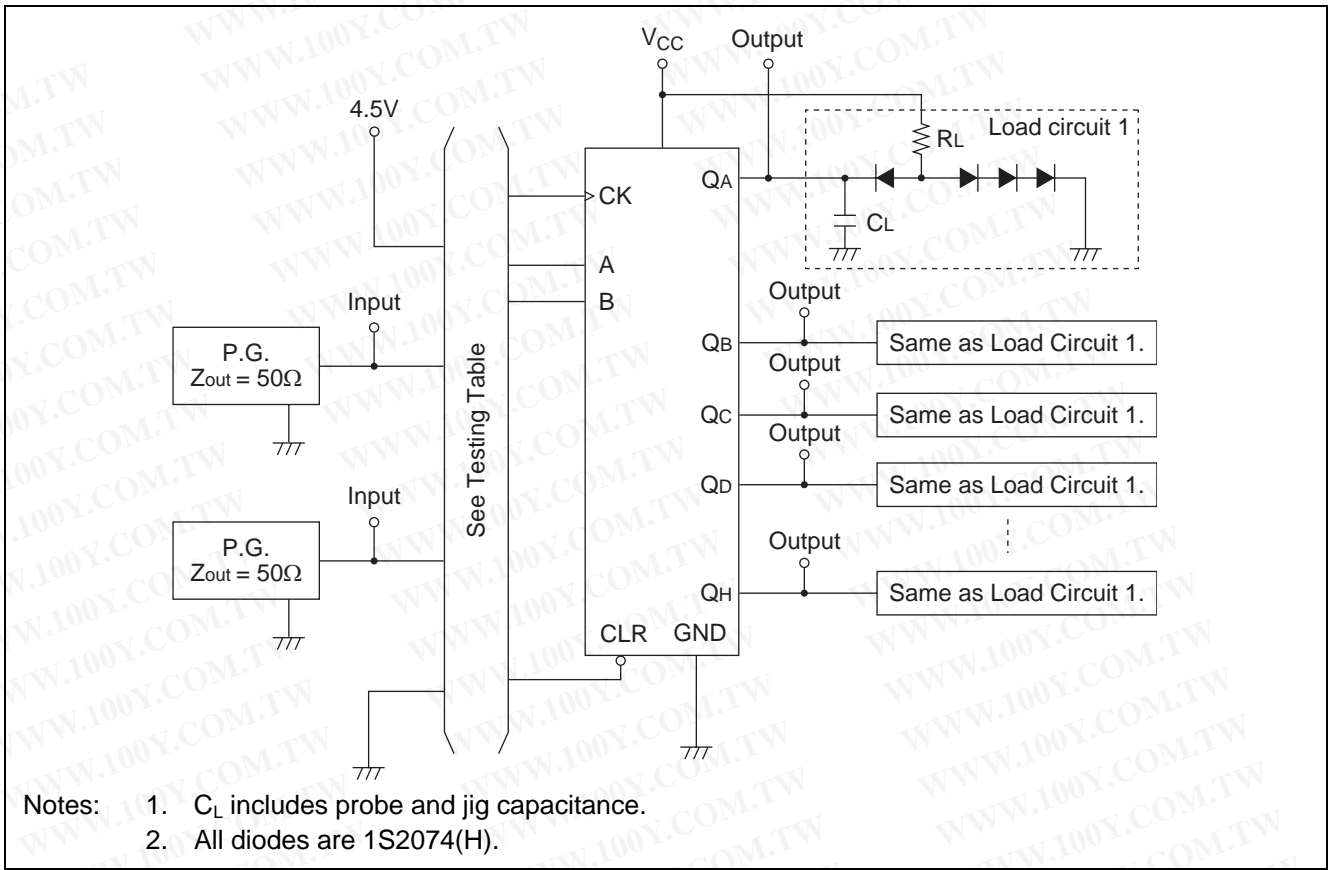
Typical Clear, Shift, and Clear Sequences



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Testing Method

Test Circuit

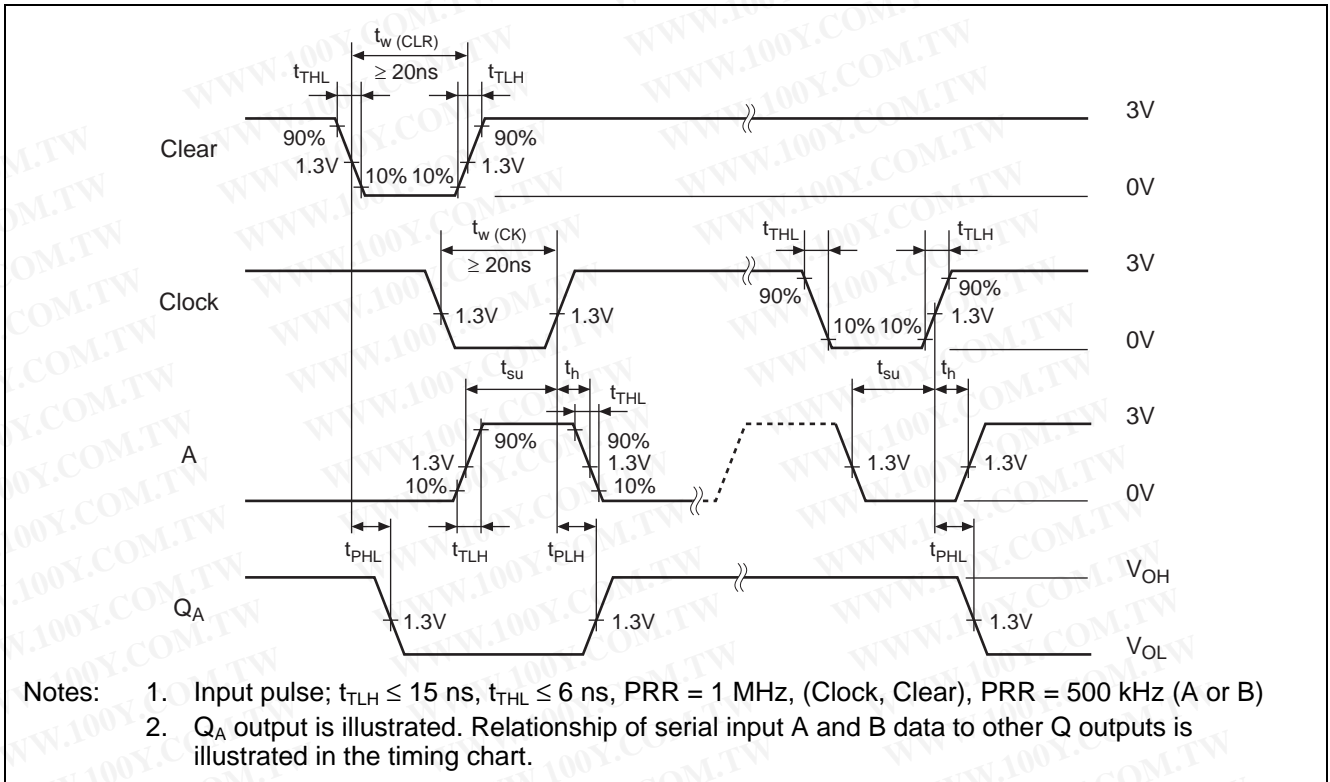


Testing Table

Item	From input to output	Inputs				Outputs							
		CLR	CK	A	B	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>E</sub>	Q <sub>F</sub>	Q <sub>G</sub>	Q <sub>H</sub>
$f_{max}$		4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
$t_{PLH}$	Clear→Q	IN	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
$t_{PHL}$	CK→Q	4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT

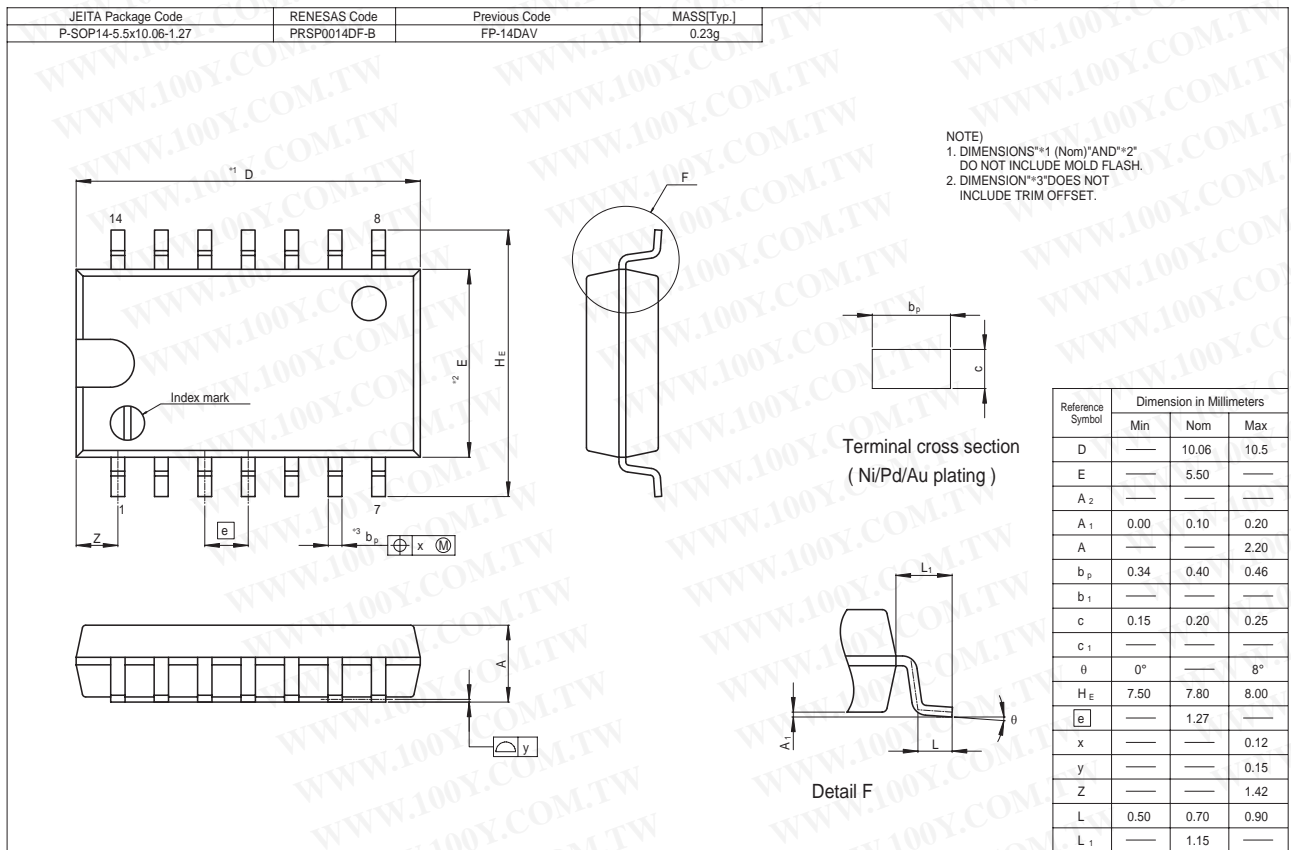
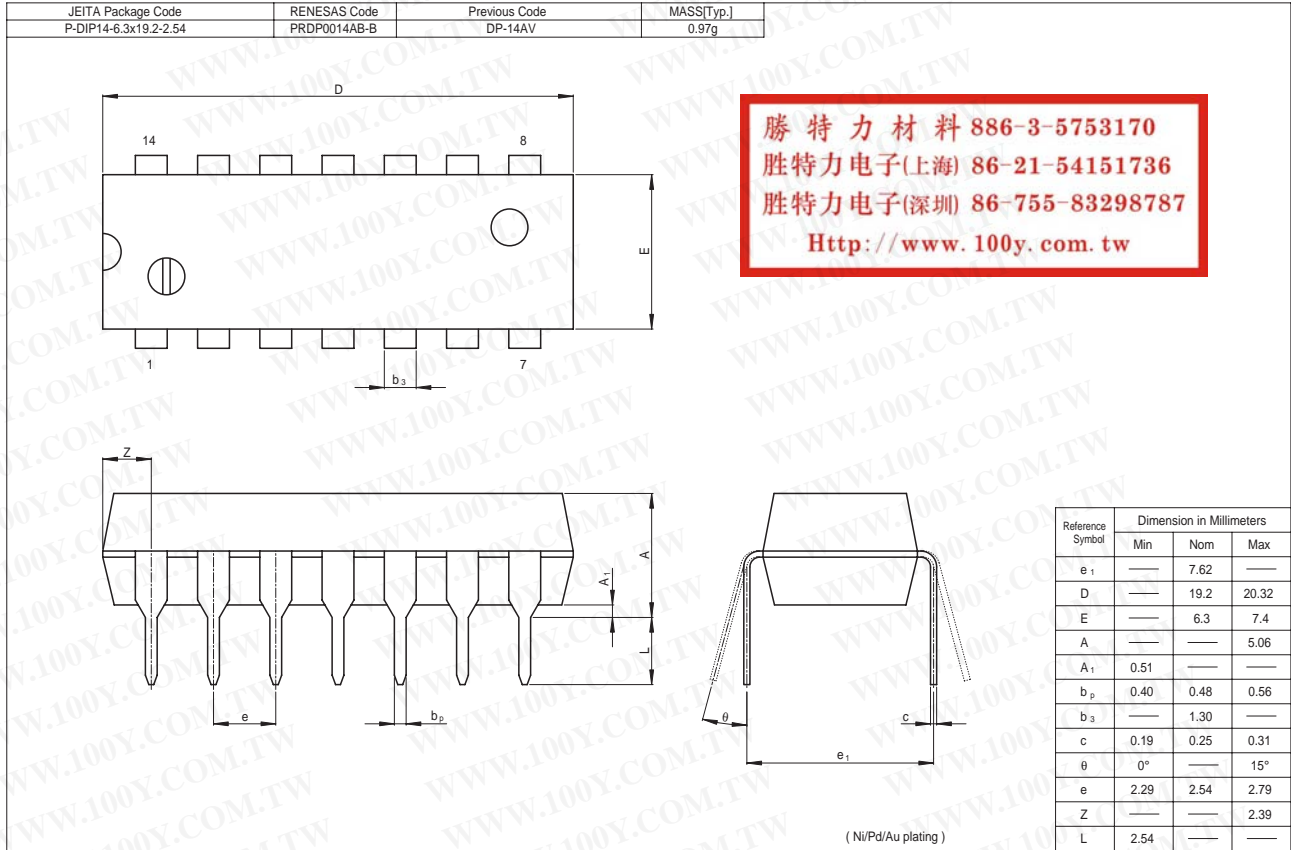
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Waveform



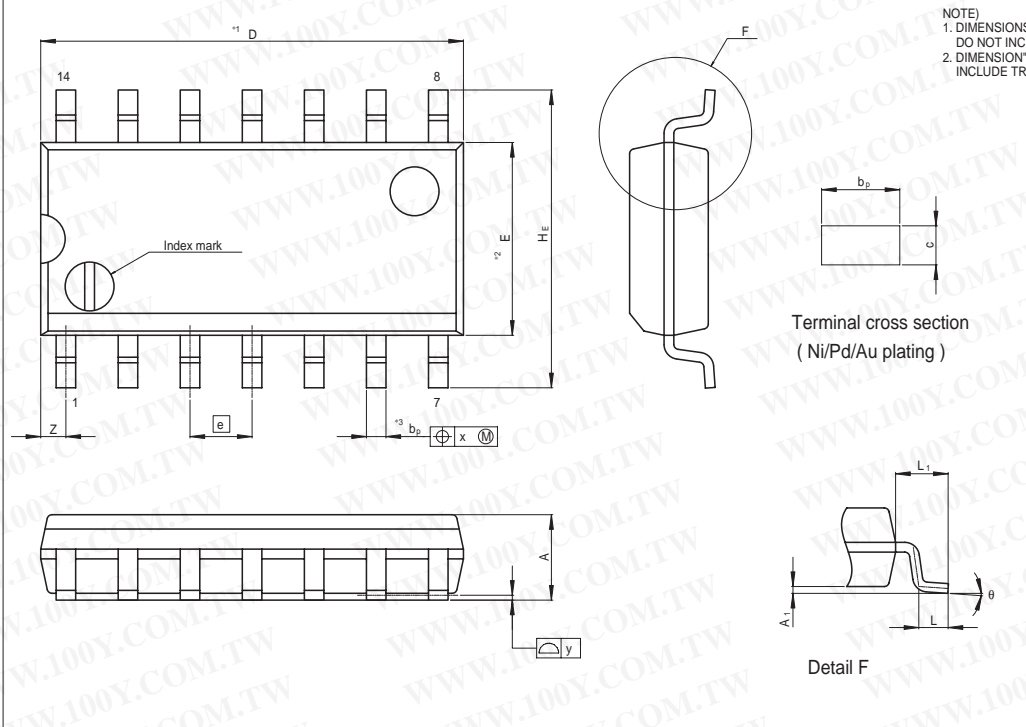
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Package Dimensions



HD74LS164

JEITA Package Code P-SOP14-3.95x8.65-1.27	RENESAS Code PRSP0014DE-A	Previous Code FP-14DNV	MASS[Typ.] 0.13g
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Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	8.65	9.05
E	—	3.95	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.10	0.14	0.25
A	—	—	1.75
b <sub>p</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.15
Z	—	—	0.635
L	0.40	0.60	1.27
L <sub>1</sub>	—	1.08	—

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