HM6264A Series

8192-word × 8-bit High Speed CMOS Static RAM

Features

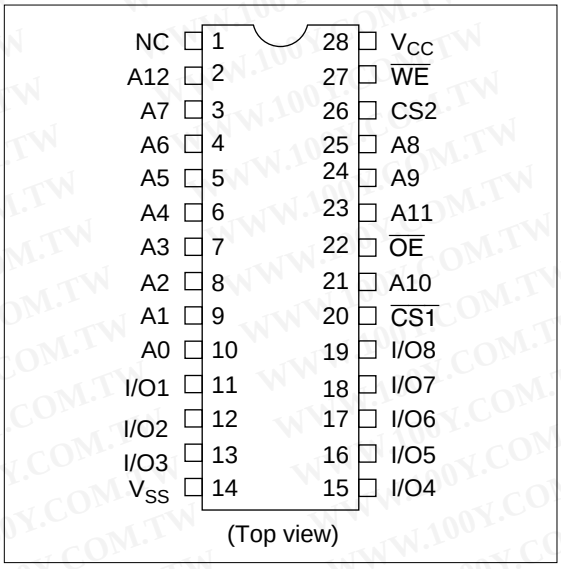
- Low-power standby
  - 0.1 mW (typ)
  - 10 µW (typ) L-/LL-version
- Low power operation
  - 15 mW/MHz (typ)
- Fast access time
  - l00/120/150 ns (max)
- Single +5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle time
- Common data input and output, three-state output
- Directly TTL compatible
  - All inputs and outputs
- Battery back up operation capability (L-/LL-version)

Ordering Information

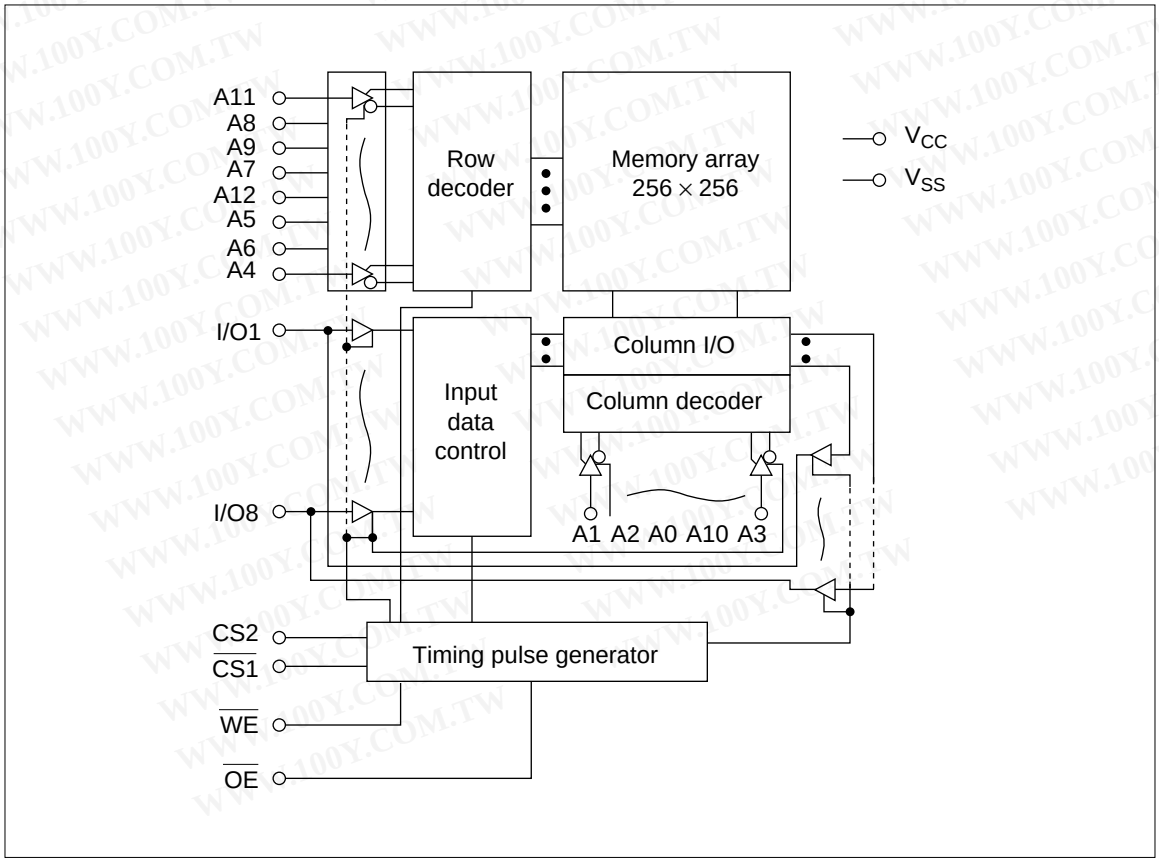
Type No.	Access time	Package
HM6264AP-10	100 ns	600-mil, 28-pin plastic DIP (DP-28)
HM6264AP-12	120 ns	
HM6264AP-15	150 ns	
HM6264ALP-10	100 ns	
HM6264ALP-12	120 ns	
HM6264ALP-15	150 ns	
HM6264ALP-10L	100 ns	
HM6264ALP-12L	120 ns	
HM6264ALP-15L	150 ns	
HM6264ASP-10	100 ns	300-mil, 28-pin plastic DIP (DP-28N)
HM6264ASP-12	120 ns	
HM6264ASP-15	150 ns	
HM6264ALSP-10	100 ns	
HM6264ALSP-12	120 ns	
HM6264ALSP-15	150 ns	
HM6264ALSP-10L	100 ns	
HM6264ALSP-12L	120 ns	
HM6264ALSP-15L	150 ns	
HM6264AFP-10	100 ns	28-pin plastic SOP *1 (FP-28D/DA)
HM6264AFP-12	120 ns	
HM6264AFP-15	150 ns	
HM6264ALFP-10	100 ns	
HM6264ALFP-12	120 ns	
HM6264ALFP-15	150 ns	
HM6264ALFP-10L	100 ns	
HM6264ALFP-12L	120 ns	
HM6264ALFP-15L	150 ns	

Note: 1. T is added to the end of the type number for a SOP of 3.00 mm (max) thickness.

Pin Arrangement



Block Diagram



Truth Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	I/O pin	V_{CC} current	Note
×	H	×	×	Not selected (power down)	High Z	I_{SB}, I_{SB1}	
×	×	L	×		High Z	I_{SB}, I_{SB1}	
H	L	H	H	Output disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	Read cycle
L	L	H	H	Write	Din	I_{CC}	Write cycle 1
L	L	H	L	Write	Din	I_{CC}	Write cycle 2

Note: ×: Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage *1	V_T	–0.5 *2 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature (under bias)	Tbias	–10 to +85	°C

Notes: 1. With respect to V_{SS}.
2. –3.0 V for pulse width ≤ 50 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	–0.3 *1	—	0.8	V

Note: 1. –3.0 V for pulse width ≤ 50 ns

DC and Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CCDC}	—	7	15	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	— —	30 30	45*5 55*6	mA	Min. cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $I_{I/O}$ = 0 mA
	I_{CC2}	—	3	5	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current	I_{SB}	—	1	3	mA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}
	I_{SB1} *2	—	0.02	2	mA	$\overline{CS1}$ ≥ Vcc – 0.2 V, CS2 ≥ Vcc – 0.2 V or
		—	2*3	100*3	µA	0 V ≤ CS2 ≤ 0.2 V, 0 V ≤ Vin
		—	2*4	50*4		
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes:
1. Typical values are at V_{CC} = 5.0 V, Ta = 25°C and not guaranteed.
2. V_{IL} min = –0.3 V
3. These characteristics are guaranteed only for the L-version.
4. These characteristics are guaranteed only for the LL-version.
5. For 120 ns/150 ns version.
6. For 100 ns version.

Capacitance (f = 1 MHz, Ta = 25°C)*1

Parameter	Symbol	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	5	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	7	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and is not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

AC Test Conditions:

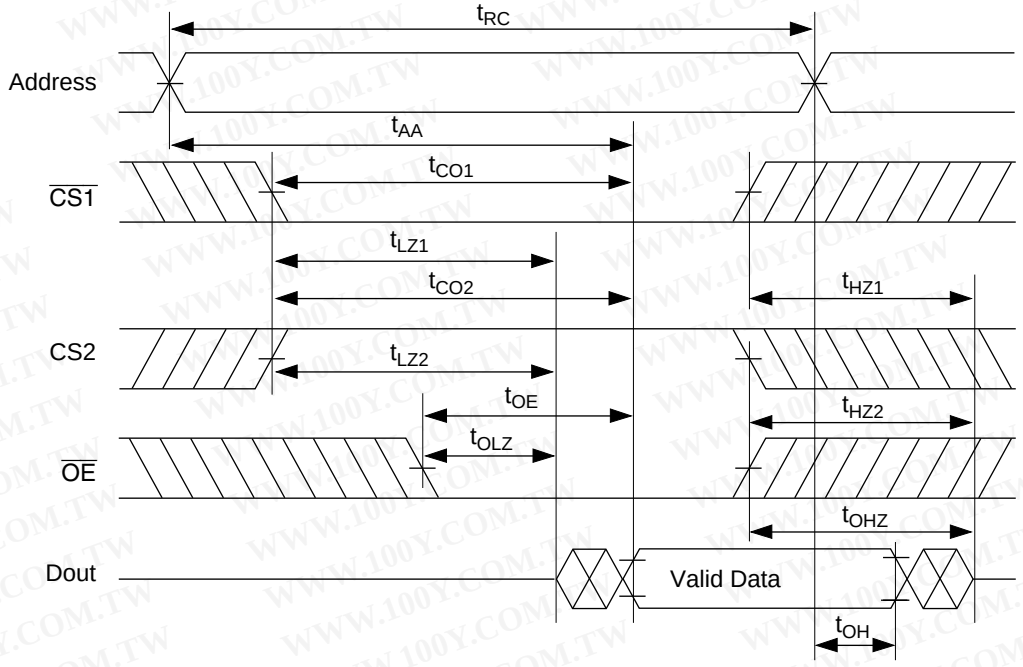
- Input pulse levels: 0.8 V/2.4 V
- Input rise and fall time: 10 ns
- Input timing reference level: 1.5 V
- Output timing reference level
  - — HM6264A-10: 1.5 V
  - — HM6264A-12/15: 0.8 V/2.0 V
- Output load: 1 TTL gate and C_L (100 pF) (including scope and jig)

Read Cycle

Parameter		Symbol	HM6264A-10 Min	HM6264A-10 Max	HM6264A-12 Min	HM6264A-12 Max	HM6264A-15 Min	HM6264A-15 Max	Unit
Read cycle time		t_{RC}	100	—	120	—	150	—	ns
Address access time		t_{AA}	—	100	—	120	—	150	ns
Chip selection to output	$\overline{CS1}$	t_{CO1}	—	100	—	120	—	150	ns
	CS2	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid		t_{OE}	—	50	—	60	—	70	ns
Chip selection to output in low Z	$\overline{CS1}$	t_{LZ1}	10	—	10	—	15	—	ns
	CS2	t_{LZ2}	10	—	10	—	15	—	ns
Output enable to output in low Z		t_{OLZ}	5	—	5	—	5	—	ns
Chip deselection to output in high Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output disable to output in high Z		t_{OHZ}	0	35	0	40	0	50	ns
Output hold from address change		t_{OH}	10	—	10	—	10	—	ns

Notes
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs to achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.

Read Timing Waveform

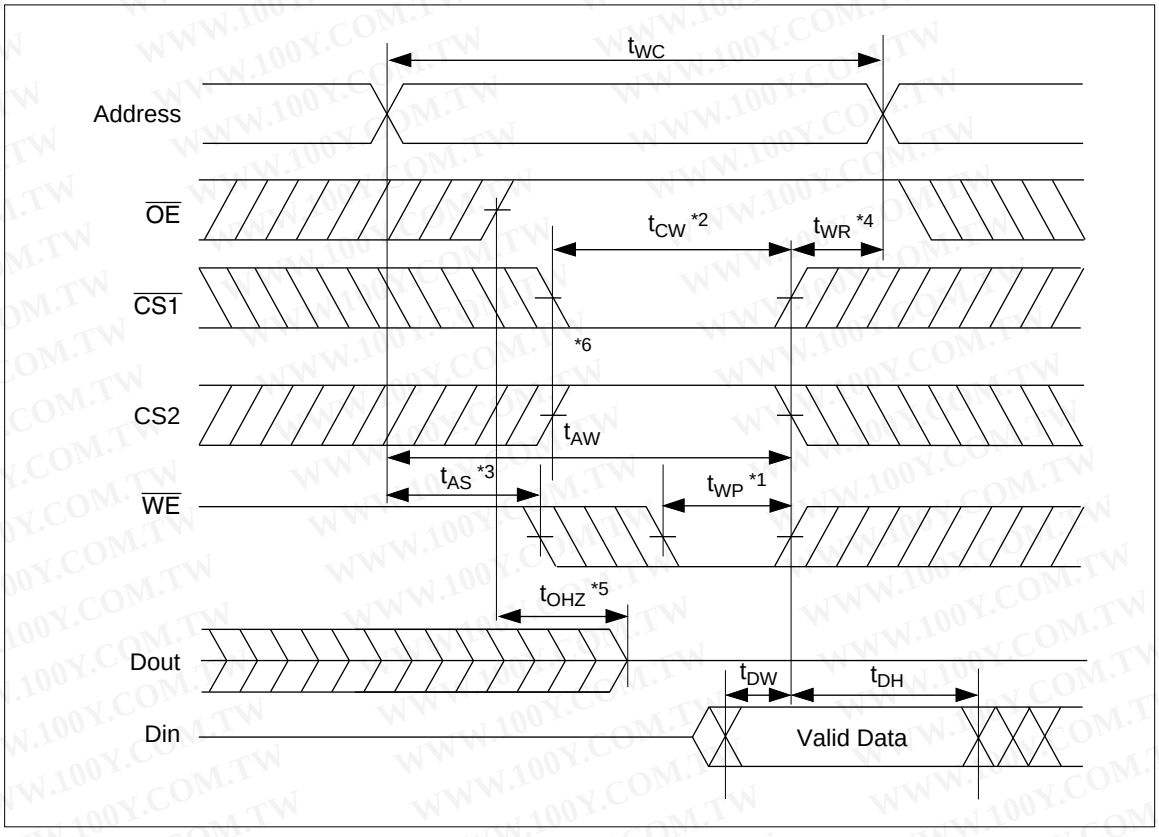


Note: $\overline{WE}$ is high for read cycle.

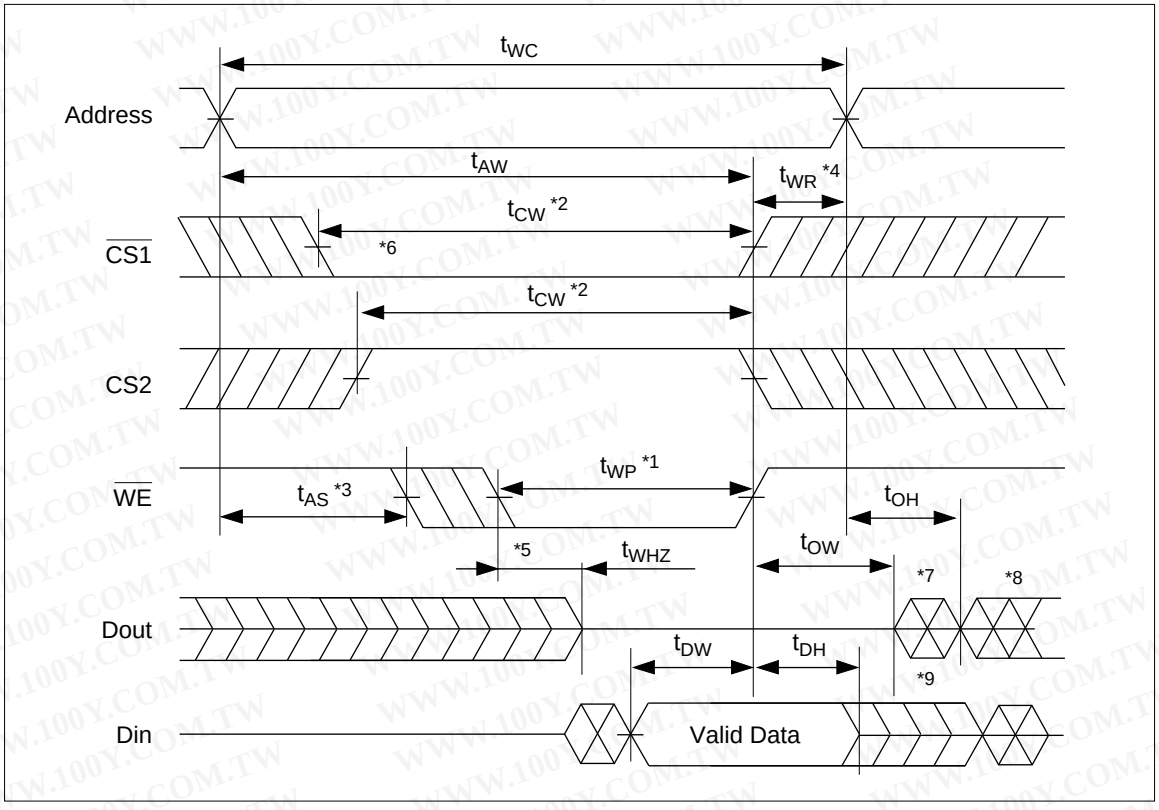
Write Cycle

Parameter	Symbol	HM6264A-10 Min	HM6264A-10 Max	HM6264A-12 Min	HM6264A-12 Max	HM6264A-15 Min	HM6264A-15 Max	Unit
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Chip selection to end of write	t_{CW}	80	—	85	—	100	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Address valid to end of write	t_{AW}	80	—	85	—	100	—	ns
Write pulse width	t_{WP}	60	—	70	—	90	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Write to output in high Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to write time overlap	t_{DW}	40	—	40	—	50	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output enable to output in high Z	t_{OHZ}	0	35	0	40	0	50	ns
Output active from end of write	t_{OW}	5	—	5	——	5	—	ns

Write Timing Waveform (1) (OE Clock)



Write Timing Waveform (2) (OE Low Fix)



Notes:
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. Time t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of the write cycle.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ goes low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of the next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Input signals of opposite phase to the outputs must not be applied to I/O pins

Low V_{CC} Data Retention

In data retention mode, CS2 controls the address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$, and the Din buffer. If CS2 controls data retention mode, Vin (for these inputs) can be in the high impedance state. If CS1 controls the data retention mode, CS2 must satisfy either $CS2 \geq V_{CC} - 0.2$ V or $CS2 \leq 0.2$ V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

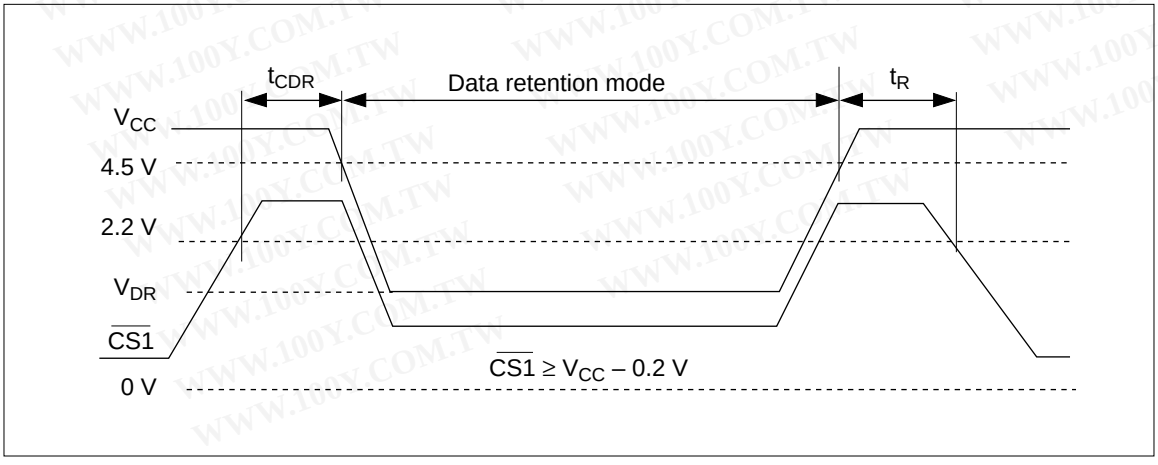
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only L/LL-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V, or $CS2 \leq 0.2$ V
Data retention current	I_{CCDR}	—	1*1	50*1	µA	V_{CC} = 3.0 V, $\overline{CS1} \geq V_{CC} - 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V, or 0 V ≤ CS2 ≤ 0.2 V, 0 V ≤ Vin
		—	1*2	25*2		
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*3	—	—	ns	See retention waveform

Notes: 1. V_{IL} min = –0.3 V, 20 µA max at Ta = 0 to 40°C. These characteristics are guaranteed only for the L-version.
2. V_{IL} min = –0.3 V, 10 µA max at Ta = 0 to 40°C. These characteristics are guaranteed only for the LL-version.
3. t_{RC} = Read cycle time.

Low V_{CC} Data Retention Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Waveform (2) ($\overline{CS2}$ Controlled)