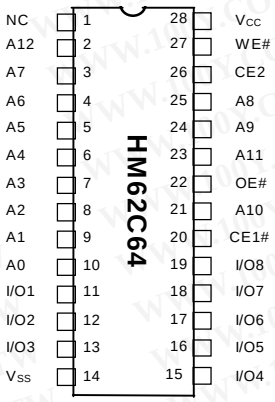
HM62C64

8K X 8 BIT CMOS SRAM

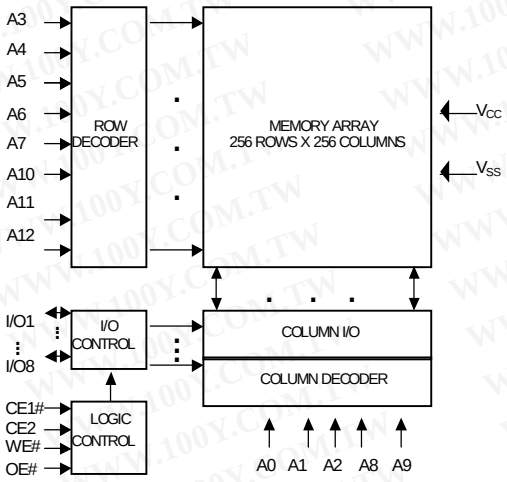
FEATURES

- Fast access time : 70 ns (max.)
- Low operating power consumption :
  1 μA (Typ.) standby
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention supply voltage: 2.0-5.5V
- Package : 28-pin 330 mil SOP
  28-pin 300 mil SOJ
  28-pin 300 mil DIP
  28-pin 600 mil DIP

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE1#, CE2	Chip Enable 1,2 Inputs
WE #	Write Enable Input
OE #	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

GENERAL DESCRIPTION

The HM62C64 is a 65,536-bit high-speed CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The HM62C64 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}	-0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	℃
Temperature Under Bias	T_{BIAS}	-10 to +85	℃
Storage Temperature	T_{STG}	-55 to +125	℃
Power Dissipation	P_T	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE1#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB},I_{SB1}
Standby	X	L	X	X	High -Z	I_{SB},I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	MIN.	TYPE	MAX.	UNIT
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	3.5	Vcc+0.2	V
Input Low Voltage	V_{IL}	- 0.3	0	0.8	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V± 10%, T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Supply Voltage	Vcc		4.5	5.5	
Supply Voltage	GND		0	0.2	
Input High Voltage	V_{IH}		3.5	0	V
Input Low Voltage	V_{IL}		- 0.3	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$	-	1	µA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ CE1# =V_{IH} or CE2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL}	-	1	µA
Output High Voltage	V_{OH}	I_{OH}= - 1mA	2.4	-	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA	-	0.4	V
Operating Power	I_{CC}	CE1# = V_{IL} , CE2=V_{IH} $I_{I/O}$ = 0mA ,Cycle=Min.	- -	30	mA
Standby Power Supply Current	I_{SB}	CE1# =V_{IH} or $I_{I/O}$ = 0mA	-	2	mA
	I_{SB1}	CE1#≧V_{CC}-0.2V or V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	-	5	µA

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=30pF, TTL Gate (see Fig.1 and Fig.2)

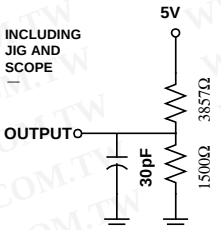


FIGURE 1A

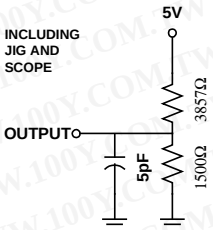


FIGURE 1B

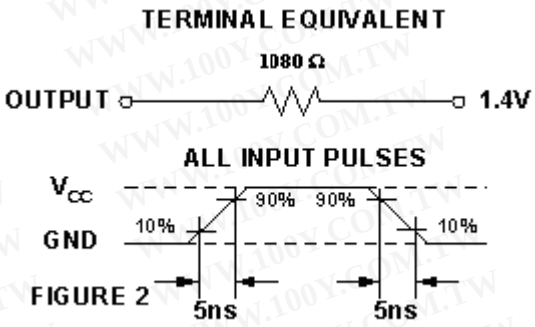


FIGURE 2

AC ELECTRICAL CHARACTERISTICS (VCC = 5V± 10% , TA = 0℃ to 70℃)

(1) READ CYCLE

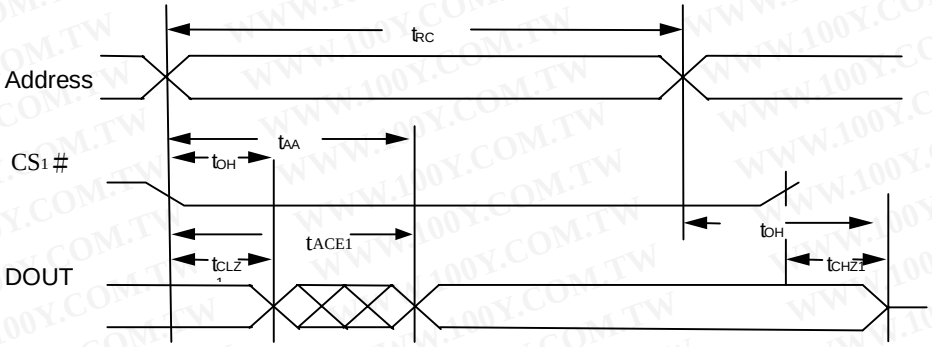
PARAMETER	SYMBOL	HM62C64-70LL		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	70	-	ns
Address Access Time	t_{AA}	-	70	ns
Chip Enable Access Time	t_{ACE1}, t_{ACE2}	-	70	ns
Output Enable Access Time	t_{OE}	-	50	ns
Chip Enable to Output in Low-Z	t_{CLZ1}, t_{CLZ2}	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ1}, t_{CHZ2}	0	35	ns
Output Disable to Output in High-Z	t_{OHZ}	0	30	ns
Output Hold from Address Change	t_{OH}	10	-	ns

(2) WRITE CYCLE

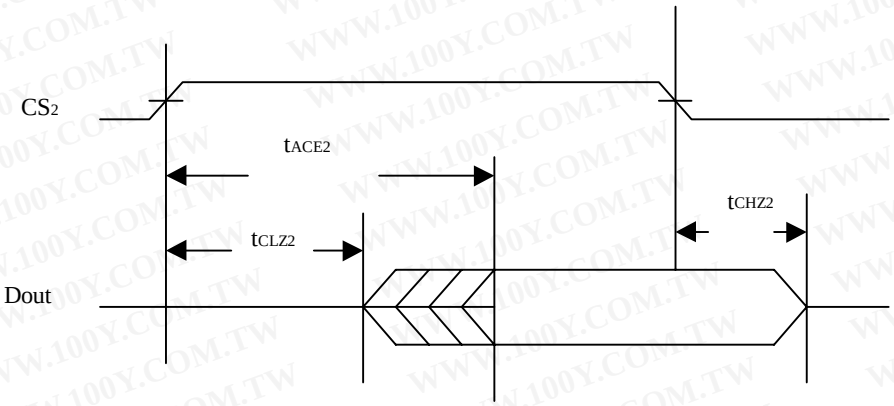
PARAMETER	SYMBOL	HM62C64-70LL		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	70	-	ns
Address Valid to End of Write	t_{AW}	70	-	ns
Chip Enable to End of Write	t_{CW1}, t_{CW2}	70	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	50	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	30	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}	5	-	ns
Write to Output in High-Z	t_{WHZ}	0	35	ns
OE to Output in High-Z	t_{OHZ}	0	30	ns

TIMING WAVEFORMS

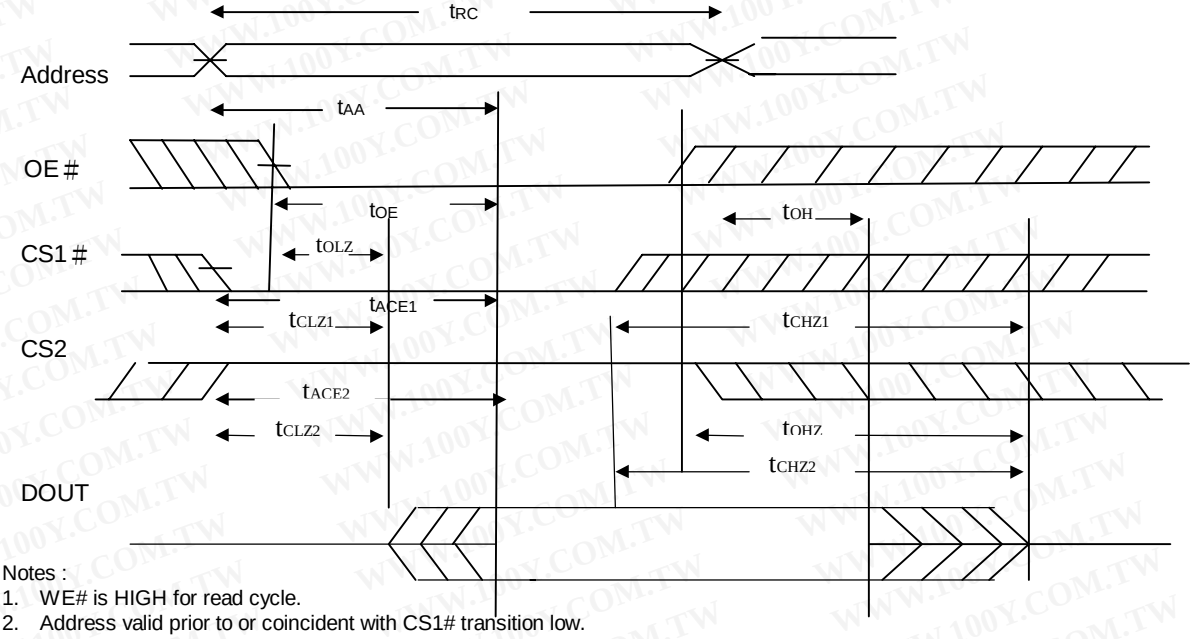
READ CYCLE 1 (1,2,3, 5)



READ CYCLE 2 (1,3, 6, 7)

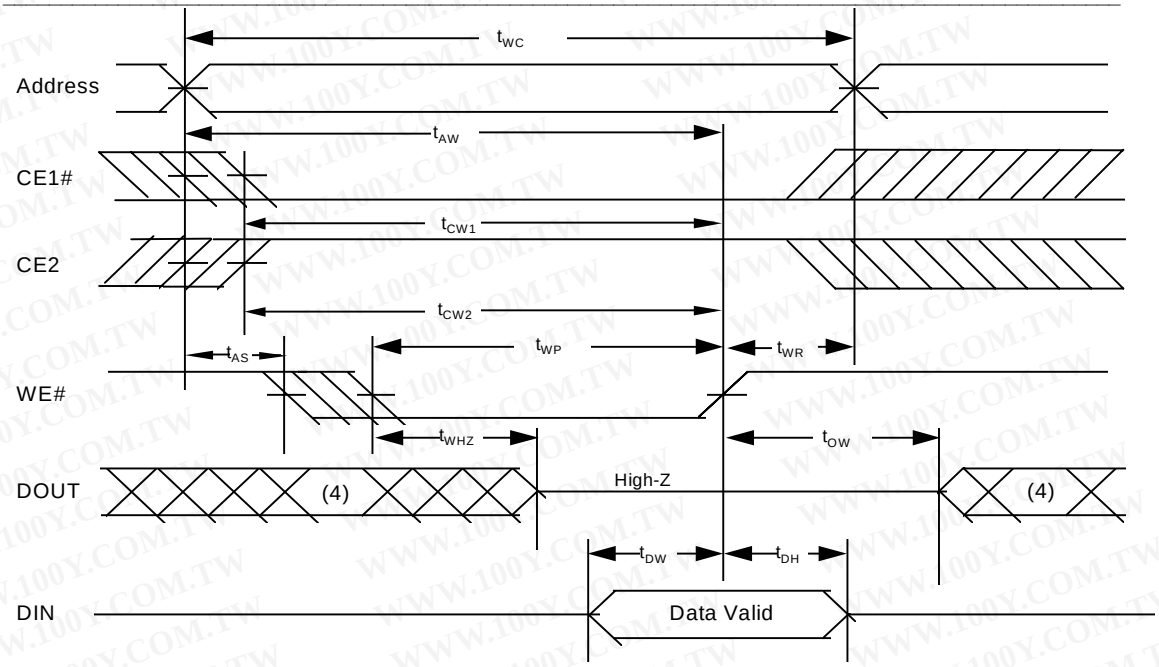


READ CYCLE 3 (1,8)

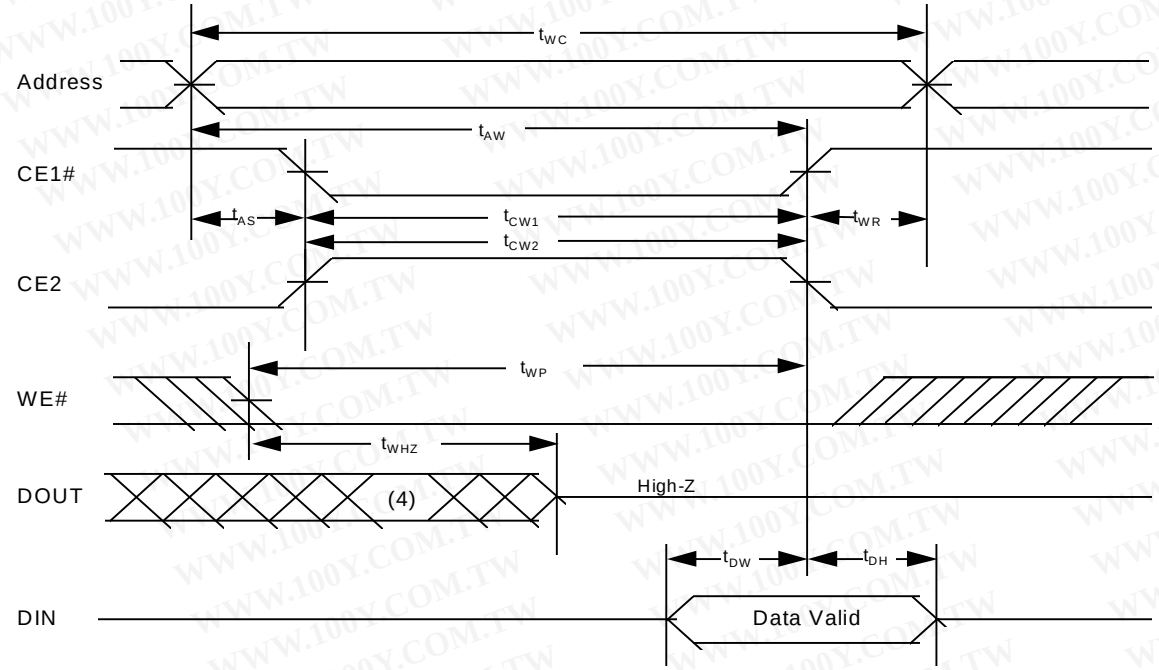


Notes :
1. WE# is HIGH for read cycle.
2. Address valid prior to or coincident with CS1# transition low.
3. OE# = V_{IL}.
4. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
5. CS_2 is high.
6. CS_1# is low.
7. Address valid prior to or coincident with CS_2 transition high.
8. Chip select signal must be format for read cycle.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5)



WRITE CYCLE 2 (CE1# and CE2 Controlled) (1,2,5)



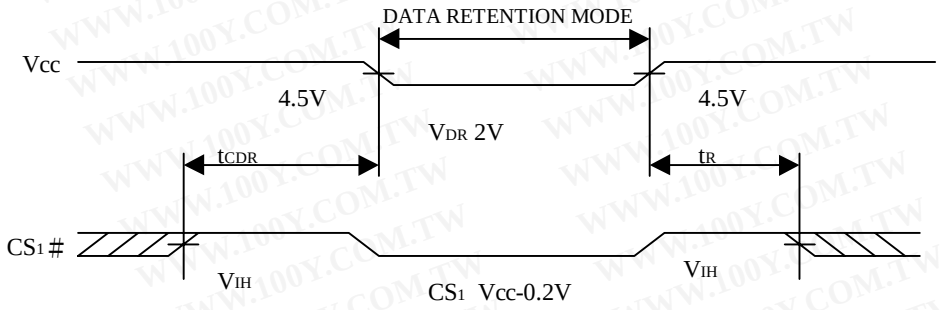
Notes :
1. t_{AS} is measured from the address valid to the beginning of write.
2. A write occurs during the overlap of a low CS1#, a high CS2 and a low WE#.
3. t_{WR} is measured from the earlier of CS1#or WE# going high or CS2 to the end of write cycle.
4. During this period, I/O pins are in the output state so that the data input singals to the outputs must not be applied.
5. If the CS1# LOW transition or the CS2 transition occurs simultaneously with the WE# low transitions or after the WE# transition, outputs remain in a high impedance state.
6. OE# is contiuously low (OE#=V_{IL}).
7. Dout is the same phase of write data of this write cyele.
8. Dout is the read data of next address.
9. If CS1# is low and CS2 is high during this period, I/O pins are in the output state. Then the data input signals to the outputs must not be applied to I/O pins.
10. Transition is measured ±500mV from steady state. This parameter is sampled and 100%tested.
11. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.

DTAT RETENTION CHARACTERISTICS

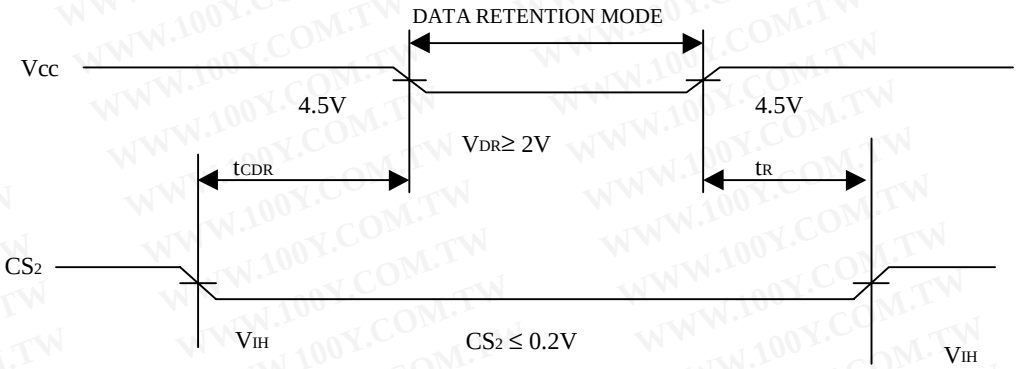
PARAMETER	SYMBOL	HM62C64-70LL		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Vcc for Data Retention	V_{DR1}	2.0	5.5	V	$CS_1 \geq Vcc-02.V$, $V_{IN} \geq V_{CC}-0.2$ $V_{IN} \leq 0.2V$
	V_{DR2}	2.0	5.5	V	$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$, o $V_{IN} \leq 0.2V$
Data retention Current	I_{CCDR1}	-	5	µA	$CS_1 \geq Vcc-02.V$, $V_{IN} \geq V_{CC}-0.2$ $V_{IN} \leq 0.2V$
	I_{CCDR2}	-	5	µA	$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$, o $V_{IN} \leq 0.2V$
Chip Deselect to Data Retention Time	t_{CDR}	0	-	ns	See Retention
Operation Recovery Time	t_R	t_{RC}	-	ns	Waveform

1. V_{CC}=2V, T_A=+25°C
2. t_{RC}=Read Cycle Time

LOW VCC DATA RETENTION WAVEFORM (CS1# CONTROLLED)



LOW VCC DATA RETENTION WAVEFORM (CS2# CONTROLLED)



ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
HM62C64J-70LL	70	28PIN SOJ
HM62C64S-70LL	70	28PIN SOP
HM62C64K-70LL	70	28PIN 300 mil DIP
HM62C64P-70LL	70	28PIN 600 mil DIP

Lot No: X X X X X X X X X
① ②

① : Manufacturing tracking code

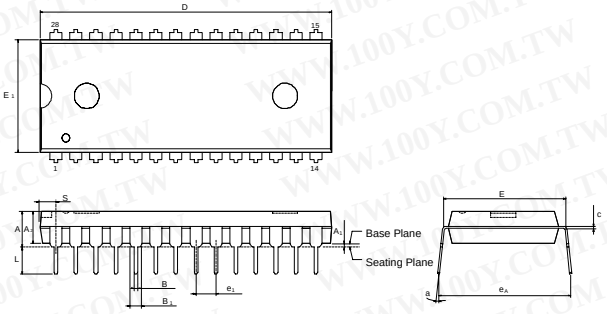
② — : Normal package

R : Lead free package

G : Green (RoHS compatible) package

PACKAGE DIMENSIONS

28-pin P-DIP

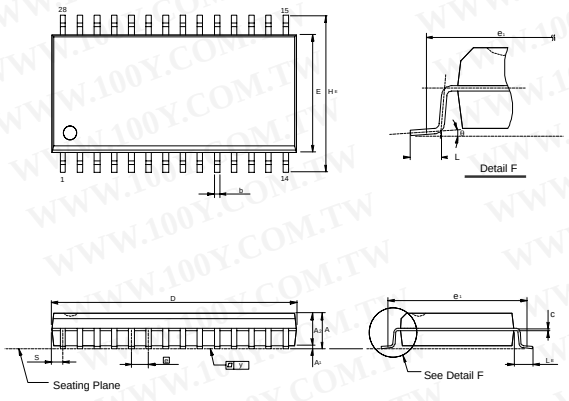


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.460	1.470	—	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

28-pin SOP Wide Body



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.112	—	—	2.85
A_1	0.004	—	—	0.10	—	—
A_2	0.093	0.098	0.103	2.36	2.49	2.62
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.713	0.733	—	18.11	18.62
E	0.326	0.331	0.336	8.28	8.41	8.53
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L_E	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.