



Integrated Device Technology, Inc.

CMOS SyncFIFO™
256 x 18, 512 x 18, 1,024 x 18,
2,048 x 18 and 4,096 x 18

IDT72205LB
IDT72215LB
IDT72225LB
IDT72235LB
IDT72245LB

FEATURES:

- 256 x 18-bit organization array (IDT72205LB)
- 512 x 18-bit organization array (IDT72215LB)
- 1,024 x 18-bit organization array (IDT72225LB)
- 2,048 x 18-bit organization array (IDT72235LB)
- 4,096 x 18-bit organization array (IDT72245LB)
- 10 ns read/write cycle time
- Empty and Full flags signal FIFO status
- Easily expandable in depth and width
- Asynchronous or coincident read and write clocks
- Programmable Almost-Empty and Almost-Full flags with default settings
- Half-Full flag capability
- Dual-Port zero fall-through time architecture
- Output enable puts output data bus in high-impedance state
- High-performance submicron CMOS technology
- Available in a 64-lead thin quad flatpack (TQFP/STQFP) and plastic leaded chip carrier (PLCC)
- Industrial temperature range (-40°C to +85°C) is available

DESCRIPTION:

The IDT72205LB/72215LB/72225LB/72235LB/72245LB are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. These FIFOs

are applicable for a wide variety of data buffering needs, such as optical disk controllers, Local Area Networks (LANs), and interprocessor communication.

These FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and an input enable pin (WEN). Data is read into the synchronous FIFO on every clock when WEN is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin (REN). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An Output Enable pin (OE) is provided on the read port for three-state control of the output.

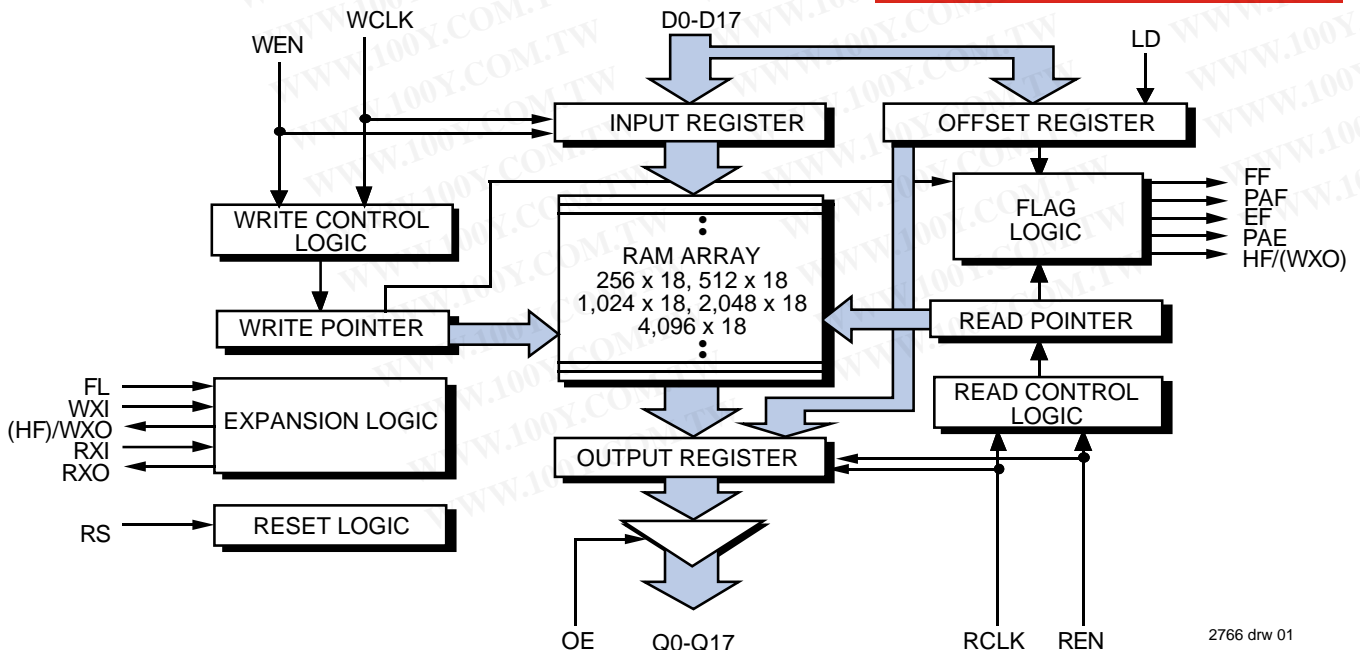
The synchronous FIFOs have two fixed flags, Empty (EF) and Full (FF), and two programmable flags, Almost-Empty (PAE) and Almost-Full (PAF). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the Load pin (LD). A Half-Full flag (HF) is available when the FIFO is used in a single device configuration.

These devices are depth expandable using a Daisy-Chain technique. The XI and XO pins are used to expand the FIFOs. In depth expansion configuration, FL is grounded on the first device and set to HIGH for all other devices in the Daisy Chain.

The IDT72205LB/72215LB/72225LB/72235LB/72245LB is fabricated using IDT's high-speed submicron CMOS technology.

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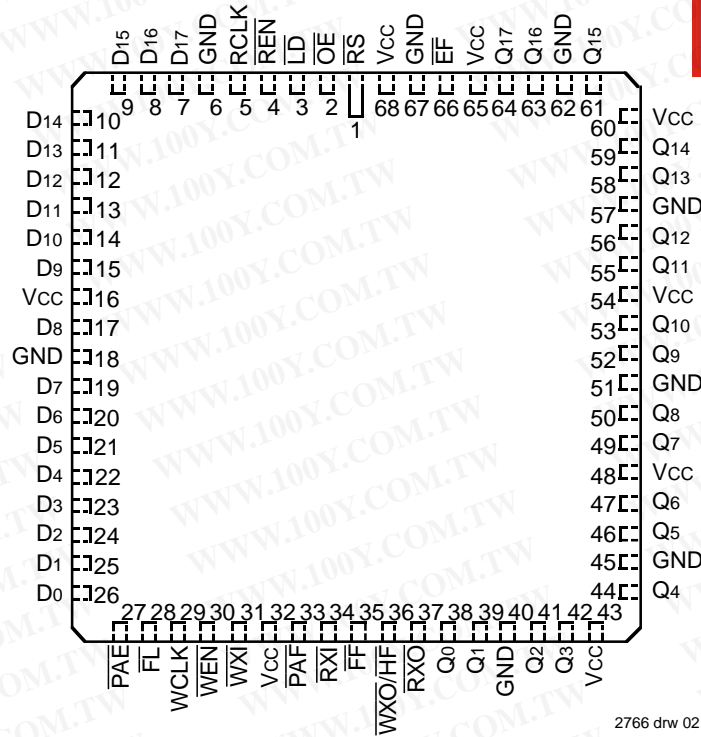
FUNCTIONAL BLOCK DIAGRAM



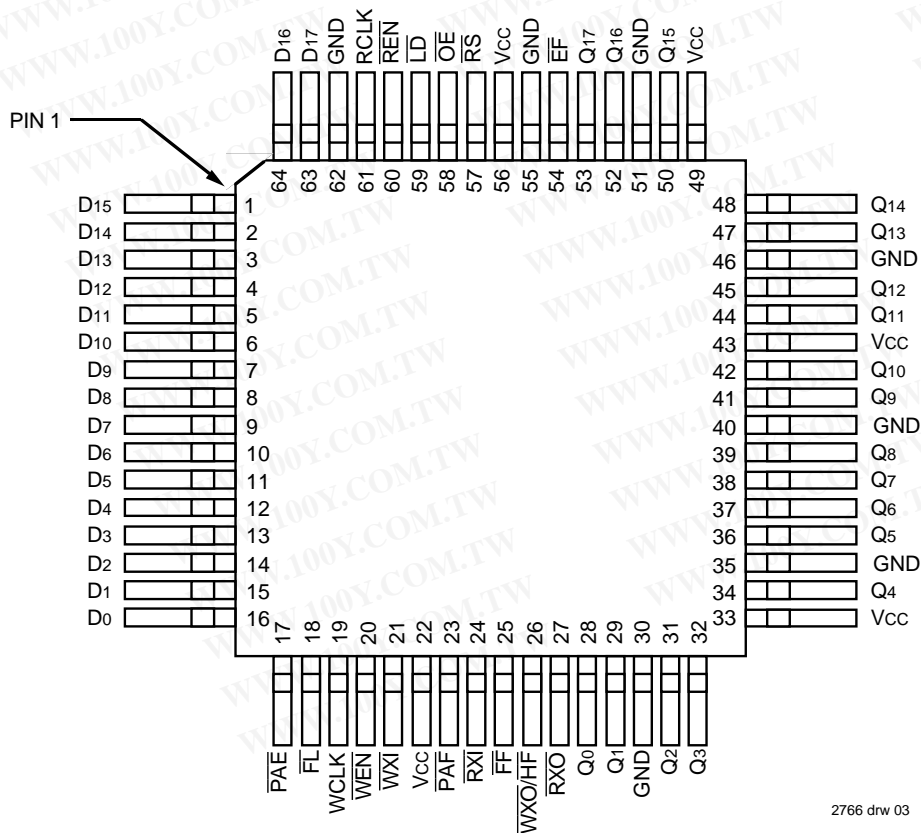
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PIN CONFIGURATIONS



PLCC (J68-1, order code: J)
 TOP VIEW



TQFP (PN64-1, order code: PF)
 STQFP (PP64-1, order code: TF)
 TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D0–D17	Data Inputs	I	Data inputs for a 18-bit bus.
\overline{RS}	Reset	I	When \overline{RS} is set LOW, internal read and write pointers are set to the first location of the RAM array, \overline{FF} and \overline{PAF} go HIGH, and \overline{PAE} and \overline{EF} go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	When \overline{WEN} is LOW, data is written into the FIFO on a LOW-to-HIGH transition of WCLK, if the FIFO is not full.
\overline{WEN}	Write Enable	I	When \overline{WEN} is LOW and \overline{LD} is HIGH, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When \overline{WEN} is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the \overline{FF} is LOW.
RCLK	Read Clock	I	When \overline{REN} is LOW, data is read from the FIFO on a LOW-to-HIGH transition of RCLK, if the FIFO is not empty.
\overline{REN}	Read Enable	I	When \overline{REN} is LOW and \overline{LD} is HIGH, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When \overline{REN} is HIGH, the output register holds the previous data. Data will not be read from the FIFO if the \overline{EF} is LOW.
\overline{OE}	Output Enable	I	When \overline{OE} is LOW, the data output bus is active. If \overline{OE} is HIGH, the output data bus will be in a high-impedance state.
\overline{LD}	Load	I	When \overline{LD} is LOW, data on the inputs D0–D11 is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when \overline{WEN} is LOW. When \overline{LD} is LOW, data on the outputs Q0–Q11 is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when \overline{REN} is LOW.
\overline{FL}	First Load	I	In the single device or width expansion configuration, \overline{FL} is grounded. In the depth expansion configuration, \overline{FL} is grounded on the first device (first load device) and set to HIGH for all other devices in the Daisy Chain.
\overline{WXI}	Write Expansion	I	In the single device or width expansion configuration, \overline{WXI} is grounded. In the depth expansion configuration, \overline{WXI} is connected to \overline{WXO} (Write Expansion Out) of the previous device.
\overline{RXI}	Read Expansion	I	In the single device or width expansion configuration, \overline{RXI} is grounded. In the depth expansion configuration, \overline{RXI} is connected to \overline{RXO} (Read Expansion Out) of the previous device.
\overline{FF}	Full Flag	O	When \overline{FF} is LOW, the FIFO is full and further data writes into the input are inhibited. When \overline{FF} is HIGH, the FIFO is not full. \overline{FF} is synchronized to WCLK.
\overline{EF}	Empty Flag	O	When \overline{EF} is LOW, the FIFO is empty and further data reads from the output are inhibited. When \overline{EF} is HIGH, the FIFO is not empty. \overline{EF} is synchronized to RCLK.
\overline{PAE}	Programmable Almost-Empty Flag	O	When \overline{PAE} is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 31 from empty for IDT72205LB, 63 from empty for IDT72215LB, and 127 from empty for IDT72225LB/72235LB/72245LB.
\overline{PAF}	Programmable Almost-Full Flag	O	When \overline{PAF} is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 31 from full for IDT72205LB, 63 from full for IDT72215LB, and 127 from full for IDT72225LB/72235LB/72245LB.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when \overline{HF} is LOW. In the depth expansion configuration, a pulse is sent from \overline{WXO} to \overline{WXI} of the next device when the last location in the FIFO is written.
\overline{RXO}	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from \overline{RXO} to \overline{RXI} of the next device when the last location in the FIFO is read.
Q0–Q17	Data Outputs	O	Data outputs for a 18-bit bus.
Vcc	Power		+5V power supply pins.
GND	Ground		Eight ground pins for the PLCC and seven pins for the TQFP/STQFP.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Unit
VTERM	Terminal Voltage with respect to GND	-0.5 to +7.0	V
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	-50 to +50	mA

NOTE: 2766 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage Com'l/Ind'l	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Com'l/Ind'l	2.0	—	—	V
VIL ⁽¹⁾	Input Low Voltage Com'l/Ind'l	—	—	0.8	V
TA	Operating Temperature Commercial	0	—	70	°C
TA	Operating Temperature Industrial	-40	—	85	°C

NOTE: 2766 tbl 03
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Industrial: VCC = 5V ± 10%, TA = -40°C to +85°C)

Symbol	Parameter	IDT72205LB IDT72215LB IDT72225LB IDT72235LB IDT72245LB Commercial and Industrial ⁽¹⁾ tCLK = 10, 15, 25 ns			Unit
		Min.	Typ.	Max.	
ILI ⁽²⁾	Input Leakage Current (any input)	-1	—	1	μA
ILO ⁽³⁾	Output Leakage Current	-10	—	10	μA
VOH	Output Logic "1" Voltage, IOH = -2 mA	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	V
ICC1 ^(4,5,6)	Active Power Supply Current	—	—	60	mA
ICC2 ^(4,7)	Standby Current	—	—	5	mA

NOTES: 2766 tbl 04
1. Industrial temperature range product for the 25 ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
3. $\overline{OE} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
4. Tested with outputs open (IOUT = 0).
5. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
6. For the 72205/72215/72225 the typical ICC1 = 1.81 + 1.12*fs + 0.02*CL*fs (in mA); for the 72235/72245 the typical ICC1 = 2.85 + 1.30*fs + 0.02*CL*fs (in mA). These equations are valid under the following conditions: VCC = 5V, TA = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, CL = capacitive load (in pF).
7. All Inputs = Vcc - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN ⁽²⁾	Input Capacitance	VIN = 0V	10	pF
COU ^(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTES: 2766 tbl 05
1. With output deselected, ($\overline{OE} \geq V_{IH}$).
2. Characterized values, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2766 tbl 06

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AC ELECTRICAL CHARACTERISTICS

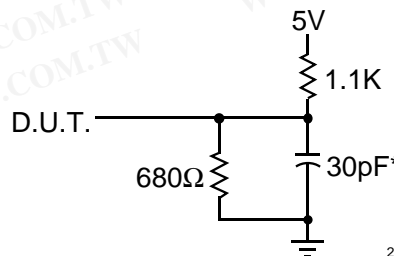
(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Industrial: VCC = 5V ± 10%, TA = -40°C to +85°C)

Symbol	Parameter	Commercial				Com'l & Ind'l ⁽¹⁾			Unit
		72205LB10		72205LB15		72205LB25			
		Min.	Max.	Min.	Max.	Min.	Max.		
fs	Clock Cycle Frequency	—	100	—	66.7	—	40	MHz	
tA	Data Access Time	2	6.5	2	10	2	15	ns	
tCLK	Clock Cycle Time	10	—	15	—	25	—	ns	
tCLKH	Clock HIGH Time	4.5	—	6	—	10	—	ns	
tCLKL	Clock LOW Time	4.5	—	6	—	10	—	ns	
tDS	Data Set-up Time	3	—	4	—	6	—	ns	
tDH	Data Hold Time	0	—	1	—	1	—	ns	
tENS	Enable Set-up Time	3	—	4	—	6	—	ns	
tENH	Enable Hold Time	0	—	1	—	1	—	ns	
trS	Reset Pulse Width ⁽²⁾	10	—	15	—	25	—	ns	
trSS	Reset Set-up Time	8	—	10	—	15	—	ns	
trSR	Reset Recovery Time	8	—	10	—	15	—	ns	
trSF	Reset to Flag and Output Time	—	15	—	20	—	25	ns	
toLZ	Output Enable to Output in Low-Z ⁽³⁾	0	—	0	—	0	—	ns	
toE	Output Enable to Output Valid	3	6	3	8	3	12	ns	
toHZ	Output Enable to Output in High-Z ⁽³⁾	3	6	3	8	3	12	ns	
twFF	Write Clock to Full Flag	—	6.5	—	10	—	15	ns	
tREF	Read Clock to Empty Flag	—	6.5	—	10	—	15	ns	
tPAF	Clock to Programmable Almost-Full Flag	—	17	—	24	—	26	ns	
tPAE	Clock to Programmable Almost-Empty Flag	—	17	—	24	—	26	ns	
tHF	Clock to Half-Full Flag	—	17	—	24	—	26	ns	
txO	Clock to Expansion Out	—	6.5	—	10	—	15	ns	
txI	Expansion In Pulse Width	3	—	6.5	—	10	—	ns	
txIS	Expansion In Set-Up Time	3.5	—	5	—	10	—	ns	
tsKEW1	Skew time between Read Clock & Write Clock for Full Flag	5	—	6	—	10	—	ns	
tsKEW2	Skew time between Read Clock & Write Clock for Empty Flag	5	—	6	—	10	—	ns	

NOTES:

1. Industrial temperature range is available by special order for speed grades faster than 25ns.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.

2766 tbl 07



2766 drw 04

Figure 1. Output Load

* Includes jig and scope capacitances.

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SIGNAL DESCRIPTIONS:

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INPUTS:

DATA IN (D0 - D17)

Data inputs for 18-bit wide data.

CONTROLS:

RESET (\overline{RS})

Reset is accomplished whenever the Reset (\overline{RS}) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag (\overline{FF}), Half-Full Flag (\overline{HF}) and Programmable Almost-Full Flag (\overline{PAF}) will be reset to HIGH after t_{RSF} . The Empty Flag (\overline{EF}) and Programmable Almost-Empty Flag (\overline{PAE}) will be reset to LOW after t_{RSF} . During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

WRITE CLOCK (WCLK)

A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

WRITE ENABLE (\overline{WEN})

When the \overline{WEN} input is LOW and \overline{LD} input is HIGH, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When \overline{WEN} is HIGH, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow, \overline{FF} will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, \overline{FF} will go HIGH allowing a write to occur. The \overline{FF} flag is updated on the rising edge of WCLK. \overline{WEN} is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK), when Output Enable (\overline{OE}) is set LOW.

The write and read clocks can be asynchronous or coincident.

READ ENABLE (\overline{REN})

When Read Enable is LOW and \overline{LD} input is HIGH, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When the \overline{REN} input is HIGH, the output register holds the previous data and no new data is loaded into the output register. The data outputs Q0-Qn maintain the previous data value.

Every word accessed at Qn, including the first word written to an empty FIFO, must be requested using \overline{REN} . When the last word has been read from the FIFO, the Empty Flag (\overline{EF}) will go LOW, inhibiting further read operations. \overline{REN} is ignored when the FIFO is empty. Once a write is performed, \overline{EF} will go HIGH allowing a read to occur. The \overline{EF} flag is updated on the rising edge of RCLK.

OUTPUT ENABLE (\overline{OE})

When Output Enable (\overline{OE}) is enabled (LOW), the parallel output buffers receive data from the output register. When \overline{OE} is disabled (HIGH), the Q output data bus is in a high-impedance state.

LOAD (\overline{LD})

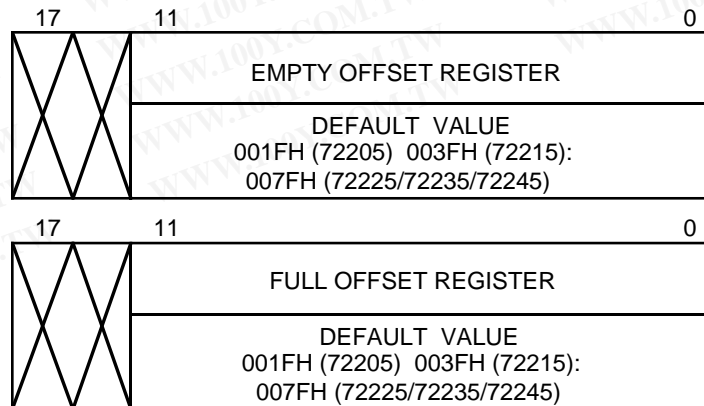
The IDT72205LB/72215LB/72225LB/72235LB/72245LB devices contain two 12-bit offset registers with data on the inputs, or read on the outputs. When the Load (\overline{LD}) pin is set LOW and \overline{WEN} is set LOW, data on the inputs D0-D11 is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the \overline{LD} pin and (\overline{WEN}) are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the \overline{LD} pin HIGH, the FIFO is returned to normal read/write operation. When the LD pin is set LOW, and \overline{WEN} is LOW, the next offset register in sequence is written.

\overline{LD}	\overline{WEN}	WCLK	Selection
0	0		Writing to offset registers: Empty Offset Full Offset
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

NOTE: 2766 tbl 08
 1. The same selection sequence applies to reading from the registers. \overline{REN} is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register



NOTE: 2766 drw 05
 1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

When the \overline{LD} pin is LOW and \overline{WEN} is HIGH, the WCLK input is disabled; then a signal at this input can neither increment the write offset register pointer, nor execute a write.

The contents of the offset registers can be read on the output lines when the \overline{LD} pin is set LOW and \overline{REN} is set LOW; then, data can be read on the LOW-to-HIGH transition of the read clock (RCLK). The act of reading the control registers employs a dedicated read offset register pointer. (The read and write pointers operate independently).

A read and a write should not be performed simultaneously to the offset registers.

FIRST LOAD (\overline{FL})

\overline{FL} is grounded to indicate operation in the Single Device or Width Expansion mode. In the Depth Expansion configuration, \overline{FL} is grounded to indicate it is the first device loaded and is set to HIGH for all other devices in the Daisy Chain. (See Operating Configurations for further details.)

WRITE EXPANSION INPUT (\overline{WXI})

This is a dual purpose pin. \overline{WXI} is grounded to indicate operation in the Single Device or Width Expansion mode. \overline{WXI} is connected to Write Expansion Out (\overline{WXO}) of the previous device in the Daisy Chain Depth Expansion mode.

READ EXPANSION INPUT (\overline{RXI})

This is a dual purpose pin. \overline{RXI} is grounded to indicate operation in the Single Device or Width Expansion mode. \overline{RXI} is connected to Read Expansion Out (\overline{RXO}) of the previous device in the Daisy Chain Depth Expansion mode.

OUTPUTS:

FULL FLAG (\overline{FF})

When the FIFO is full, \overline{FF} will go LOW, inhibiting further write operations. When \overline{FF} is HIGH, the FIFO is not full. If no reads are performed after a reset, \overline{FF} will go LOW after D writes to the FIFO. D = 256 writes for the IDT72205LB, 512 for the IDT72215LB, 1,024 for the IDT72225LB, 2,048 for the IDT72235LB and 4,096 for the IDT72245LB.

The \overline{FF} is updated on the LOW-to-HIGH transition of the write clock (WCLK).

EMPTY FLAG (\overline{EF})

When the FIFO is empty, \overline{EF} will go LOW, inhibiting further read operations. When \overline{EF} is HIGH, the FIFO is not empty.

The \overline{EF} is updated on the LOW-to-HIGH transition of the read clock (RCLK).

PROGRAMMABLE ALMOST-FULL FLAG (\overline{PAF})

The Programmable Almost-Full Flag (\overline{PAF}) will go LOW when FIFO reaches the Almost-Full condition. If no reads are performed after Reset (\overline{RS}), the \overline{PAF} will go LOW after (256-m) writes for the IDT72205LB, (512-m) writes for the IDT72215LB, (1,024-m) writes for the IDT72225LB, (2,048-m) writes for the IDT72235LB and (4,096-m) writes for the IDT72245LB. The offset "m" is defined in the FULL offset register.

If there is no Full offset specified, the \overline{PAF} will be LOW when the device is 31 away from completely full for IDT72205LB, 63 away from completely full for IDT72215LB, and 127 away from completely full for IDT72225LB/72235LB/72245LB.

The \overline{PAF} is asserted LOW on the LOW-to-HIGH transition of the write clock (WCLK). \overline{PAF} is reset to HIGH on the LOW-to-HIGH transition of the read clock (RCLK). Thus \overline{PAF} is asynchronous.

PROGRAMMABLE ALMOST-EMPTY FLAG (\overline{PAE})

The Programmable Almost-Empty Flag (\overline{PAE}) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the EMPTY offset register.

If there is no Empty offset specified, the Programmable Almost-Empty Flag (\overline{PAE}) will be LOW when the device is 31 away from completely empty for IDT72205LB, 63 away from completely empty for IDT72215LB, and 127 away from completely empty for IDT72225LB/72235LB/72245LB.

The \overline{PAE} is asserted LOW on the LOW-to-HIGH transition of the read clock (RCLK). \overline{PAE} is reset to HIGH on the LOW-to-HIGH transition of the write clock (WCLK). Thus \overline{PAE} is asynchronous.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO/HF}$)

This is a dual-purpose output. In the Single Device and Width Expansion mode, when Write Expansion In (\overline{WXI}) and Read Expansion In (\overline{RXI}) are grounded, this output acts as an indication of a half-full memory.

TABLE I — STATUS FLAGS

Number of Words in FIFO Memory					\overline{FF}	\overline{PAF}	\overline{HF}	\overline{PAE}	\overline{EF}
72205	72215	72225	72235	72245					
0	0	0	0	0	H	H	H	L	L
1 to n ⁽¹⁾	1 to n ⁽¹⁾	1 to n ⁽¹⁾	1 to n ⁽¹⁾	1 to n ⁽¹⁾	H	H	H	L	H
(n + 1) to 128	(n + 1) to 256	(n + 1) to 512	(n + 1) to 1,024	(n + 1) to 2,048	H	H	H	H	H
129 to (256-(m+1))	257 to (512-(m+1))	513 to (1,024-(m+1))	1,025 to (2,048-(m+1))	2,049 to (4,096-(m+1))	H	H	L	H	H
(256-m) ⁽²⁾ to 255	(512-m) ⁽²⁾ to 511	(1,024-m) ⁽²⁾ to 1,023	(2,048-m) ⁽²⁾ to 2,047	(4,096-m) ⁽²⁾ to 4,095	H	L	L	H	H
256	512	1,024	2,048	4,096	L	L	L	H	H

NOTES:

- n = Empty Offset (Default Values : IDT72205 n=31, IDT72215 n = 63, IDT72225/72235/72245 n = 127)
- m = Full Offset (Default Values : IDT72205 n=31, IDT72215 n = 63, IDT72225/72235/72245 n = 127)

2766 tbl 09

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After half of the memory is filled, and at the LOW-to-HIGH transition of the next write cycle, the Half-Full Flag goes LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag (HF) is then reset to HIGH by the LOW-to-HIGH transition of the read clock (RCLK). The HF is asynchronous.

In the Daisy Chain Depth Expansion mode, \overline{WXI} is connected to \overline{WXO} of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device writes to the last location of memory.

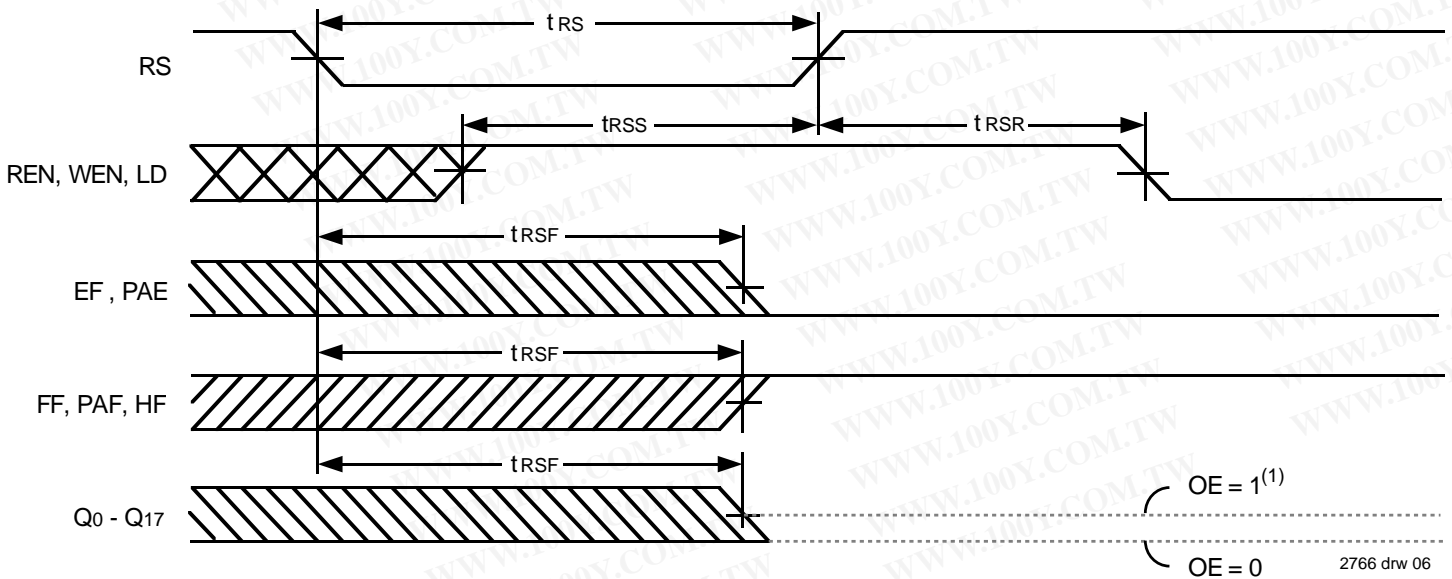
READ EXPANSION OUT (\overline{RXO})

In the Daisy Chain Depth Expansion configuration, Read Expansion In (RXI) is connected to Read Expansion Out (\overline{RXO}) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device reads from the last location of memory.

DATA OUTPUTS (Q0-Q17)

Q0-Q17 are data outputs for 18-bit wide data.

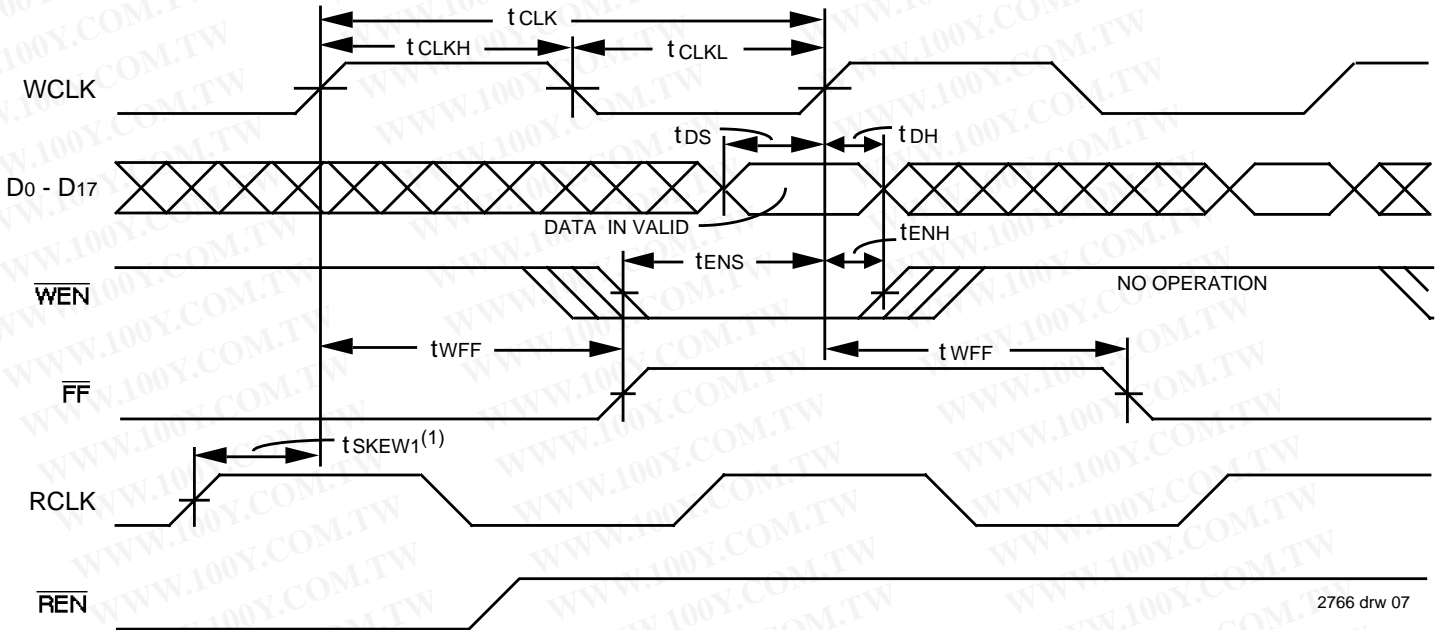
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NOTES:

1. After reset, the outputs will be LOW if $\overline{OE} = 0$ and tri-state if $\overline{OE} = 1$.
2. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 4. Reset Timing⁽²⁾



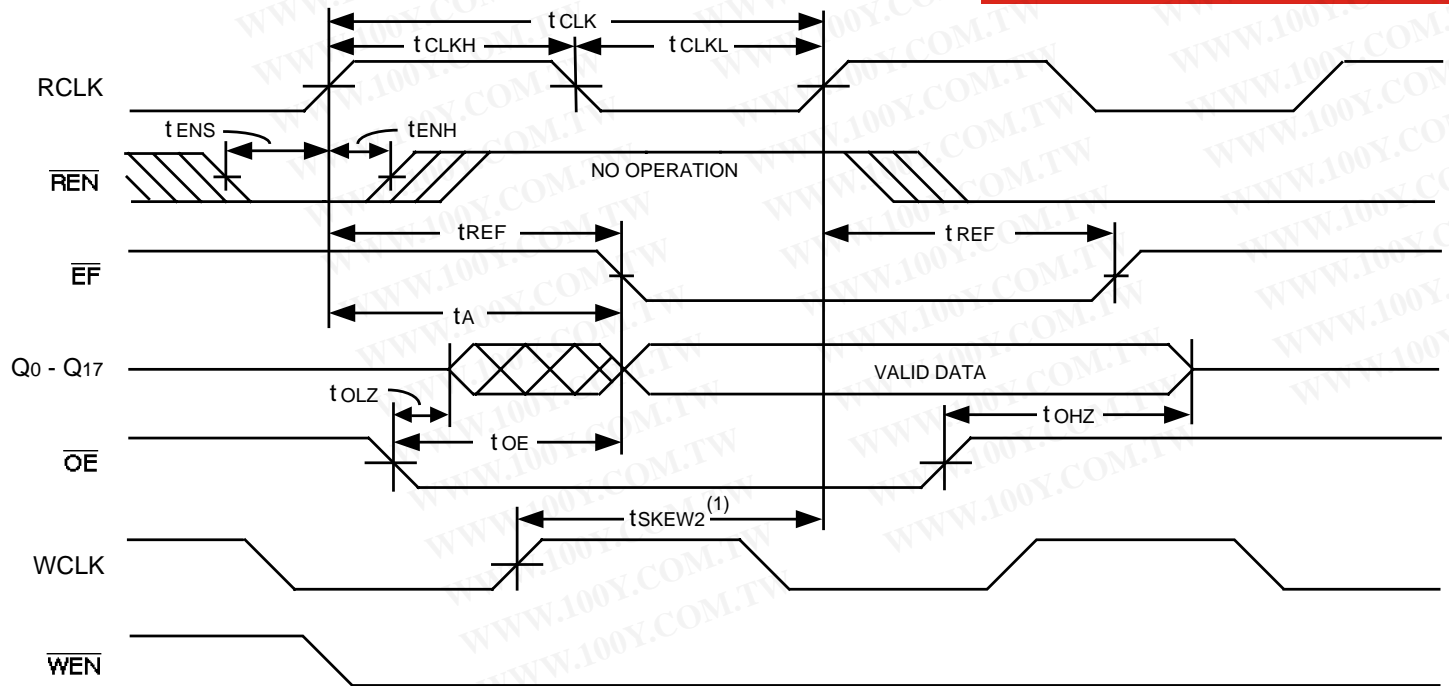
2766 drw 07

NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that \overline{FF} will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1} , then \overline{FF} may not change state until the next WCLK edge.

Figure 5. Write Cycle Timing

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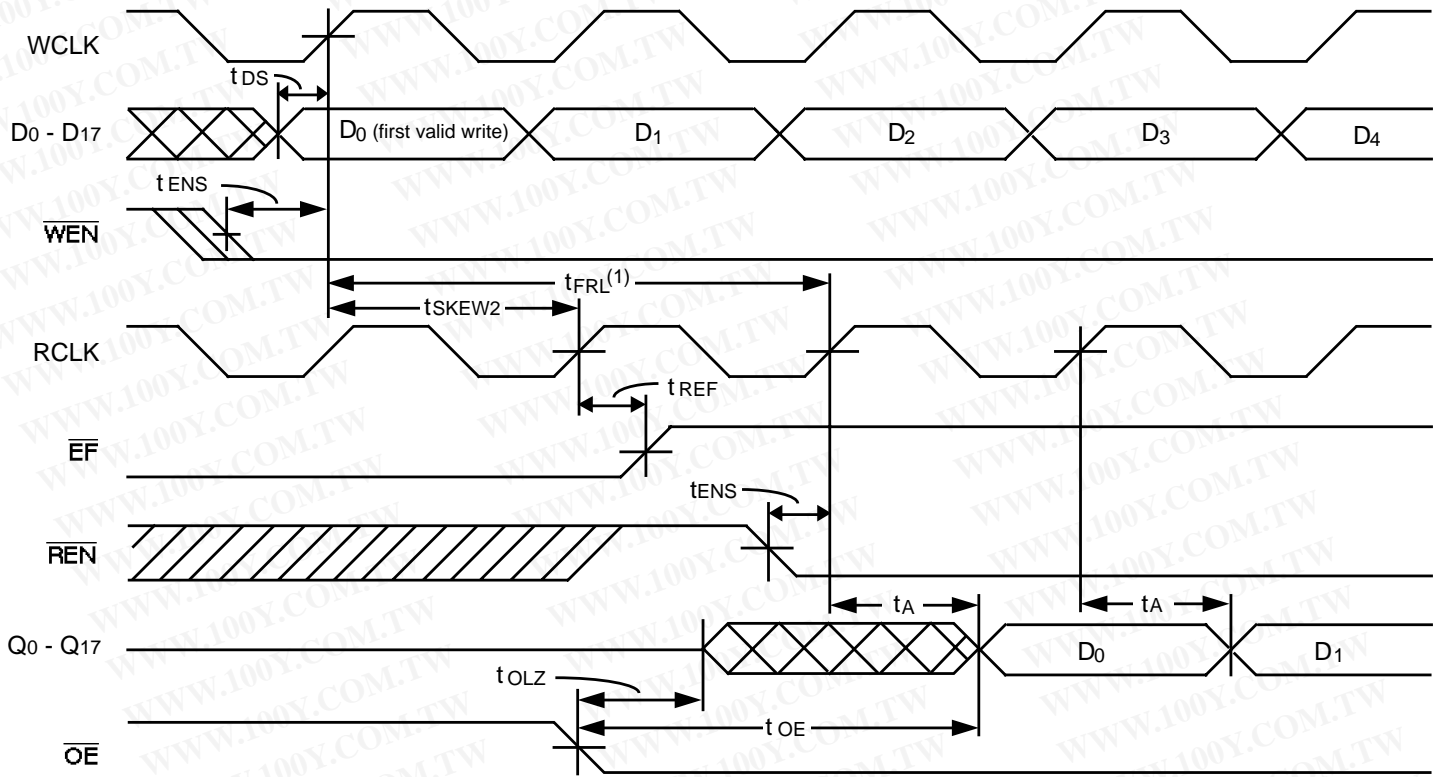


2766 drw 08

NOTE:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that \overline{EF} will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2} , then \overline{EF} may not change state until the next RCLK edge.

Figure 6. Read Cycle Timing



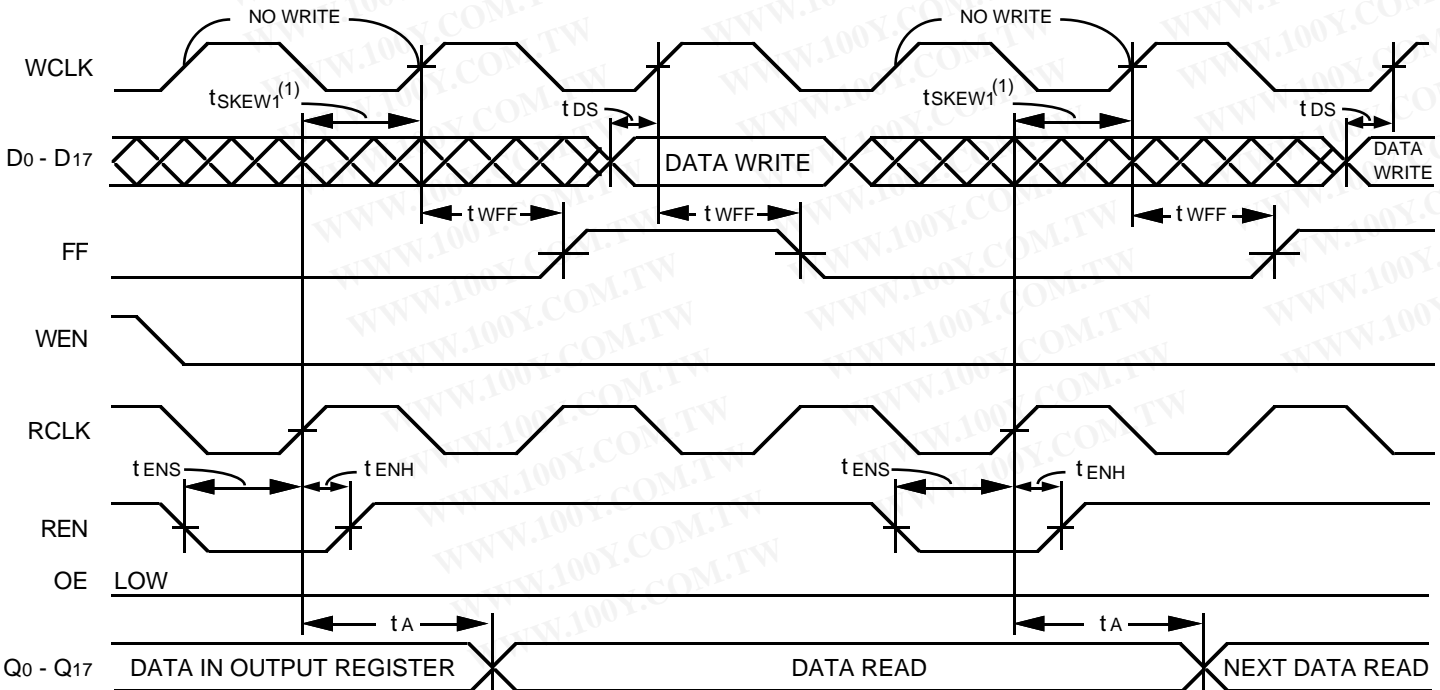
2766 drw 09

NOTES:

1. When tSKEW2 minimum specification, tFRL (maximum) = tCLK + tSKEW2. When tSKEW2 < minimum specification, tFRL (maximum) = either 2*tCLK + tSKEW2 or tCLK + tSKEW2. The Latency Timing applies only at the Empty Boundary (EF = LOW).
2. The first word is available the cycle after EF goes HIGH, always.

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Figure 7. First Data Word Latency after Reset with Simultaneous Read and Write

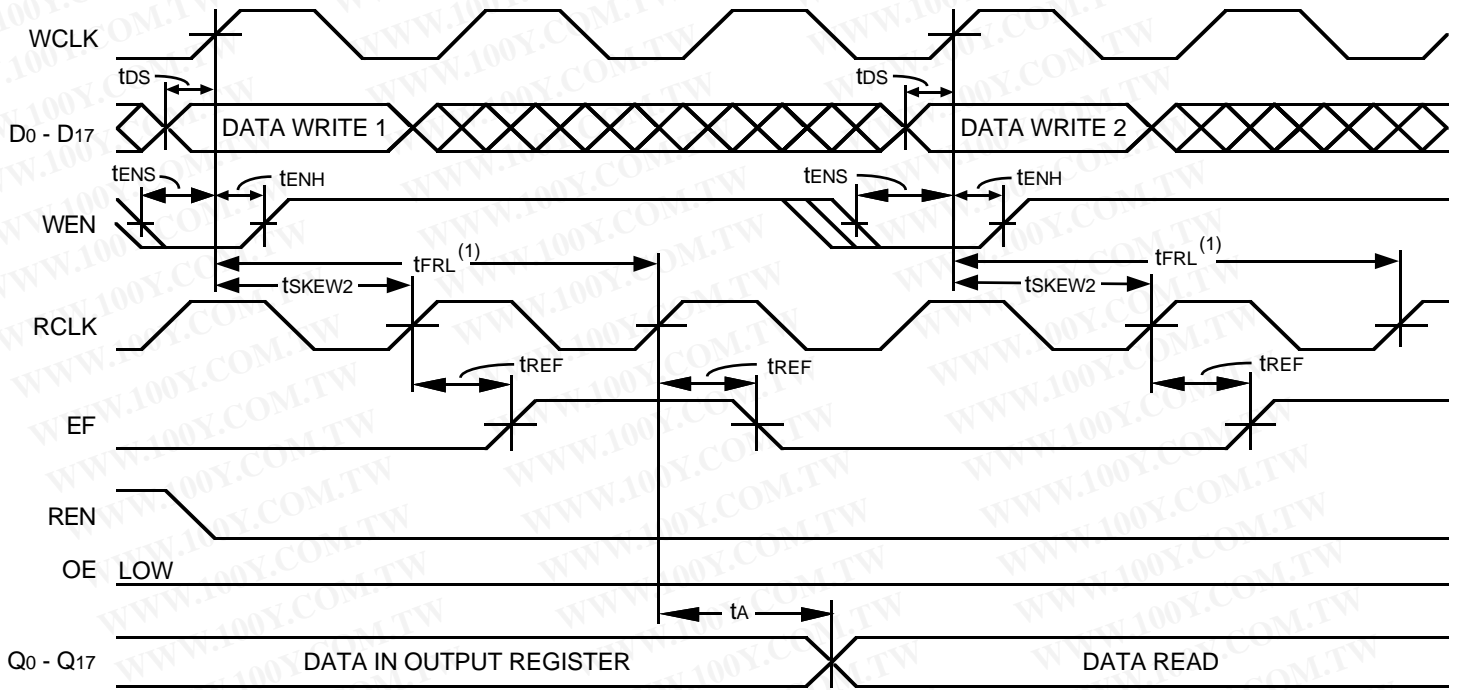


2766 drw 10

NOTE:

1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that FF will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then FF may not change state until the next WCLK edge.

Figure 8. Full Flag Timing

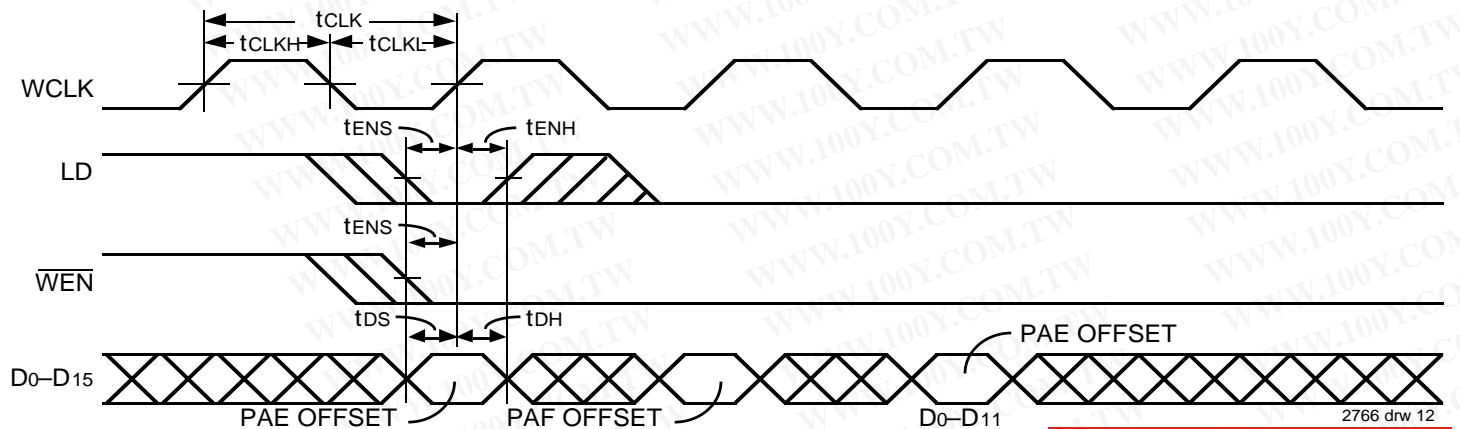


2766 drw 11

NOTE:

1. When t_{SKEW2} minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When $t_{SKEW2} <$ minimum specification, t_{FRL} (maximum) = either $2 * t_{CLK} + t_{SKEW2}$, or $t_{CLK} + t_{SKEW2}$. The Latency Timing apply only at the Empty Boundary (EF = LOW).

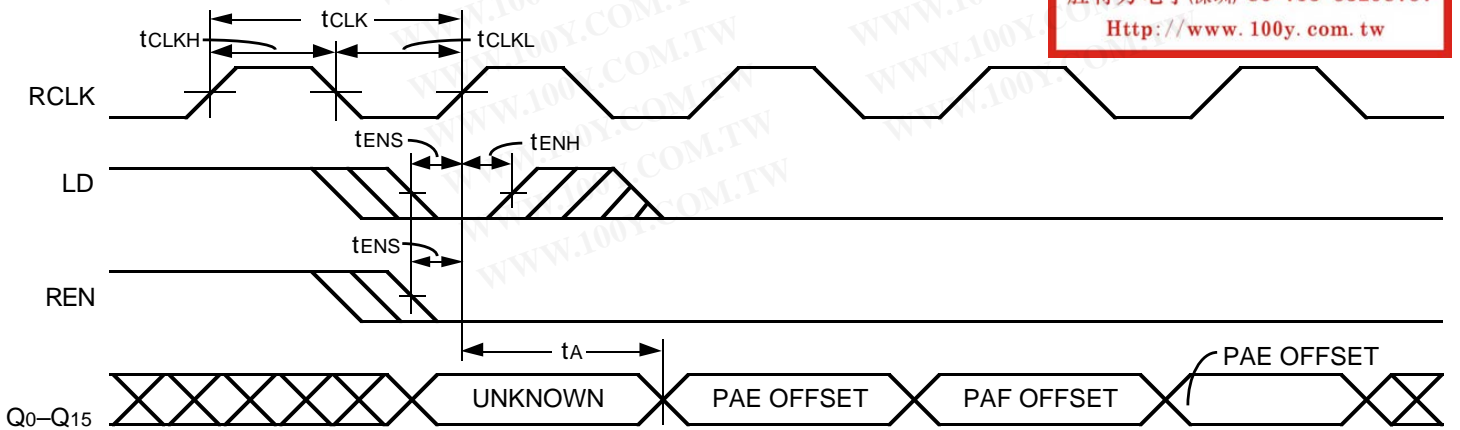
Figure 9. Empty Flag Timing



2766 drw 12

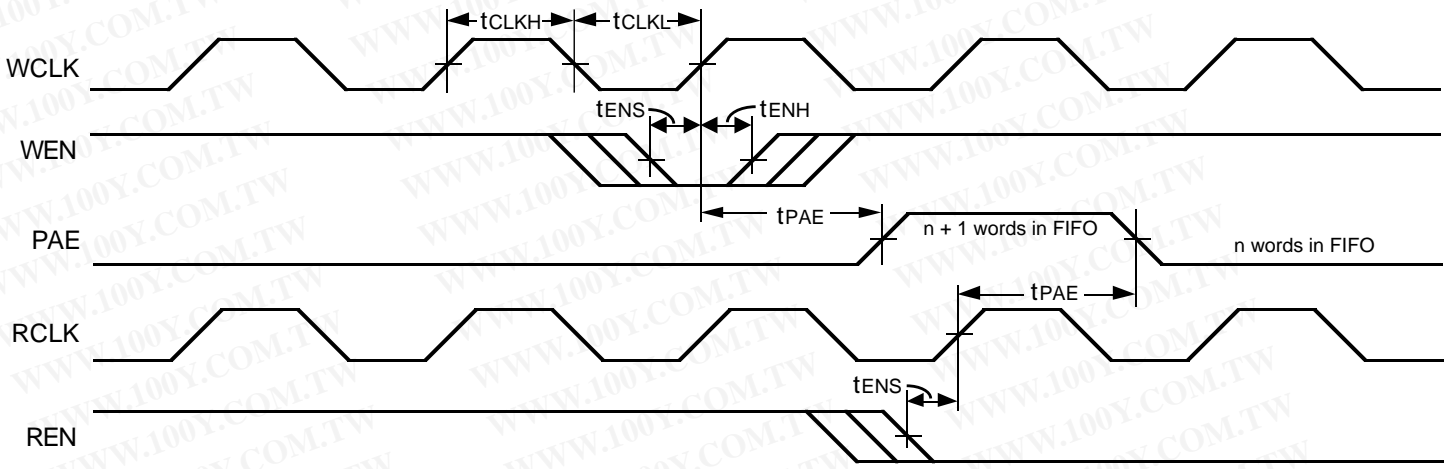
Figure 10. Write Programmable Registers

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2766 drw 13

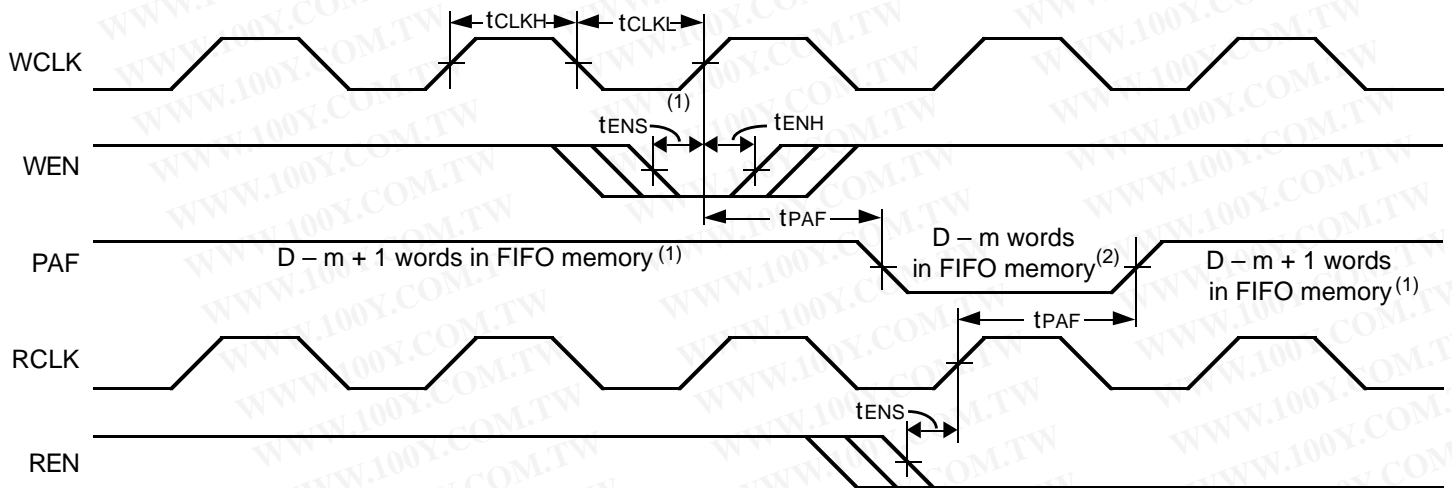
Figure 11. Read Programmable Registers



NOTE:
 1. $n = \overline{PAE}$ offset. Number of data words written into FIFO already = n .

2766 drw 14

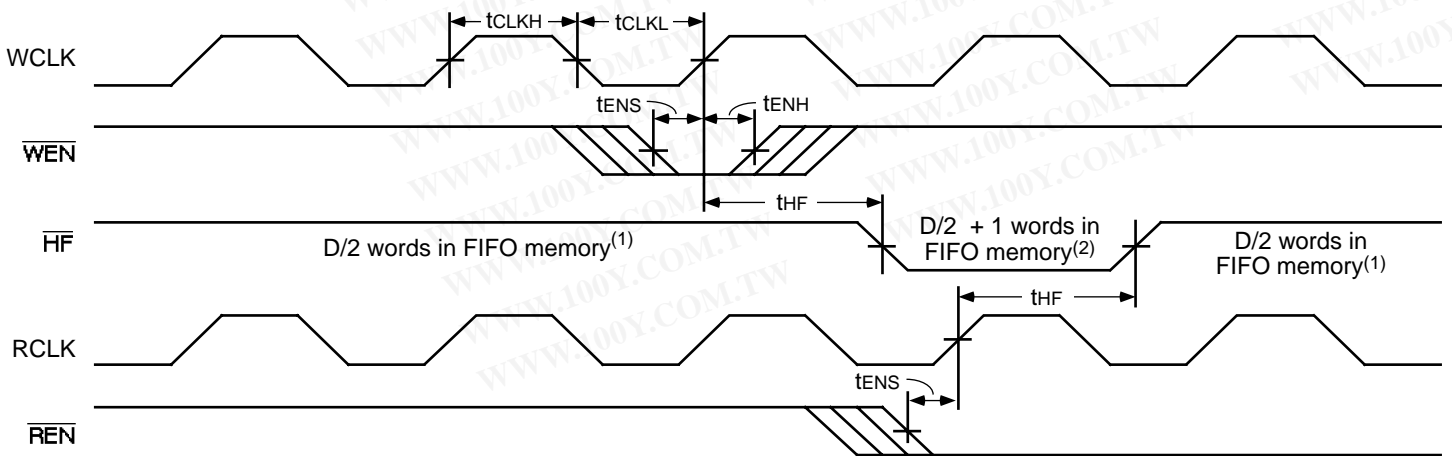
Figure 12. Programmable Almost-Empty Flag Timing



NOTES:
 1. $m = \overline{PAF}$ offset. $D =$ maximum FIFO Depth. Number of data words written into FIFO memory = $256 - m + 1$ for the IDT72205, $512 - m + 1$ for the IDT72215, $1,024 - m + 1$ for the IDT72225, $2,048 - m + 1$ for the IDT72235 and $4,096 - m + 1$ for the IDT72245.
 2. $256 - m$ words in IDT72205, $512 - m$ words in IDT72215, $1,024 - m$ words in IDT72225, $2,048 - m$ words in IDT72235 and $4,096 - m$ words in IDT72245.

2766 drw 15

Figure 13. Programmable Almost-Full Flag Timing

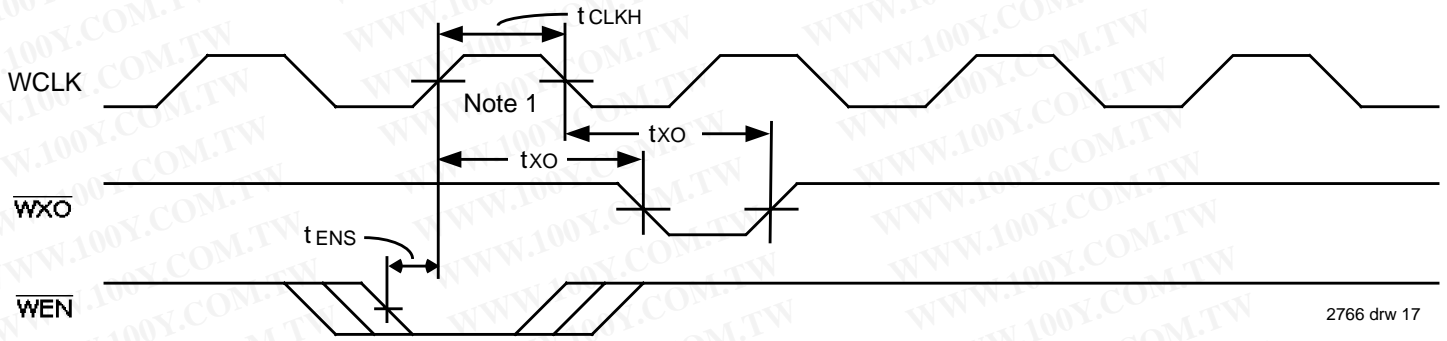


NOTE:
 1. $D =$ maximum FIFO Depth = 256 words for the IDT72205, 512 words for the IDT72215, 1,024 words for the IDT72225, 2,048 words for the IDT72235 and 4,096 words for the IDT72245.

2766 drw 16

Figure 14. Half-Full Flag Timing

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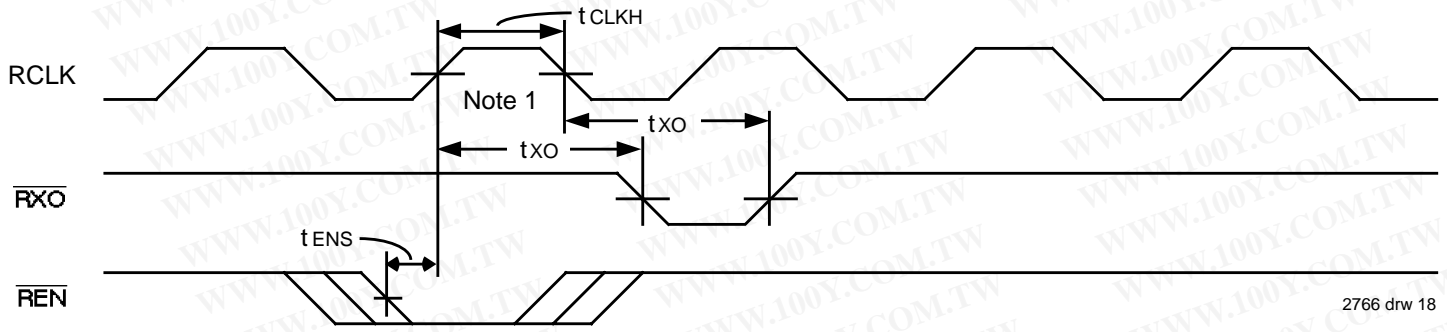


2766 drw 17

NOTE:
 1. Write to Last Physical Location.

Figure 15. Write Expansion Out Timing

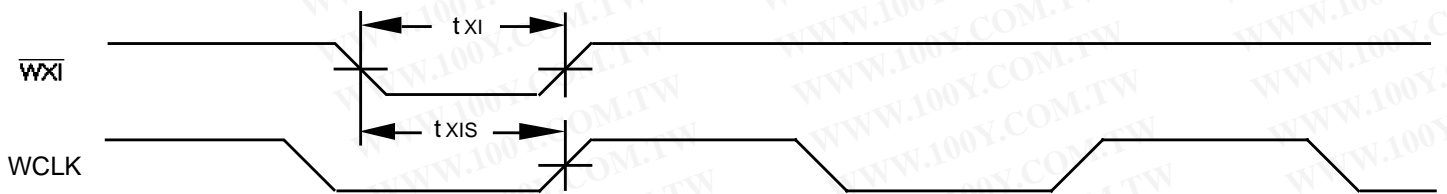
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2766 drw 18

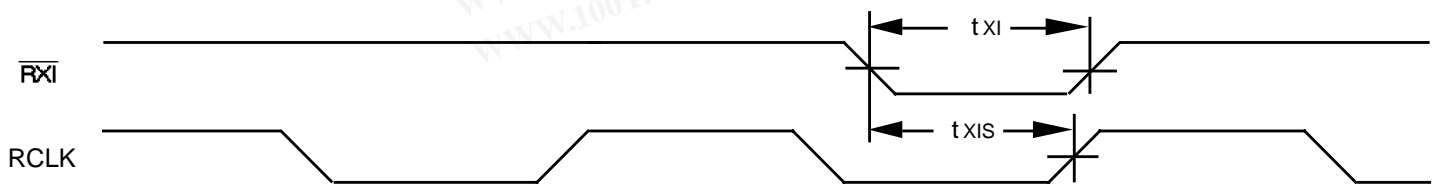
NOTE:
 1. Read from Last Physical Location.

Figure 16. Read Expansion Out Timing



2766 drw 19

Figure 17. Write Expansion In Timing



2766 drw 20

Figure 18. Read Expansion In Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72205LB/72215LB/72225LB/72235LB/72245LB may be used when the application requirements are for 256/

512/1,024/2,048/4,096 words or less. These FIFOs are in a single Device Configuration when the First Load (FL), Write Expansion In (WXI) and Read Expansion In (RXI) control inputs are grounded (Figure 19).

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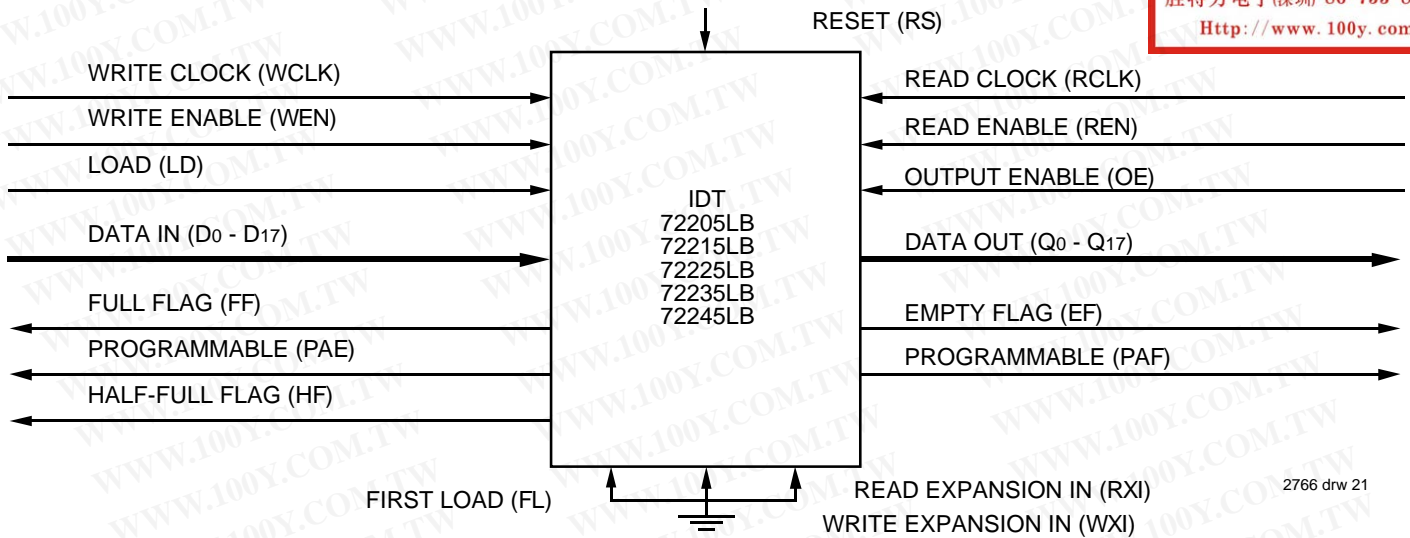
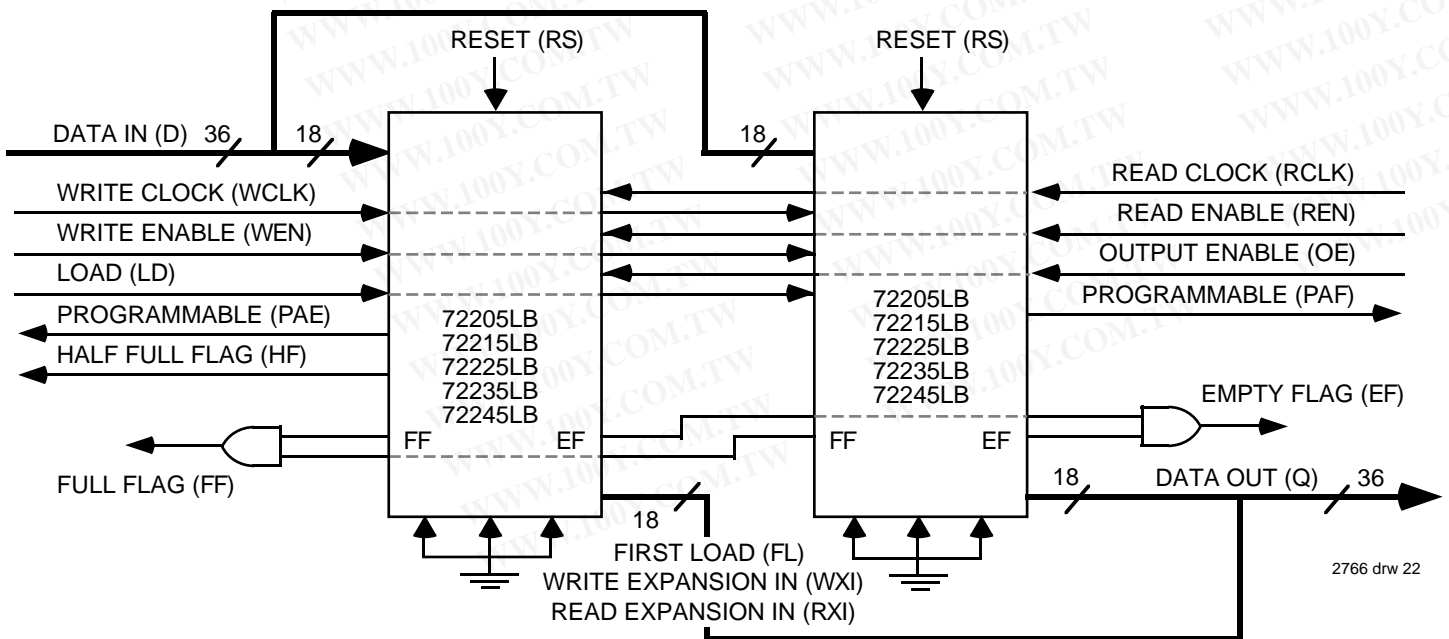


Figure 19. Block Diagram of Single 256 x 18, 512 x 18, 1,024 x 18, 2,048 x 18, 4,096 x 18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the Empty Flag and Full Flag. Because of variations in skew between RCLK and WCLK, it is possible for flag assertion and deassertion to vary by one cycle between FIFOs. To avoid problems the

user must create composite flags by ANDing the Empty Flags of every FIFO, and separately ANDing all Full Flags. Figure 20 demonstrates a 36-word width by using two IDT72205B/72215B/72225B/72235B/72245Bs. Any word width can be attained by adding additional IDT72205B/72215B/72225B/72235B/72245Bs. Please see the Application Note AN-83.



NOTE:

1. Do not connect any output control signals directly together.

Figure 20. Block Diagram of 256 x 36, 512 x 36, 1,024 x 36, 2,048 x 36, 4,096 x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

**DEPTH EXPANSION CONFIGURATION
(WITH PROGRAMMABLE FLAGS)**

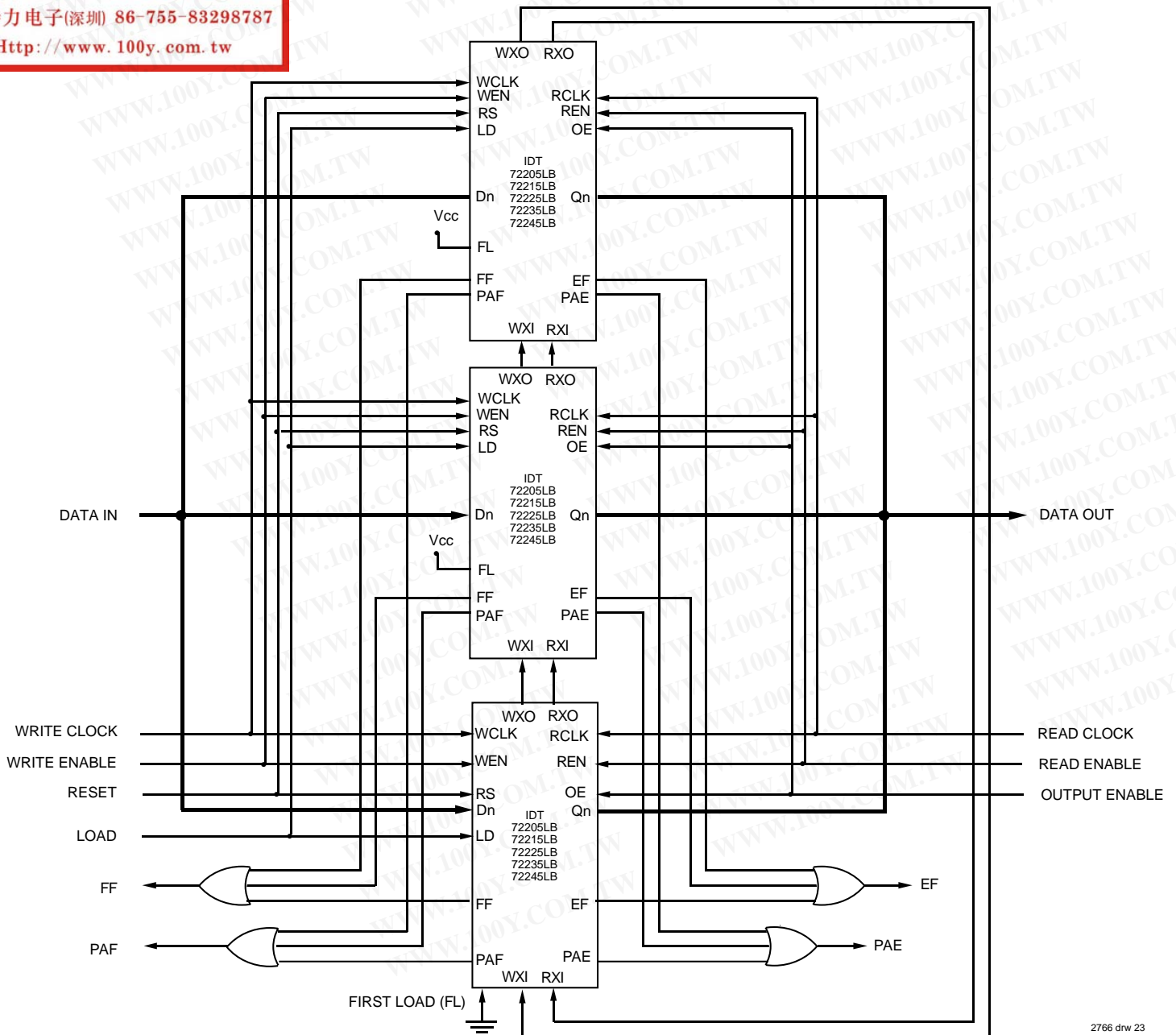
These devices can easily be adapted to applications requiring more than 256/512/1,024/2,048/4,096 words of buffering. Figure 21 shows Depth Expansion using three IDT72205LB/72215LB/72225LB/72235LB/72245LBs. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load (FL) control input.
2. All other devices must have FL in the HIGH state.
3. The Write Expansion Out (WXO) pin of each device must be tied to the Write Expansion In (WXI) pin of

the next device. See Figure 21.

4. The Read Expansion Out (RXO) pin of each device must be tied to the Read Expansion In (RXI) pin of the next device. See Figure 21.
5. All Load (LD) pins are tied together.
6. The Half-Full Flag (HF) is not available in this Depth Expansion Configuration.
7. EF, FF, PAE, and PAF are created with composite flags by ORing together every respective flags for monitoring. The composite PAE and PAF flags are not precise.

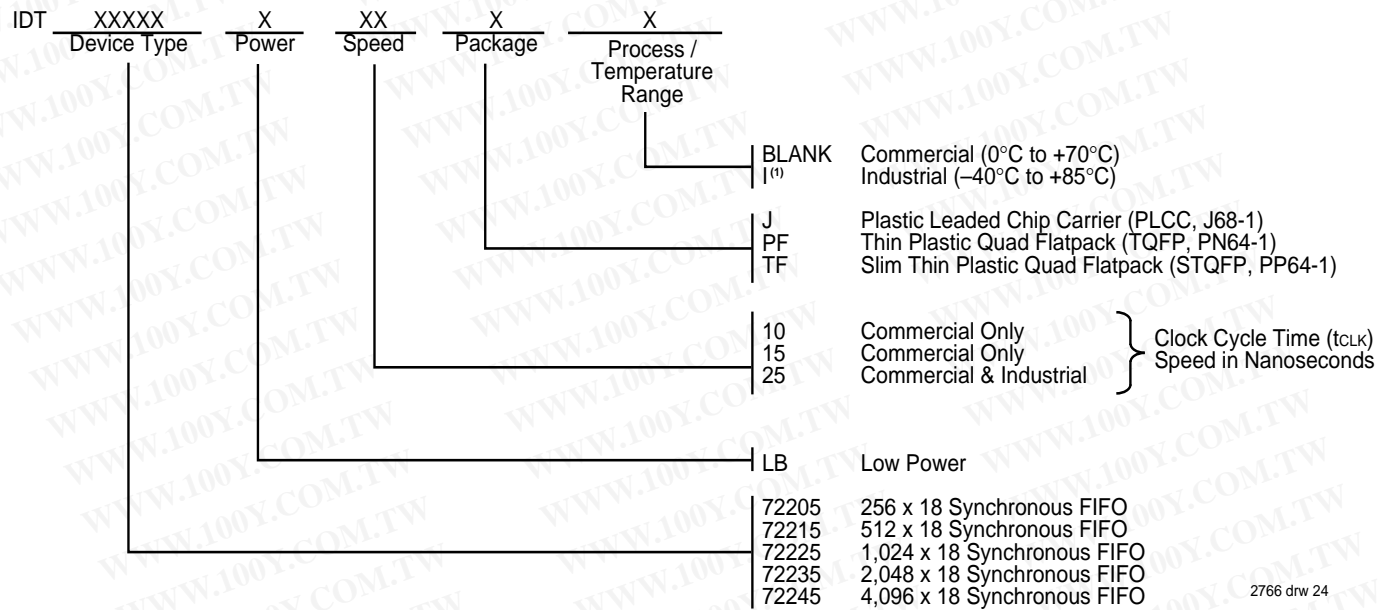
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2766 drw 23

Figure 21. Block Diagram of 768 x 18, 1,536 x 18, 3,072 x 18, 6,144 x 18, 12,288 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

ORDERING INFORMATION



2766 drw 24

NOTE:

1. Industrial temperature range is available by special order for speed grades faster than 25 ns.

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