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勝特力材料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

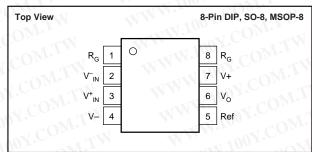
00Y.COM.TW	CONDITIONS	INA126P, U, E INA2126P, U, E		INA126PA, UA, EA INA2126PA, UA, EA					
PARAMETER		MIN	ТҮР	MAX	MIN	TYP	MAX	UNITS	
INPUT	WW.L	O.v.	N/		ΔM	N.C.		N	1
Offset Voltage, RTI	W 1 100 1.	Mo	±100	±250		±150	±500	μV	
vs Temperature	Voc - WWIE	COm	±0.5	±3 <	N VI	*	±5	μV/°C	
vs Power Supply (PSRR)	$V_{S} = \pm 1.35V$ to $\pm 18V$	-oN	5	15	-TV	*	50	μV/V	
Input Impedance	NW Y		10 ⁹ 4		NN V	*		Ω pF	
Safe Input Voltage	R _S = 0	(V–)–0.5	1.1	(V+)+0.5	*	1.10	*	V	
NN. CUT TW	$R_{S} = 1k\Omega$	(V–)–10	WT	(V+)+10	*	0011	*	V	
Common-Mode Voltage Range	$V_{O} = 0V$	±11.25	±11.5	<1	*	*		V	
Channel Separation (dual)	G = 5, dc	101.	130		N.	-110	J	dB	
Common-Mode Rejection	$R_{S} = 0, V_{CM} = \pm 11.25V$	83	94	<n td="" <=""><td>74</td><td>90</td><td>N.C.</td><td>dB</td><td></td></n>	74	90	N.C.	dB	
INA2126U (dual SO-16)		80	94			1	<u> </u>	dB	
INPUT BIAS CURRENT	WWW.		-10	-25	1	*	-50	nA	
vs Temperature	UN N.	100 -	±30	1.1.		*	100 -	pA/°C	- 1
Offset Current	WWW WWW	1.	±0.5	±2	1	*	±5	nA	
vs Temperature	3	N100'	±10			*		pA/°C	
GAIN	WW Wm	100	G = 5 to 10	k N		*	100	V/V	C.M
Gain Equation	T.L.	G	= 5 + 80kΩ	/R _G	r.	*	1.10	V/V	
Gain Error	$V_0 = \pm 14V, G = 5$	1	±0.02	±0.1		*	±0.18	%	TN
vs Temperature	G = 5	1.WV	±2	±10	1	*	*	ppm/°C	AV.
Gain Error	$V_0 = \pm 12V, G = 100$	-11	±0.2	±0.5		*	±1	%	Λ
vs Temperature	G = 100	WW.	±25	±100	X	*	*	ppm/°C	W
Nonlinearity	$G = 100, V_0 = \pm 14V$		±0.002	±0.012		*	*	%	MIT
NOISE	CONT.	NV	. Sol	COR	W		1111	N.V.	WT -
Voltage Noise, f = 1kHz	M.TY		35	AN		*	WIZ-	nV/√Hz	ON
f = 100Hz	COM	WW	35		WT -	*	NN I	nV/√Hz	WT a
f = 10Hz	-onl.		45]	1.1	*		nV/√Hz	-ON
$f_B = 0.1Hz$ to 10Hz	V.CUTT	WW	0.7	N.U	WT .	*	NN	μVp-p	WT.M.
Current Noise, f = 1kHz	COM.		60	CC CC	Wr.	*		fA/√Hz	COM.
$f_B = 0.1Hz$ to 10Hz	NT. U.		2	01.	The	*	N.	рАр-р	I.I.M.I.Y
OUTPUT	100N.		NN.	~ C	Own	<n i<="" td=""><td></td><td>14</td><td>V.COM</td></n>		14	V.COM
Voltage, Positive	$R_L = 25k\Omega$	(V+)-0.9	(V+)-0.75	1002.	*	*		V	- M.
Negative	$R_L = 25k\Omega$	(V–)+0.95		- 1	*	*	1	V	N.C.
Short-Circuit Current	Short-Circuit to Ground		+10/-5	100 -	Mon	*		mA	CON
Capacitive Load Drive	N.COM		1000		CO.	*		pF	MY.C
FREQUENCY RESPONSE	1100 - 01.1			N.100	100			WIX.	NOD T
Bandwidth, –3dB	G = 5		200	00	1.00	*		kHz	1001.0
	G = 100		9	W.Iv.	- CO	*	ſ	kHz	CO ST
N/N	G = 500	N	1.8	1	01.0-	*		kHz	11001.
Slew Rate	$V_0 = \pm 10V, G = 5$		0.4	NN.1	-1 C	*	1	V/µs	N.J.
Settling Time, 0.01%	10V Step, G = 5	N T	30	11	~~~~	*		μs	-x1 100 r.
	10V Step, G = 100		160	NN.	~ _ (*	IN	μs	N. Son V.C
1	10V Step, G = 500	TV	1500		1002.	*		μs	W.100 P
Overload Recovery	50% Input Overload		4	N WI	N.	*	IV	μs	WW.100Y.C
POWER SUPPLY	1001	1.1			1100 -	AN			W.100
Voltage Range	WWW.	±1.35	±15	±18	*	*	*	V 🔨	
Current (per channel)	$I_0 = 0$	N.1.	±175	±200	W.100	*	*	μΑ	
TEMPERATURE RANGE			N			N.C	WT I		
Specification Range	WWW.100Y.CC	-40		+85	*		*	°C	
Operation Range	WW CONT.C	-55	N	+125	*	01.0	*	°C	
Storage Range	WWW.100X.C	-55		+125	*		*	°C	
Thermal Resistance, θ_{JA}	WWW.100Y.	- 1	WI	N N	1 C 1				
8-Pin DIP	WW.IU	COM	100			*		°C/W	
SO-8 Surface-Mount	X001		150			*		°C/W	
MSOP-8 Surface-Mount		J CON	200			*		°C/W	
16-Pin DIP (dual)	WWW.100	1.~	80			*		°C/W	
SO-16 (dual)	WW.10		100			*		°C/W	
SSOP-16 (dual)		1	100			*		°C/W	1

* Specification same as INA126P, INA126U, INA126E; INA2126P, INA2126U, INA2126E.

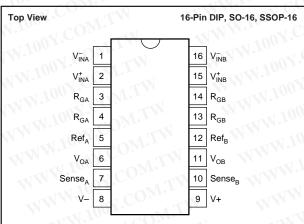
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PIN CONFIGURATION (Single)



PIN CONFIGURATION (Dual)



PACKAGE INFORMATION

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Power Supply Voltage, V+ to V	
Input Signal Voltage ⁽²⁾	(V–)–0.7 to (V+)+0.7V
Input Signal Current ⁽²⁾	10mA
Output Short Circuit	Continuous
Operating Temperature	55°C to +125°C
Storage Temperature	55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input signal voltage is limited by internal diodes connected to power supplies. See text.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	PACKAGE MARKING		TRANSPORT MEDIA
Single	W.IV. CO	NI.	WW.LO ST CC	N	WWW.
INA126PA	8-Pin DIP	006	INA126PA	INA126PA	Rails
INA126P	8-Pin DIP	006	INA126P	INA126P	Rails
INA126UA	SO-8	182	INA126UA	INA126UA	Rails or Reel
INA126U	SO-8	182	INA126U	INA126U	Rails or Reel
INA126EA ⁽²⁾ " INA126E ⁽²⁾	MSOP-8 " MSOP-8	337 " 337 "	A26 ⁽³⁾ " A26 ⁽³⁾ "	INA126EA-250 INA126EA-2500 INA126E-250 INA126E-2500	Reel Only " Reel Only "
Dual	WW.I.	V COMP.	WWW.	N.COM	WWW.
INA2126PA	16-Pin DIP	180	INA2126PA	INA2126PA	Rails
INA2126P	16-Pin DIP	180	INA2126P	INA2126P	Rails
INA2126UA	SO-16	265	INA2126UA	INA2126UA	Rails
INA2126U	SO-16	265	INA2126U	INA2126U	Rails
INA2126EA ⁽²⁾ SSOP-16		322	INA2126EA	INA2126EA-250	Reel Only
"		"	"	INA2126EA-2500	"
INA2126E ⁽²⁾ SSOP-16		322	INA2126E	INA2126E-250	Reel Only
"		"	"	INA2126E-2500	"

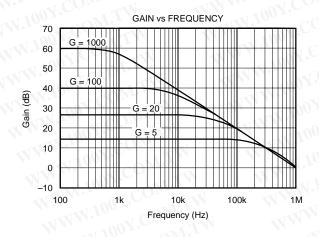
NOTES: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) MSOP-8 and SSOP-16 packages are available only on 250 or 2500 piece reels. (3) Grade designation is marked on reel.

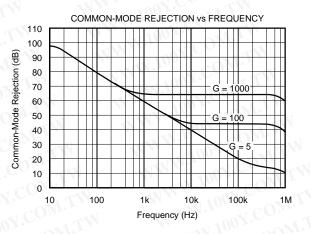


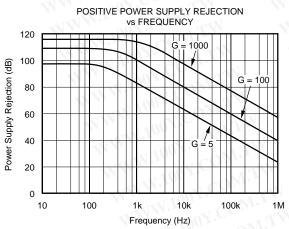
1002 TYPICAL PERFORMANCE CURVES

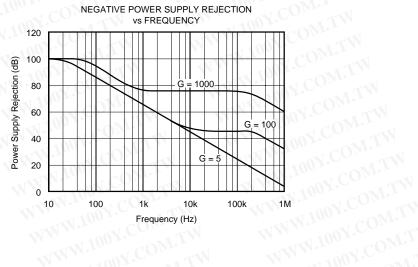
At T_A = +25°C and V_S = ±15V, unless otherwise noted.

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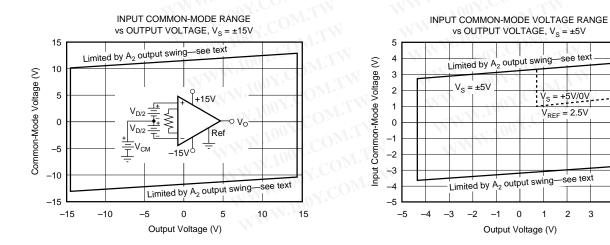






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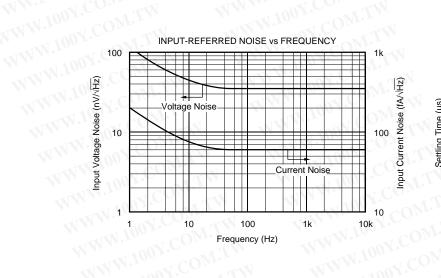


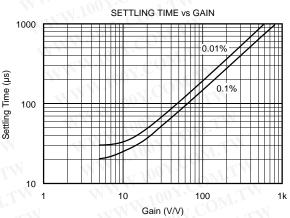


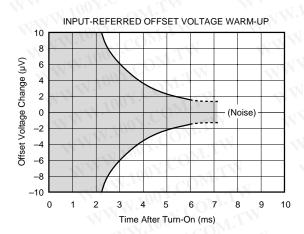
TYPICAL PERFORMANCE CURVES (CONT)

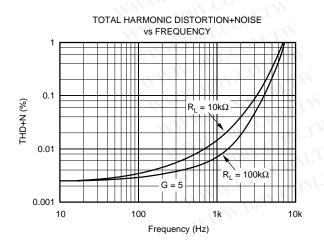
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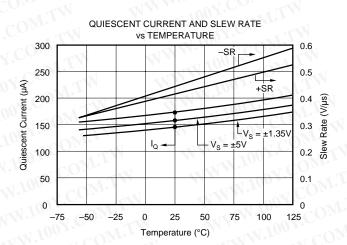
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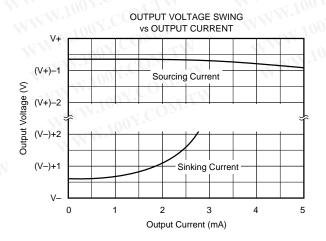










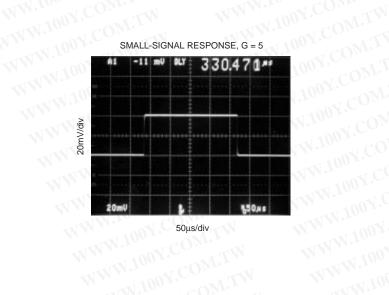


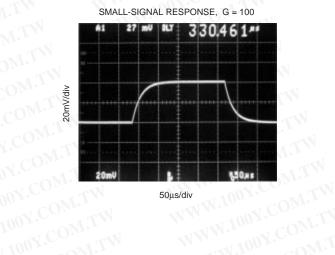
INA126, INA2126

100% TYPICAL PERFORMANCE CURVES (CONT)

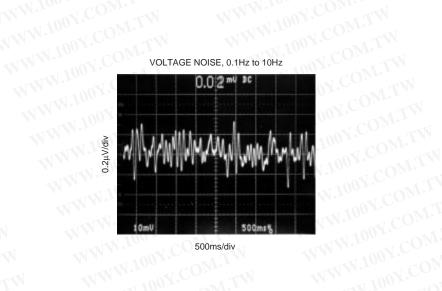
At T_A = +25°C and V_S = ±15V, unless otherwise noted.

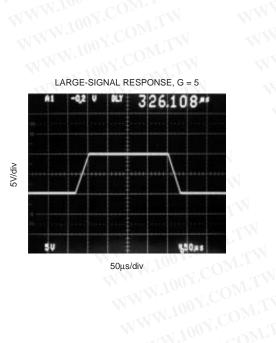
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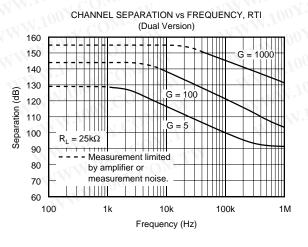




VOLTAGE NOISE, 0.1Hz to 10Hz









APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA126. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to ensure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR.

Dual versions (INA2126) have feedback sense connections, $Sense_A$ and $Sense_B$. These must be connected to their respective output terminals for proper operation. The sense connection can be used to sense the output voltage directly at the load for best accuracy.

SETTING THE GAIN

Gain is set by connecting an external resistor, R_G, as shown:

$$G = 5 + \frac{80k\Omega}{R_G}$$

Commonly used gains and R_G resistor values are shown in Figure 1.

The $80k\Omega$ term in equation 1 comes from the internal metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain

equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which will contribute additional gain error in gains of approximately 100 or greater.

OFFSET TRIMMING

The INA126 and INA2126 are laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An op amp buffer is used to provide low impedance at the Ref terminal to preserve good common-mode rejection.

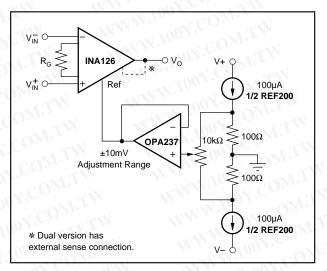


FIGURE 2. Optional Trimming of Output Offset Voltage.

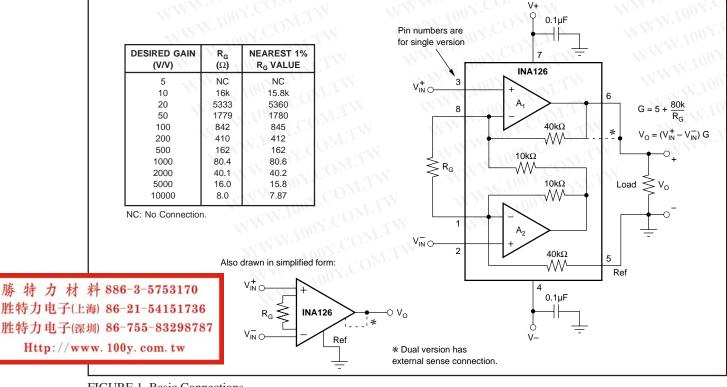


FIGURE 1. Basic Connections.

INA126, INA2126



INPUT BIAS CURRENT RETURN

The input impedance of the INA126/2126 is extremely high—approximately $10^{9}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically –10nA (current flows out of the input terminals). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the commonmode range and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

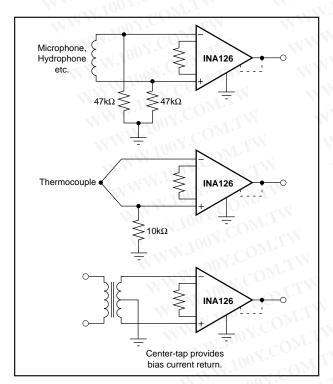


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The input common-mode range of the INA126/2126 is shown in typical performance curves. The common-mode range is limited on the negative side by the output voltage swing of A_2 , an internal circuit node that cannot be measured on an external pin. The output voltage of A_2 can be expressed as:

$$V_{O2} = 1.25 V_{IN}^{-} - (V_{IN}^{+} - V_{IN}^{-}) (10k\Omega/R_G)$$
(2)

(Voltages referred to Ref terminal, pin 5)

The internal op amp A_2 is identical to A_1 and its output swing is limited to typically 0.7V from the supply rails. When the input common-mode range is exceeded (A_2 's output is saturated), A_1 can still be in linear operation and respond to changes in the non-inverting input voltage. The output voltage, however, will be invalid.

LOW VOLTAGE OPERATION

The INA126/2126 can be operated on power supplies as low as ± 1.35 V. Performance remains excellent with power supplies ranging from ± 1.35 V to ± 18 V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to ensure that the commonmode voltage remains within its linear range. See "Input Common-Mode Voltage Range."

The INA126/2126 can be operated from a single power supply with careful attention to input common-mode range, output voltage swing of both op amps and the voltage applied to the Ref terminal. Figure 4 shows a bridge amplifier circuit operated from a single +5V power supply. The bridge provides an input common-mode voltage near 2.5V, with a relatively small differential voltage.

INPUT PROTECTION

The inputs are protected with internal diodes connected to the power supply rails. These diodes will clamp the applied signal to prevent it from exceeding the power supplies by more than approximately 0.7V. If the signal source voltage can exceed the power supplies, the source current should be limited to less than 10mA. This can generally be done with a series resistor. Some signal sources are inherently currentlimited and do not require limiting resistors.

CHANNEL CROSSTALK—DUAL VERSION

The two channels of the INA2126 are completely independent, including all bias circuitry. At DC and low frequency there is virtually no signal coupling between channels. Crosstalk increases with frequency and is dependent on circuit gain, source impedance and signal characteristics.

As source impedance increases, careful circuit layout will help achieve lowest channel crosstalk. Most crosstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Carefully balance the stray capacitance of each input to ground, and run the differential inputs of each channel parallel to each other, or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal that is rejected by the IA's input.

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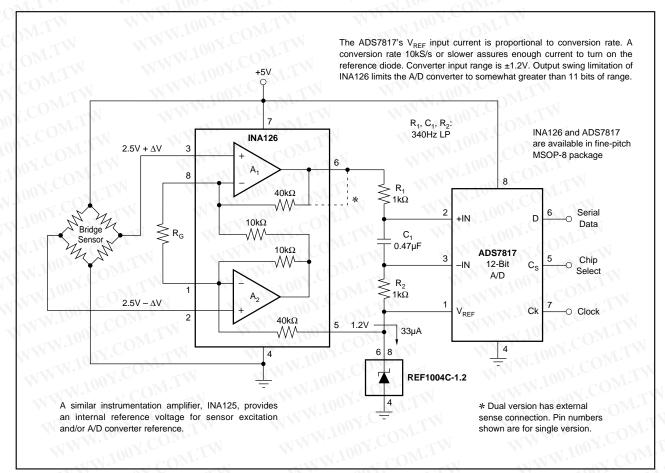
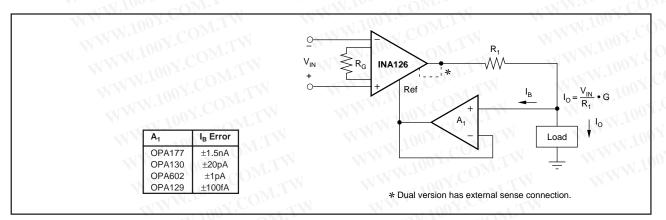


FIGURE 4. Bridge Signal Acquisition-Single 5V Supply.





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