Preliminary Data Sheet No. PD60030 rev.O

International
IOR Rectifier

IR2213(S) & (PbF)

HIGH AND LOW SIDE DRIVER

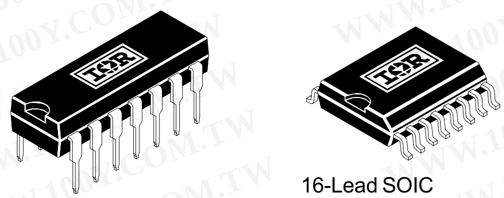
Features

- Floating channel designed for bootstrap operation
  Fully operational to +1200V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 12 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Also available LEAD-FREE (PbF)

Product Summary

V_{OFFSET}	1200V max.
I_O+/-	1.7A / 2A
V_{OUT}	12 - 20V
$t_{on/off}$ (typ.)	280 & 225 ns
Delay Matching	30 ns

Packages



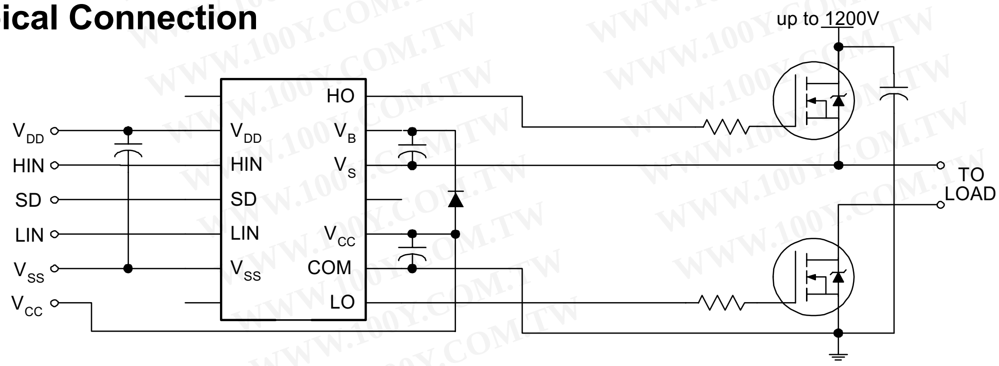
14-Lead PDIP

16-Lead SOIC (wide body)

Description

The IR2213(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 1200 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High Side Floating Supply Voltage		-0.3	1225	V
V_S	High Side Floating Supply Offset Voltage		V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low Side Fixed Supply Voltage		-0.3	25	
V_{LO}	Low Side Output Voltage		-0.3	V_{CC} + 0.3	
V_{DD}	Logic Supply Voltage		-0.3	V_{SS} + 25	
V_{SS}	Logic Supply Offset Voltage		V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)		V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient (Figure 2)		—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$	(14 Lead PDIP)	—	1.6	W
		(16 Lead SOIC)	—	1.25	
R_{THJA}	Thermal Resistance, Junction to Ambient	(14 Lead PDIP)	—	75	°C/W
		(16 Lead SOIC)	—	100	
T_J	Junction Temperature		—	125	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 12	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	Note 1	1200	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	12	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic Supply Offset Voltage	-5 (Note 2)	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	

Note 1: Logic operational for V_S of -5 to +1200V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: When V_{DD}<5V, the minimum V_{SS} offset is limited to $-V_{DD}$

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

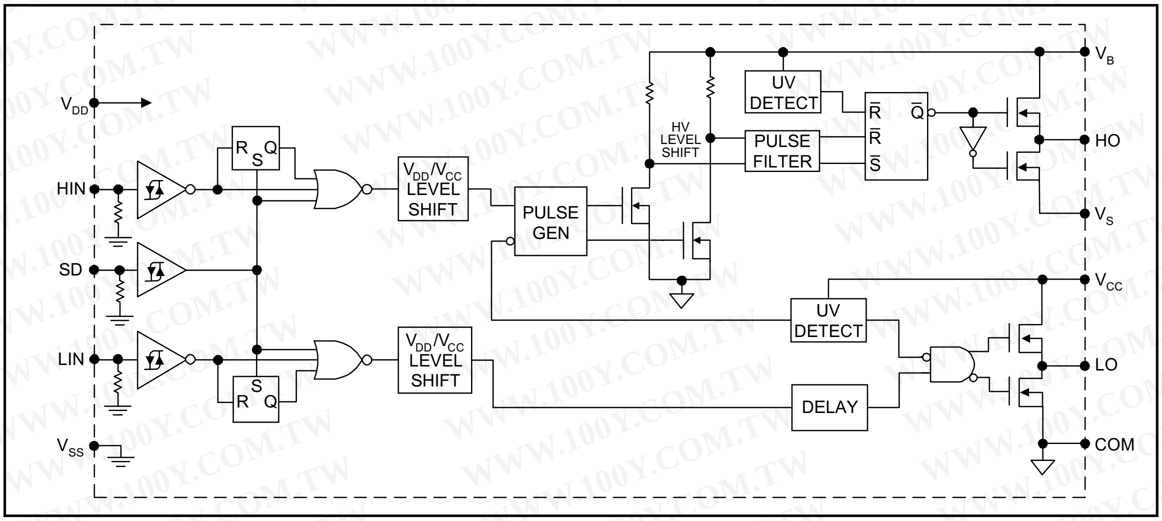
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	—	280	—	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	—	225	—		V_S = 1200V
t_{sd}	Shutdown Propagation Delay	—	230	—		V_S = 1200V
t_r	Turn-On Rise Time	—	25	—		
t_f	Turn-Off Fall Time	—	17	—		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	30		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	—	—	6.0		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50	µA	V_B = V_S = 1200V
I_{QBS}	Quiescent V_{BS} Supply Current	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" Input Bias Current	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.7	10.2	11.7	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.9	9.3	10.7		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	8.7	10.2	11.7		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.9	9.3	10.7		
I_{O+}	Output High Short Circuit Pulsed Current	1.7	2.0`	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

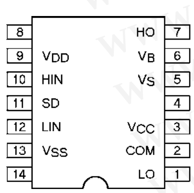
Functional Block Diagram



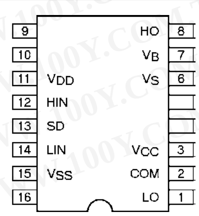
Lead Definitions

Symbol	Description
VDD	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic ground
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



14 Lead PDIP



16 Lead SOIC (Wide Body)

IR2213	IR2213S
Part Number	

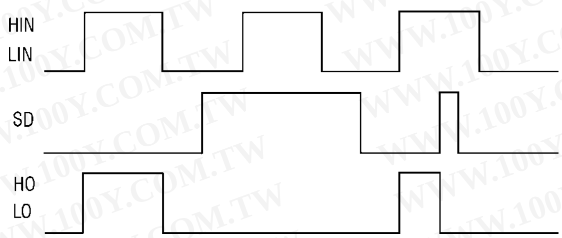


Figure 1. Input/Output Timing Diagram

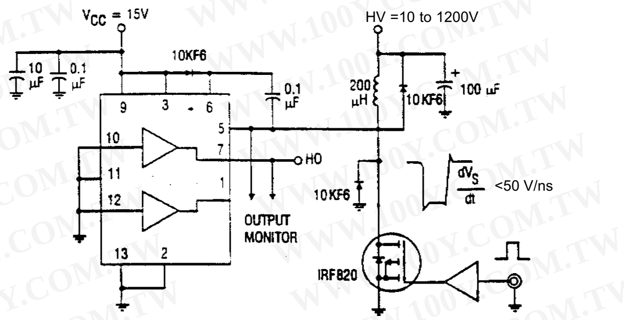


Figure 2. Floating Supply Voltage Transient Test Circuit

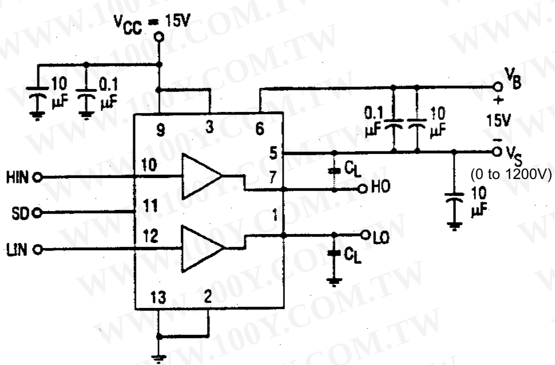


Figure 3. Switching Time Test Circuit

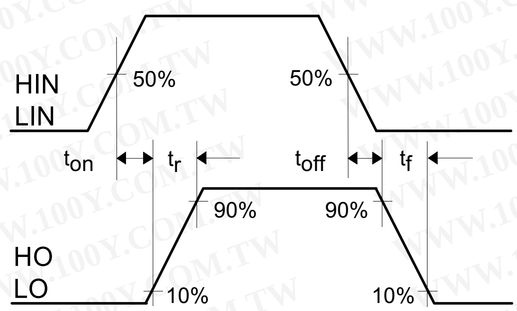


Figure 4. Switching Time Waveform Definition

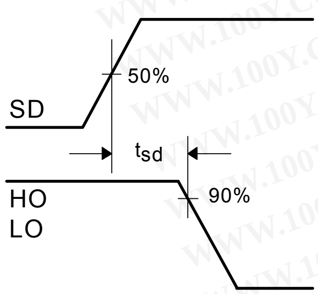


Figure 5. Shutdown Waveform Definitions

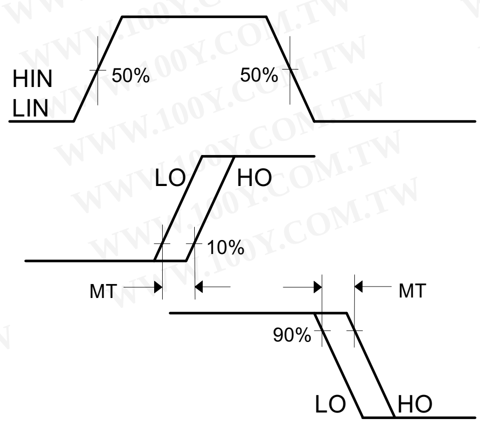


Figure 6. Delay Matching Waveform Definitions

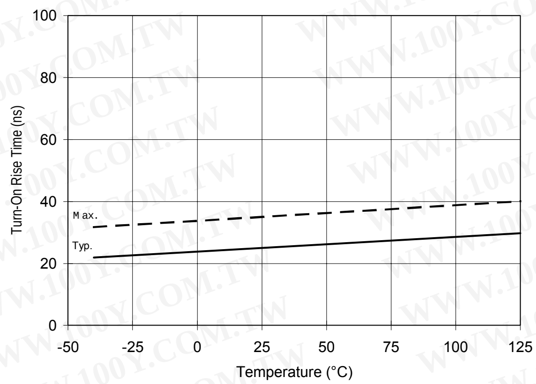


Figure 10A. Turn-On Rise Time vs. Temperature

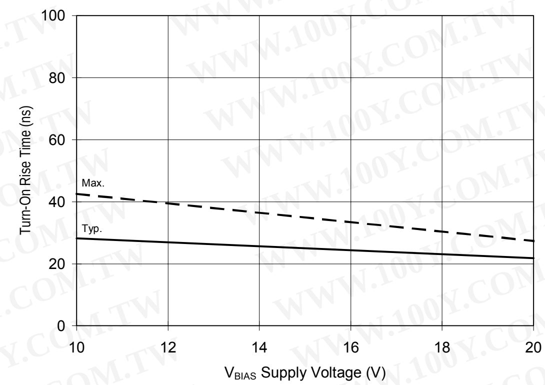


Figure 10B. Turn-On Rise Time vs. Voltage

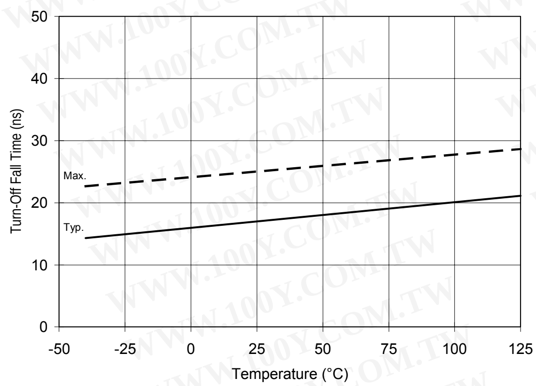


Figure 11A. Turn-Off Fall Time vs. Temperature

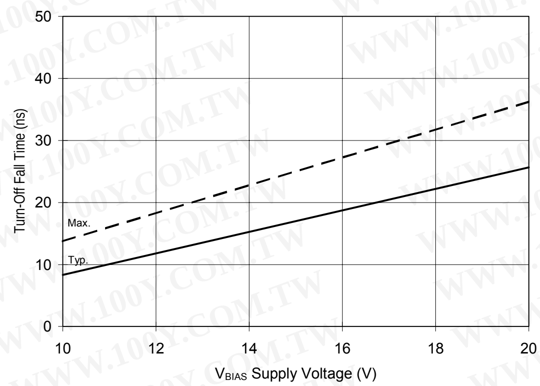


Figure 11B. Turn-Off Fall Time vs. Voltage

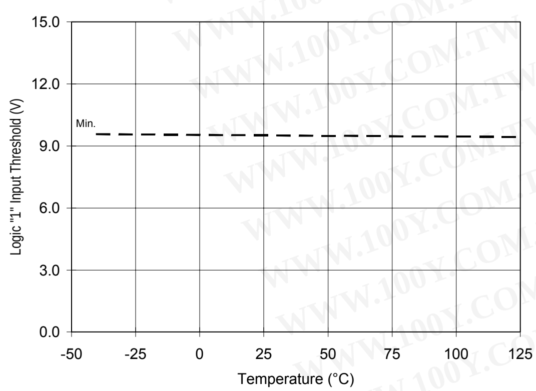


Figure 12A. Logic “1” Input Threshold vs. Temperature

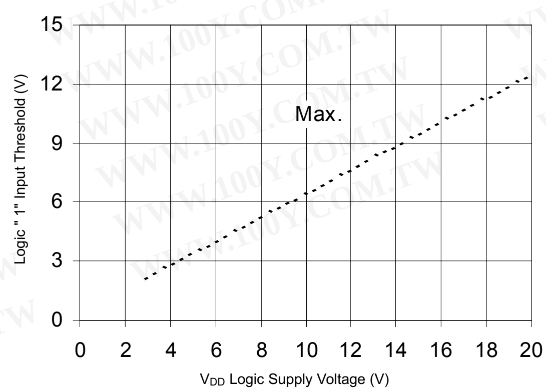


Figure 12B. Logic “1” Input Threshold vs. Voltage

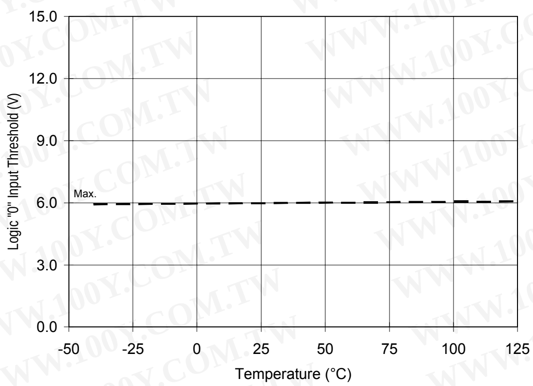


Figure 13A. Logic "0" Input Threshold vs. Temperature

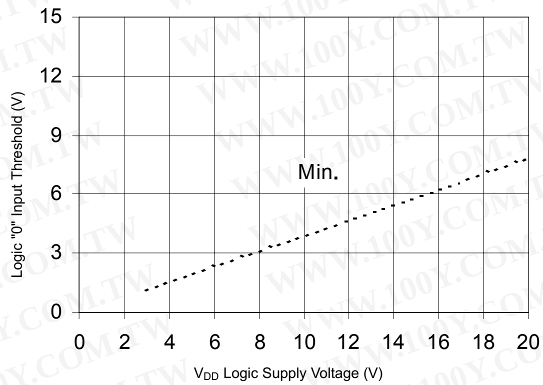


Figure 13B. Logic "0" Input Threshold vs. Voltage

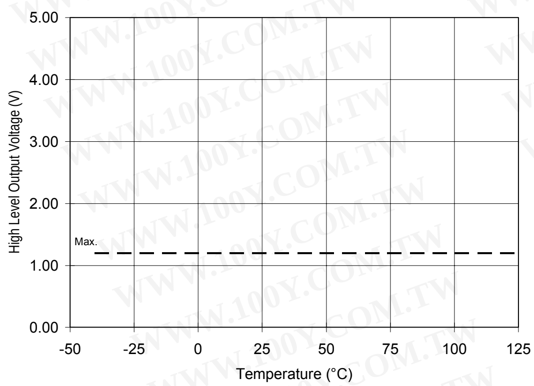


Figure 14A. High Level Output vs. Temperature

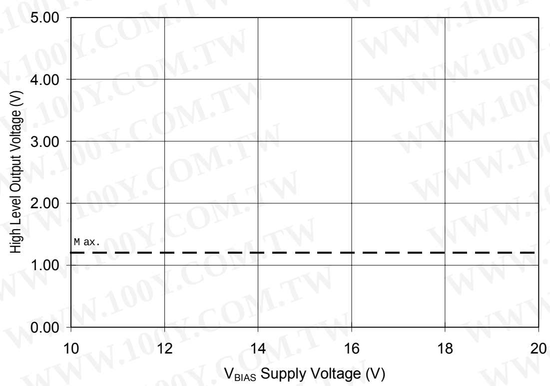


Figure 14B. High Level Output vs. Voltage

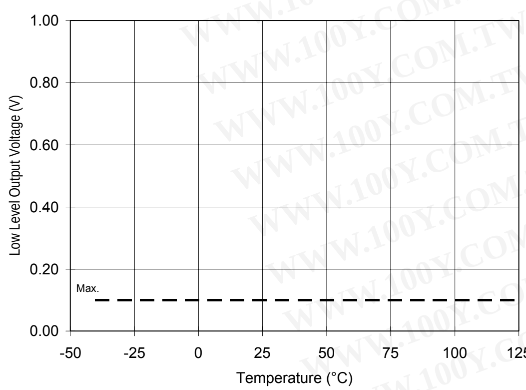


Figure 15A. Low Level Output vs. Temperature

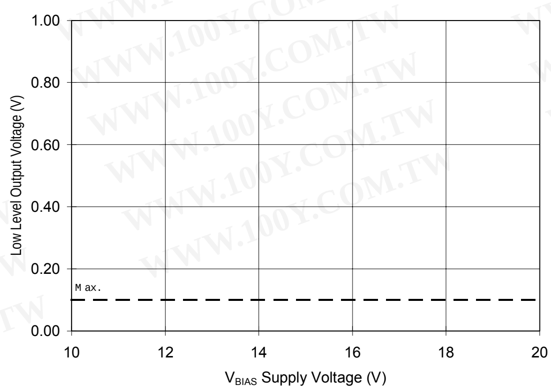


Figure 15B. Low Level Output vs. Voltage

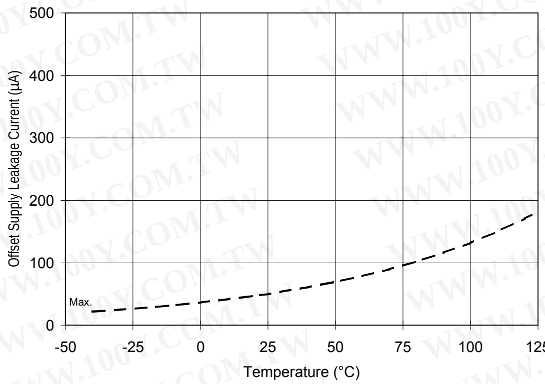


Figure 16A. Offset Supply Current vs. Temperature

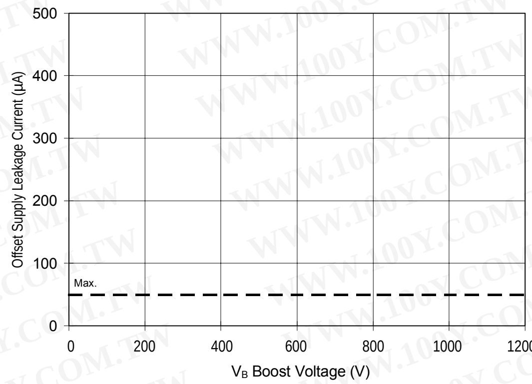


Figure 16B. Offset Supply Current vs. Voltage

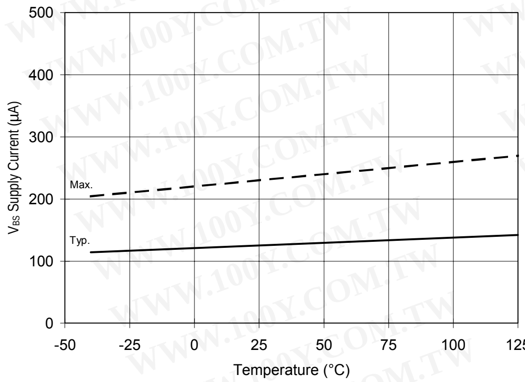


Figure 17A. V_{BS} Supply Current vs. Temperature

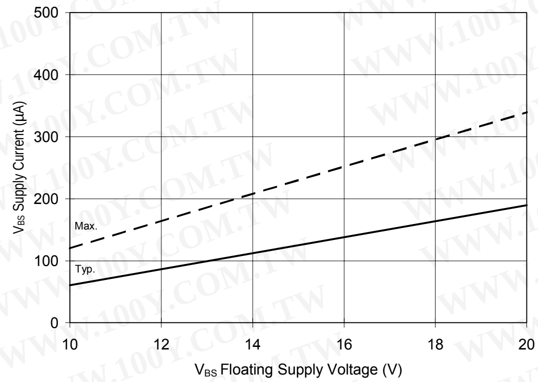


Figure 17B. V_{BS} Supply Current vs. Voltage

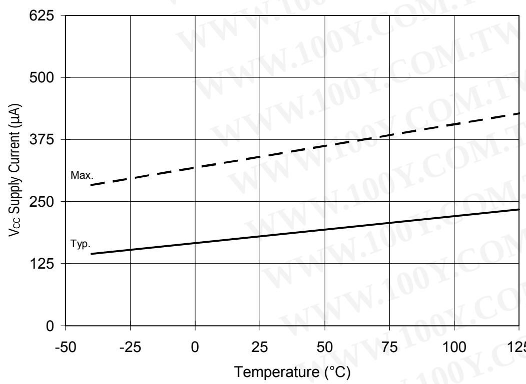


Figure 18A. V_{CC} Supply Current vs. Temperature

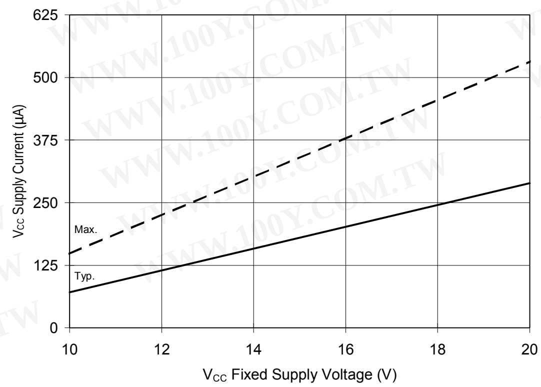


Figure 18B. V_{CC} Supply Current vs. Voltage

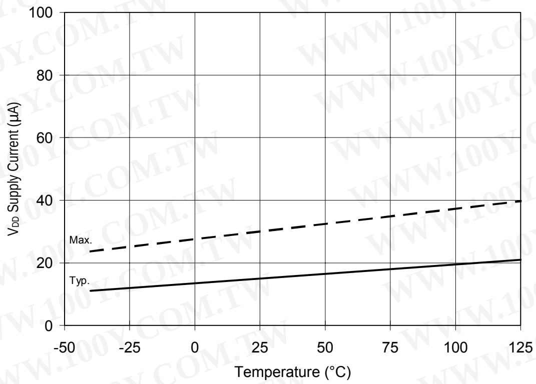


Figure 19A. V_{DD} Supply Current vs. Temperature

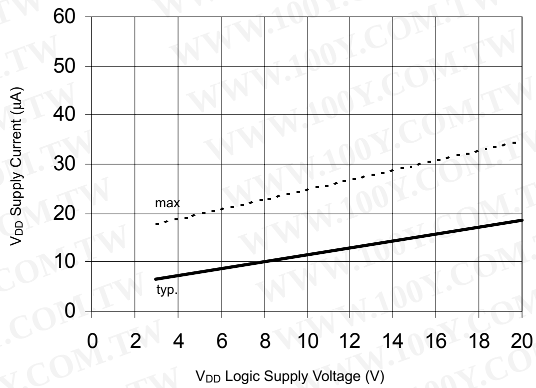


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

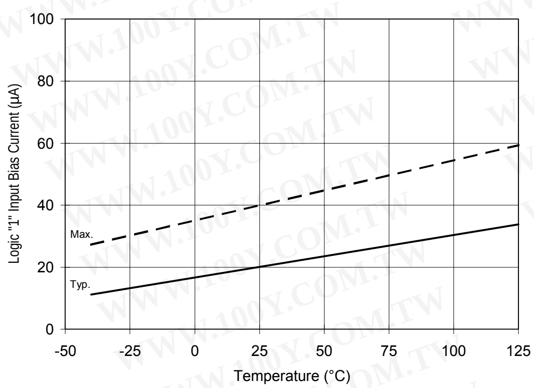


Figure 20A. Logic “1” Input Current vs. Temperature

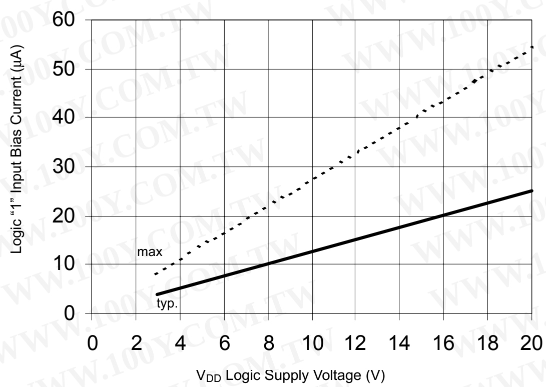


Figure 20B. Logic “1” Input Current vs. V_{DD} Voltage

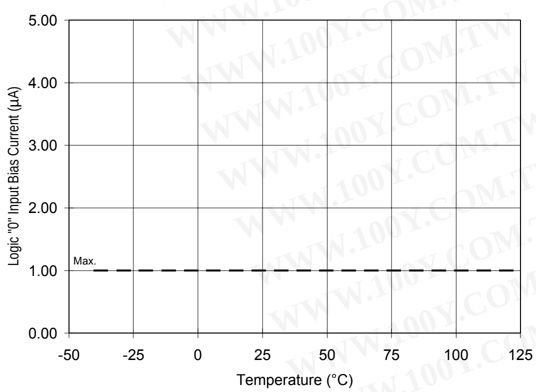


Figure 21A. Logic “0” Input Current vs. Temperature

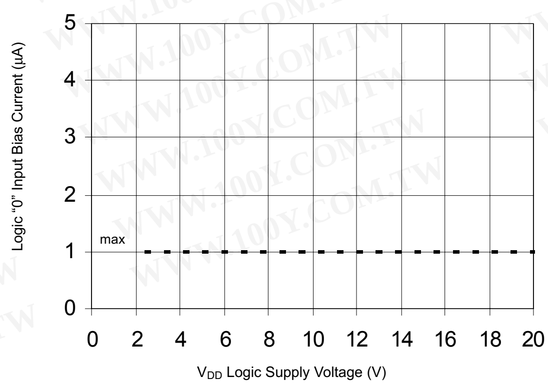


Figure 21B. Logic “0” Input Current vs. V_{DD} Voltage

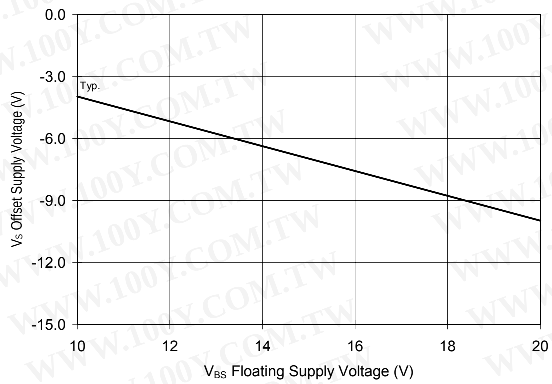


Figure 22. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

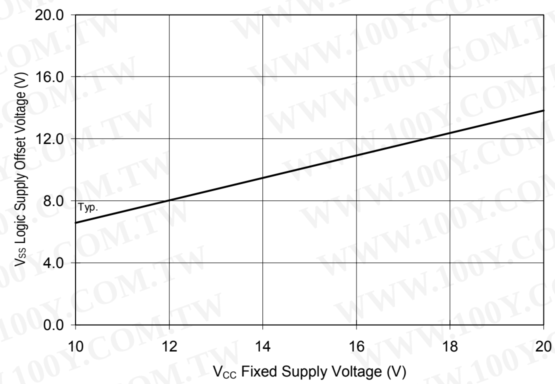


Figure 23. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

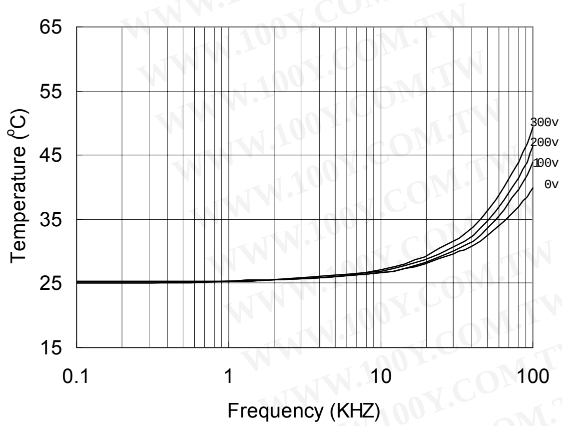


Figure 24. IR2213s vs. Frequency (IRFBC20) R_{gate}=33Ω, V_{CC}=15V

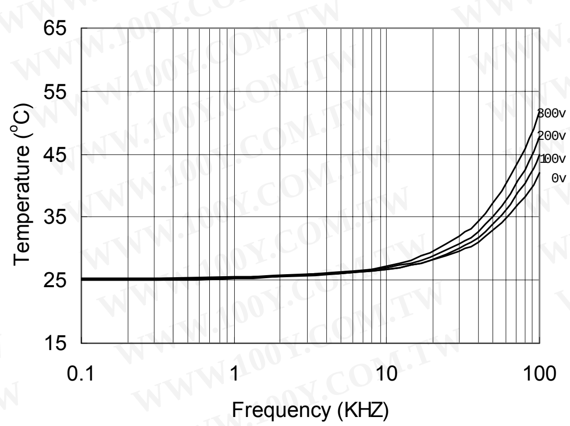


Figure 25. IR2213s vs. Frequency (IRFBC30) R_{gate}=22Ω, V_{CC}=15V

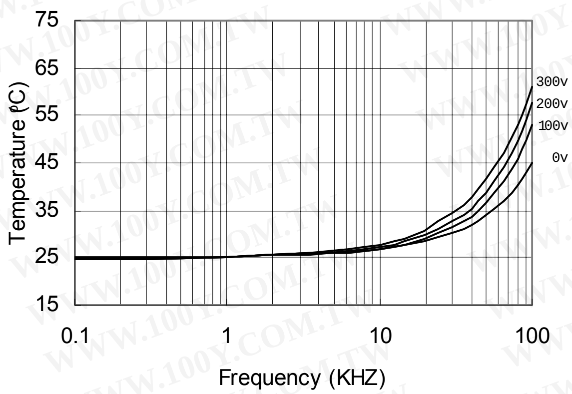


Figure 26. IR2213s vs. Frequency (IRFBC40)
R_{gate}=15Ω, V_{CC}=15V

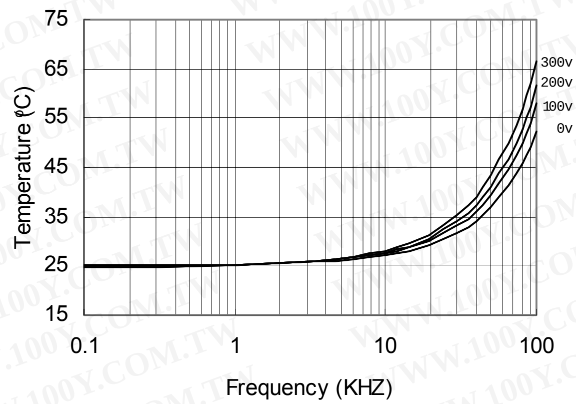


Figure 27. IR2213s vs. Frequency (IRFBC50)
R_{gate}=10Ω, V_{CC}=15V

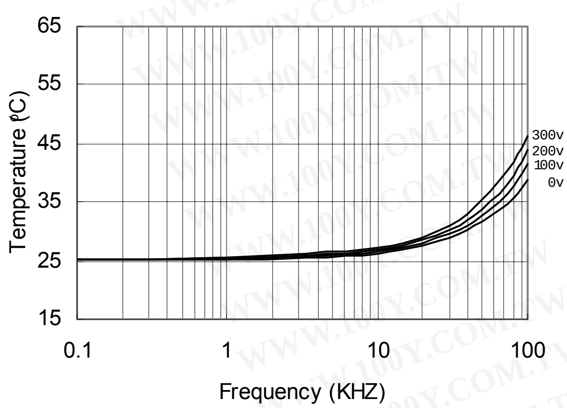


Figure 28. IR2213 vs. Frequency (IRFBC20)
R_{gate}=33Ω, V_{CC}=15V

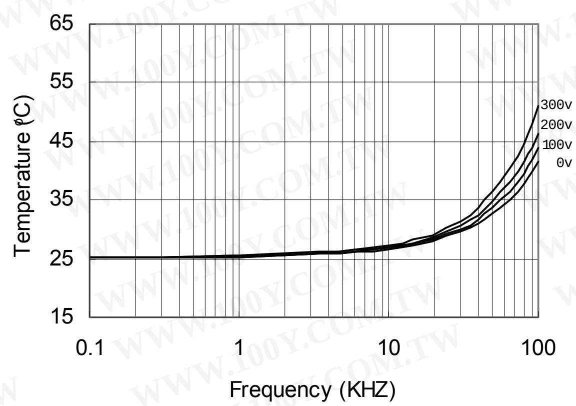


Figure 29. IR2213 vs. Frequency (IRFBC30)
R_{gate}=22Ω, V_{CC}=15V

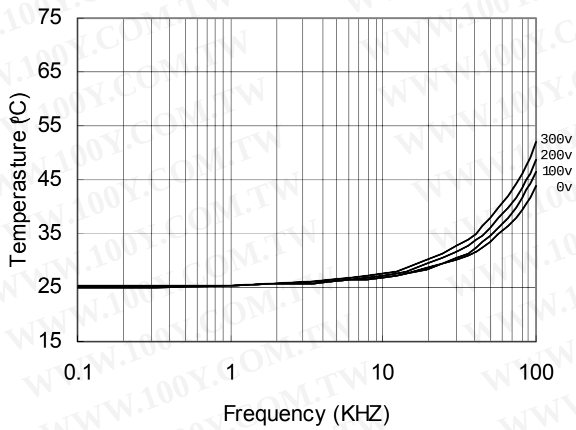


Figure 30. IR2213 vs. Frequency (IRFBC40)
R_{gate}=15Ω, V_{CC}=15V

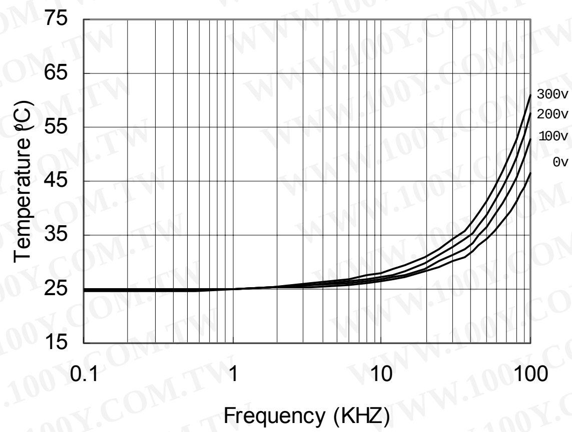
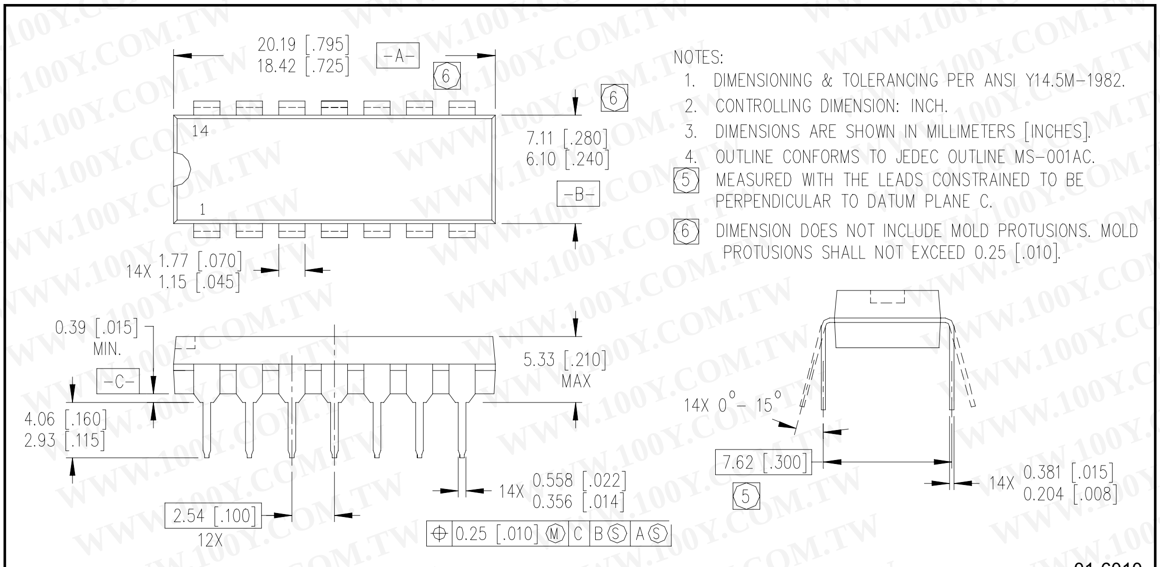


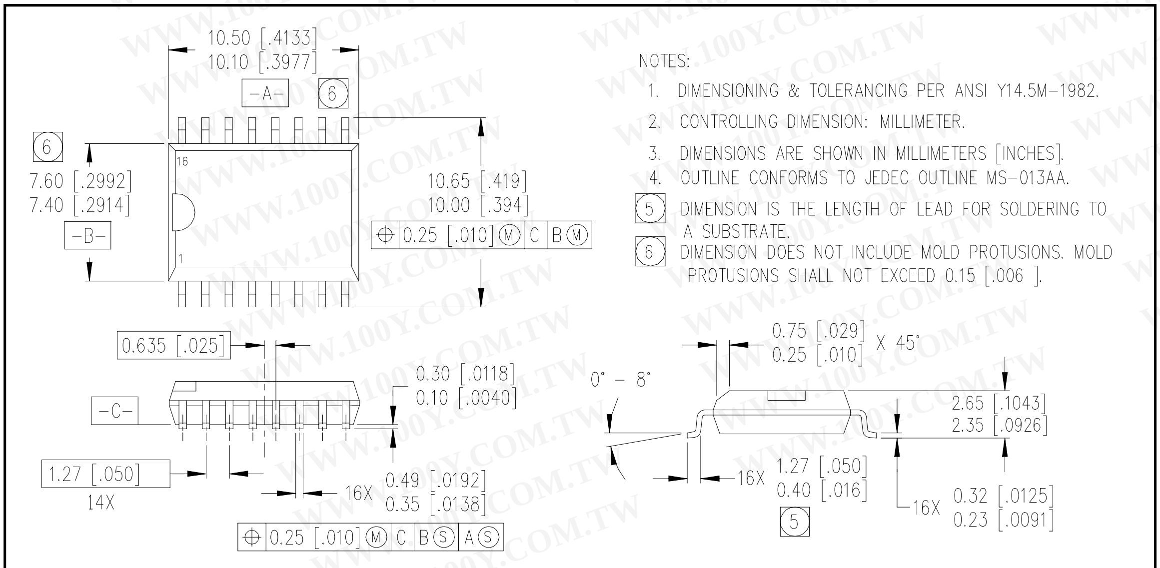
Figure 31. IR213 vs. Frequency (IRFBC50)
R_{gate}=10Ω, V_{CC}=15V

Case outlines



14-Lead PDIP

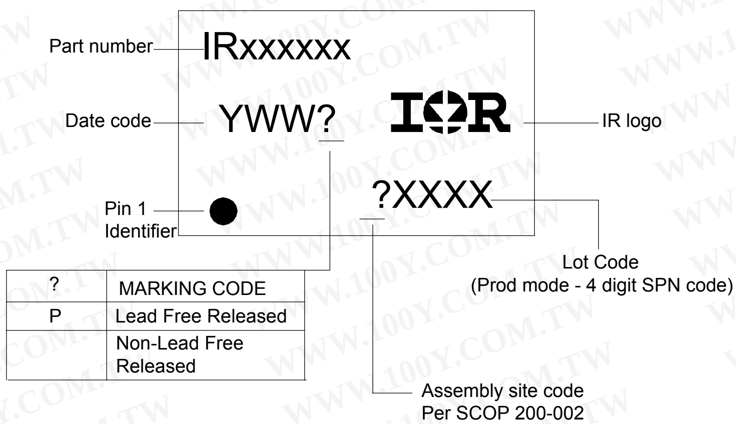
01-6010
01-3002 03 (MS-001AC)



16-Lead SOIC (wide body)

01 6015
01-3014 03 (MS-013AA)

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)
8-Lead PDIP IR2181 order IR2181
8-Lead SOIC IR2181S order IR2181S
14-Lead PDIP IR21814 order IR21814
14-Lead SOIC IR21814 order IR21814S

Leadfree Part
8-Lead PDIP IR2181 order IR2181PbF
8-Lead SOIC IR2181S order IR2181SPbF
14-Lead PDIP IR21814 order IR21814PbF
14-Lead SOIC IR21814 order IR21814SPbF

International
IOR Rectifier

Thisproduct has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web Site *http://www.irf.com*
Data and specifications subject to change without notice.
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
9/21/2004