

International Rectifier

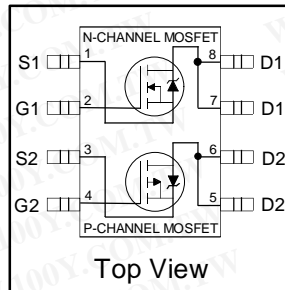
PRELIMINARY

PD - 9.1243B

IRF7309

HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

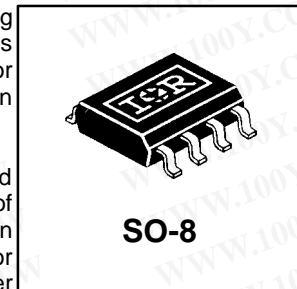


	N-Ch	P-Ch
V_{DS}	30V	-30V
$R_{DS(on)}$	0.050Ω	0.10Ω

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design for which HEXFET Power MOSFETs are well known, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra-red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



Absolute Maximum Ratings

Parameter		Max.		Units
		N-Channel	P-Channel	
I_D @ $T_A = 25^\circ\text{C}$	10 Sec. Pulse Drain Current, V_{GS} @ 10V	4.7	-3.5	A
I_D @ $T_A = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	4.0	-3.0	A
I_D @ $T_A = 70^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	3.2	-2.4	A
I_{DM}	Pulsed Drain Current $\text{\textcircled{D}}$	16	-12	A
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation (PCB Mount)**	1.4		W
	Linear Derating Factor (PCB Mount)**	0.011		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt $\text{\textcircled{D}}$	6.9	-6.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Amb. (PCB Mount, steady state)**	—	—	90	°C/W

** When mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Description	N-Ch	P-Ch	Min.	Typ.	Max.	Units	Conditions
				—	—	—		
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	N-Ch	P-Ch	30	—	—	V	V _{GS} = 0V, I _D = 250μA V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	N-Ch	P-Ch	—	0.032	—	V/°C	Reference to 25°C, I _D = 1mA Reference to 25°C, I _D = -1mA
R _{DS(ON)}	Static Drain-to-Source On-Resistance	N-Ch	P-Ch	—	—	0.050	Ω	V _{GS} = 10V, I _D = 2.4A ③ V _{GS} = 4.5V, I _D = 2.0A ③ V _{GS} = -10V, I _D = -1.8A ③ V _{GS} = -4.5V, I _D = -1.5A ③
V _{GS(th)}	Gate Threshold Voltage	N-Ch	P-Ch	1.0	—	—	V	V _{DS} = V _{GS} , I _D = 250μA V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	N-Ch	P-Ch	5.2	—	—	S	V _{DS} = 15V, I _D = 2.4A ③ V _{DS} = -24V, I _D = -1.8A ③
I _{DSS}	Drain-to-Source Leakage Current	N-Ch	P-Ch	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V V _{DS} = -24V, V _{GS} = 0V V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C V _{DS} = -24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	—	±100	—	V _{GS} = ±20V
Q _g	Total Gate Charge	N-Ch	P-Ch	—	—	25	—	N-Channel I _D = 2.6A, V _{DS} = 16V, V _{GS} = 4.5V ③
Q _{gs}	Gate-to-Source Charge	N-Ch	P-Ch	—	—	2.9	nC	
Q _{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	P-Ch	—	—	7.9	—	P-Channel I _D = -2.2A, V _{DS} = -16V, V _{GS} = -4.5V
t _{d(on)}	Turn-On Delay Time	N-Ch	P-Ch	—	6.8	—	ns	N-Channel V _{DD} = 10V, I _D = 2.6A, R _G = 6.0Ω, R _D = 3.8Ω ③
t _r	Rise Time	N-Ch	P-Ch	—	21	—		
t _{d(off)}	Turn-Off Delay Time	N-Ch	P-Ch	—	22	—	ns	P-Channel V _{DD} = -10V, I _D = -2.2A, R _G = 6.0Ω, R _D = 4.5Ω
t _f	Fall Time	N-Ch	P-Ch	—	7.7	—		
L _D	Internal Drain Inductance	N-P	—	—	—	4.0	nH	Between lead tip and center of die contact
L _S	Internal Source Inductance	N-P	—	—	—	6.0		
C _{iss}	Input Capacitance	N-Ch	P-Ch	—	—	520	pF	N-Channel V _{GS} = 0V, V _{DS} = 15V, f = 1.0MHz ③
C _{oss}	Output Capacitance	N-Ch	P-Ch	—	—	180		
C _{rss}	Reverse Transfer Capacitance	N-Ch	P-Ch	—	—	200	pF	P-Channel V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz
C _{rss}	Reverse Transfer Capacitance	N-Ch	P-Ch	—	—	72		
C _{rss}	Reverse Transfer Capacitance	N-Ch	P-Ch	—	—	93	—	—

Source-Drain Ratings and Characteristics

Parameter	Description	N-Ch	P-Ch	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	N-Ch	P-Ch	—	—	1.8	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	P-Ch	—	—	16		
V _{SD}	Diode Forward Voltage	N-Ch	P-Ch	—	—	1.0	V	T _J = 25°C, I _S = 1.8A, V _{GS} = 0V ③
		N-Ch	P-Ch	—	—	-1.0		T _J = 25°C, I _S = -1.8A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	N-Ch	P-Ch	—	47	71	ns	N-Channel T _J = 25°C, I _F = 2.6A, di/dt = 100A/μs ③
Q _{rr}	Reverse Recovery Charge	N-Ch	P-Ch	—	56	84		P-Channel T _J = 25°C, I _F = -2.2A, di/dt = 100A/μs ③
t _{on}	Forward Turn-On Time	N-P	—	—	—	—	—	Intrinsic turn-on time is negligible (turn-on is dominated by I _S +L _D)

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 23)

② N-Channel I_{SD} ≤ 2.4A, di/dt ≤ 73A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
 P-Channel I_{SD} ≤ -1.8A, di/dt ≤ 90A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.



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N-Channel

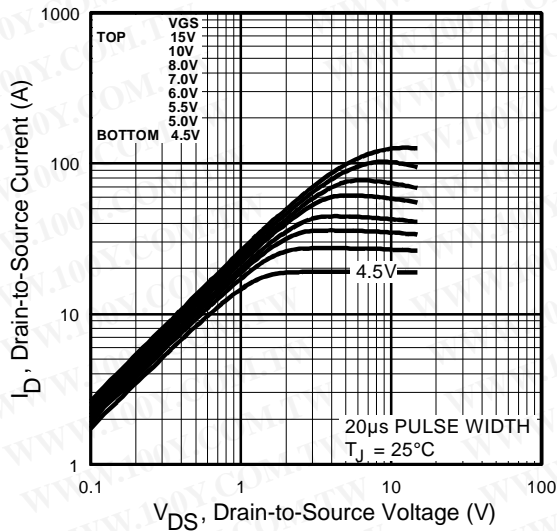


Fig 1. Typical Output Characteristics,
 $T_J = 25^\circ\text{C}$

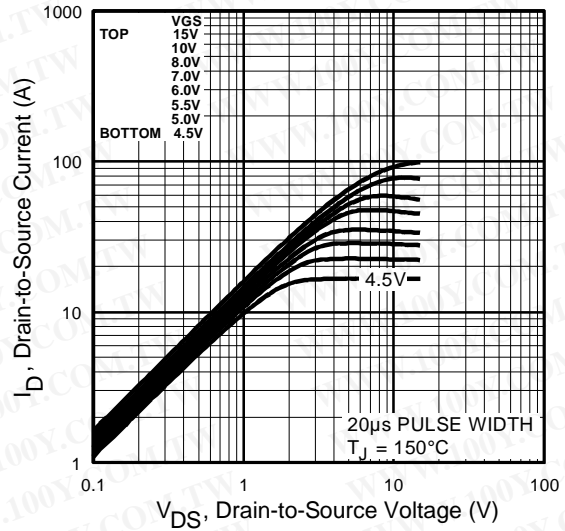


Fig 2. Typical Output Characteristics,
 $T_J = 150^\circ\text{C}$

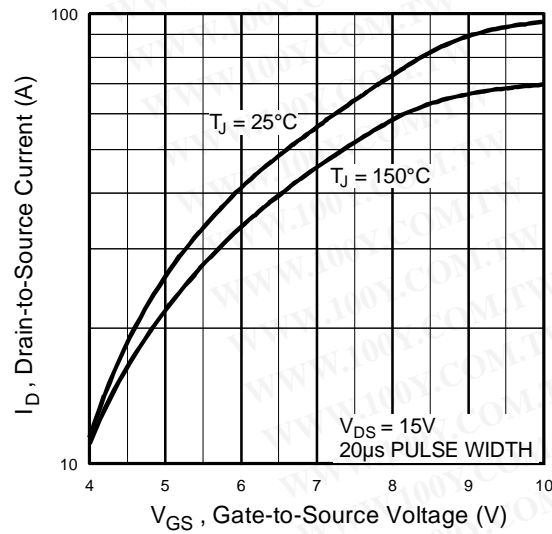


Fig 3. Typical Transfer Characteristics

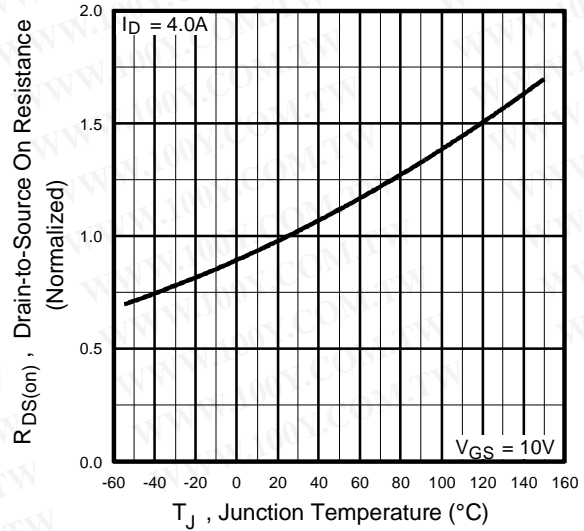


Fig 4. Normalized On-Resistance
 Vs. Temperature

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N-Channel

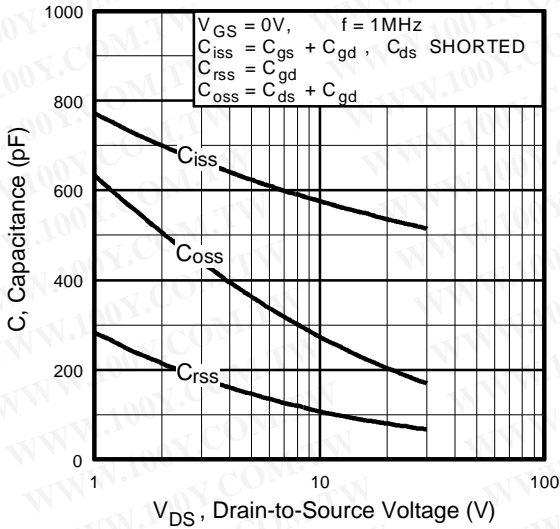


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

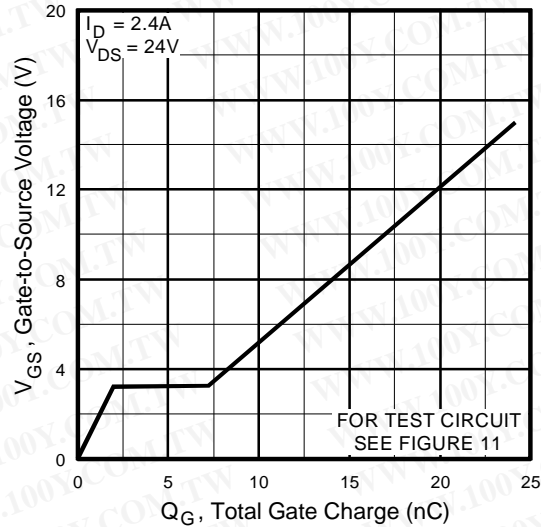


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

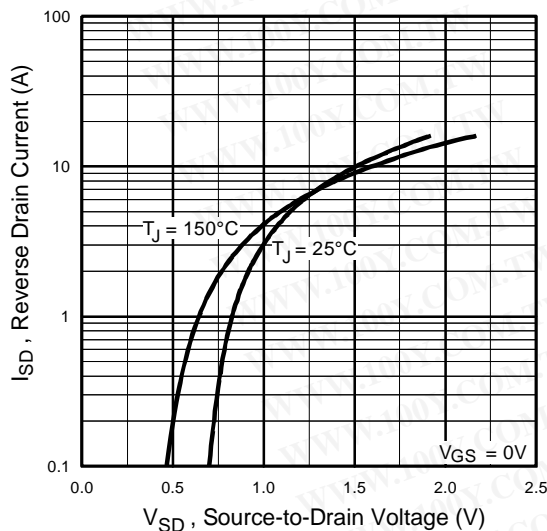


Fig 7. Typical Source-Drain Diode Forward Voltage

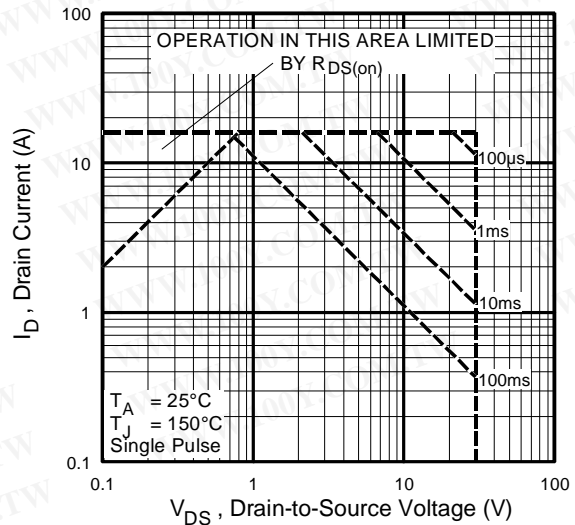


Fig 8. Maximum Safe Operating Area



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N-Channel

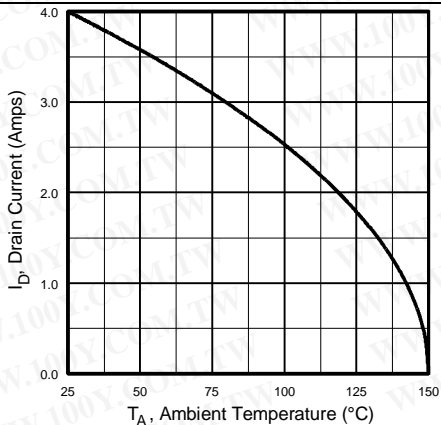


Fig 9. Max. Drain Current Vs. Ambient Temp.

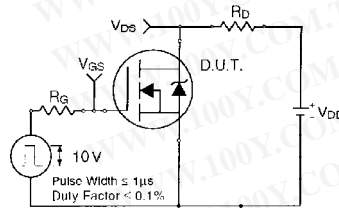


Fig 10a. Switching Time Test Circuit

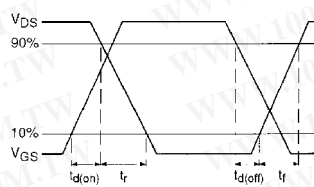


Fig 10b. Switching Time Waveforms

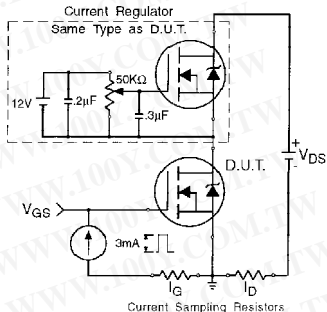


Fig 11a. Gate Charge Test Circuit

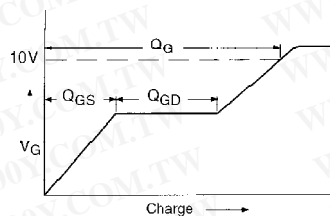


Fig 11b. Basic Gate Charge Waveform

P-Channel

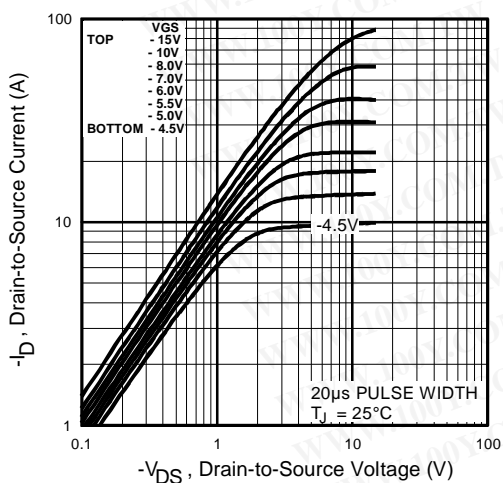


Fig 12. Typical Output Characteristics, $T_J = 25^\circ\text{C}$

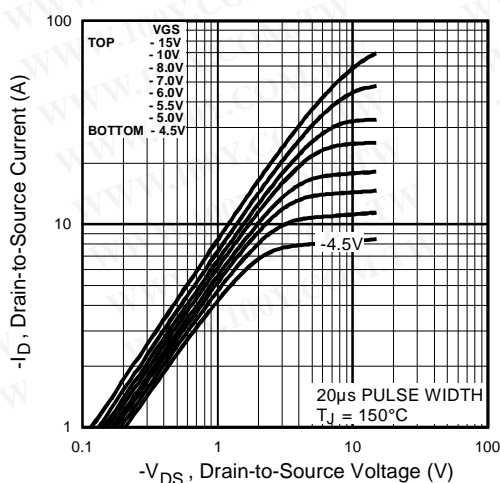


Fig 13. Typical Output Characteristics, $T_J = 150^\circ\text{C}$

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P-Channel

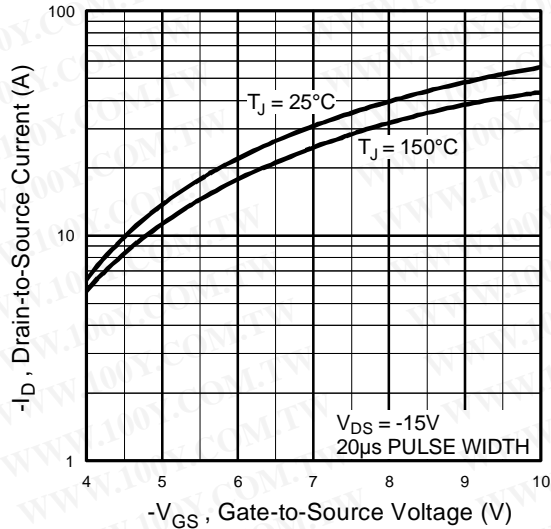


Fig 14. Typical Transfer Characteristics

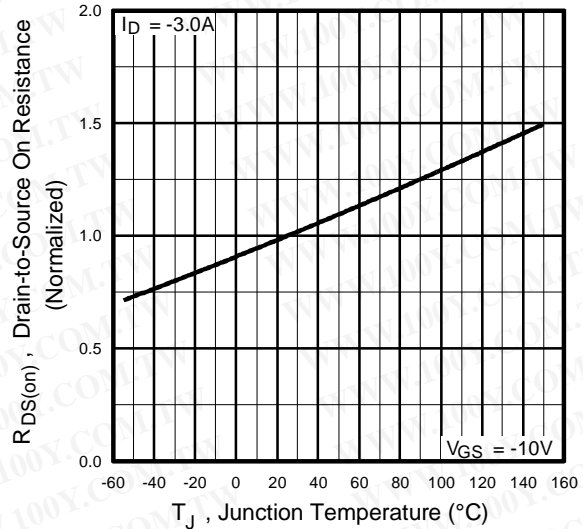


Fig 15. Normalized On-Resistance Vs. Temperature

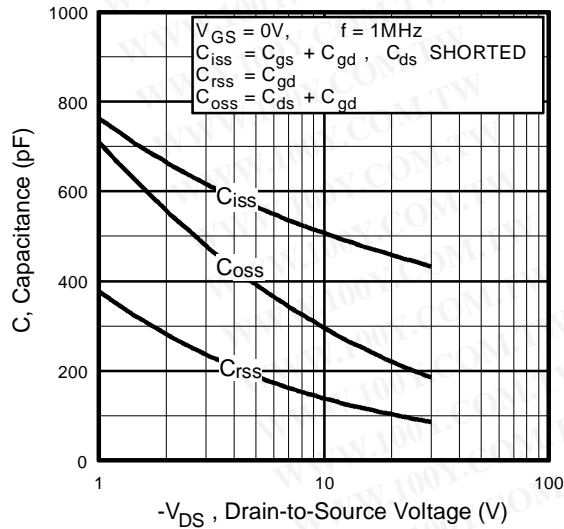


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

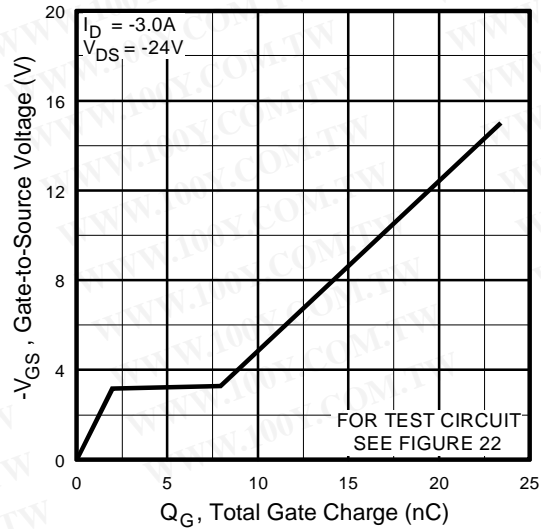


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage



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P-Channel

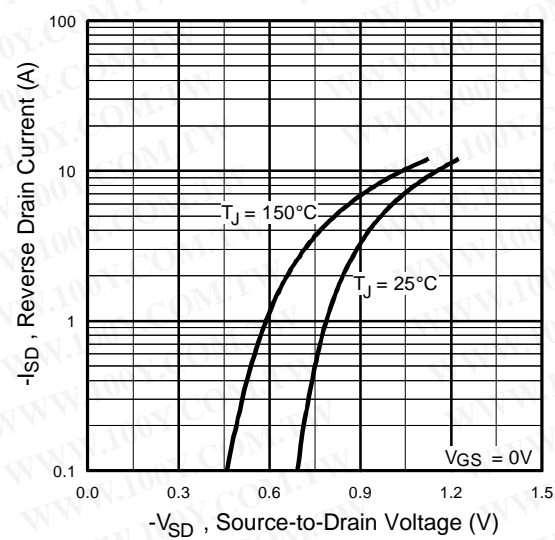


Fig 18. Typical Source-Drain Diode Forward Voltage

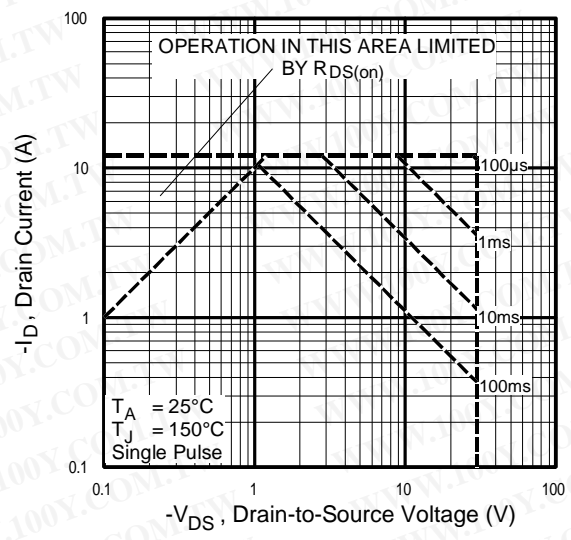


Fig 19. Maximum Safe Operating Area

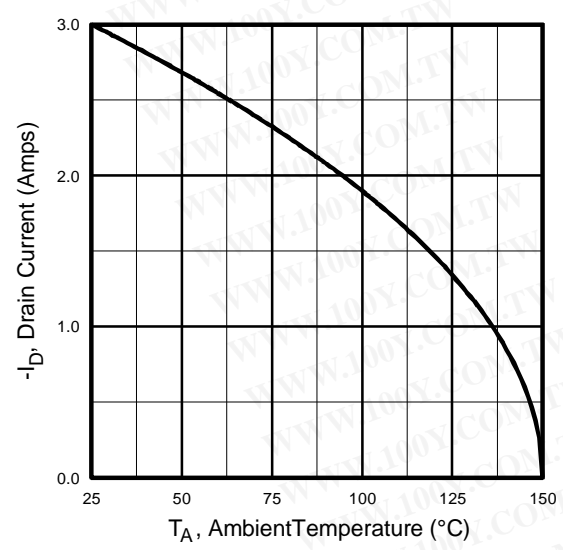


Fig 20. Max. Drain Current Vs. Ambient Temp.

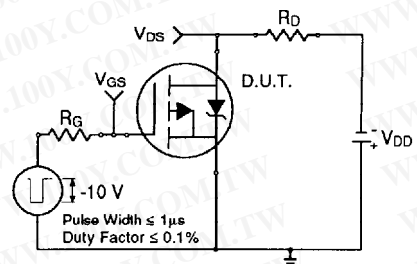


Fig 21a. Switching Time Test Circuit

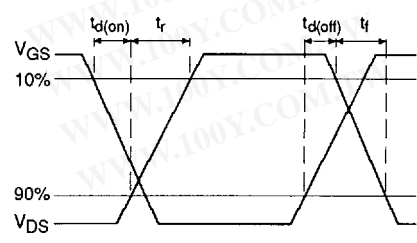


Fig 21b. Switching Time Waveforms

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P-Channel

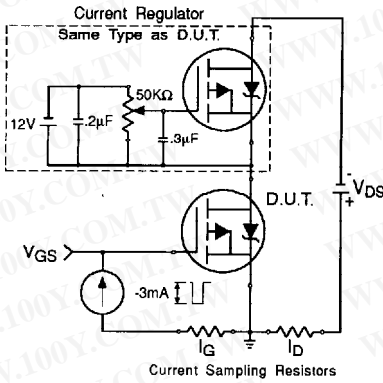


Fig 22b. Gate Charge Test Circuit

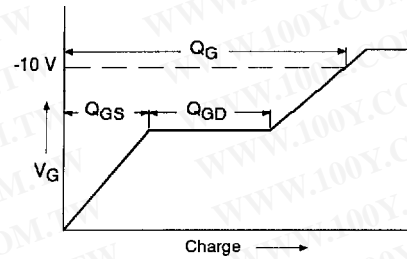


Fig 22b. Basic Gate Charge Waveform

N- and P-Channel

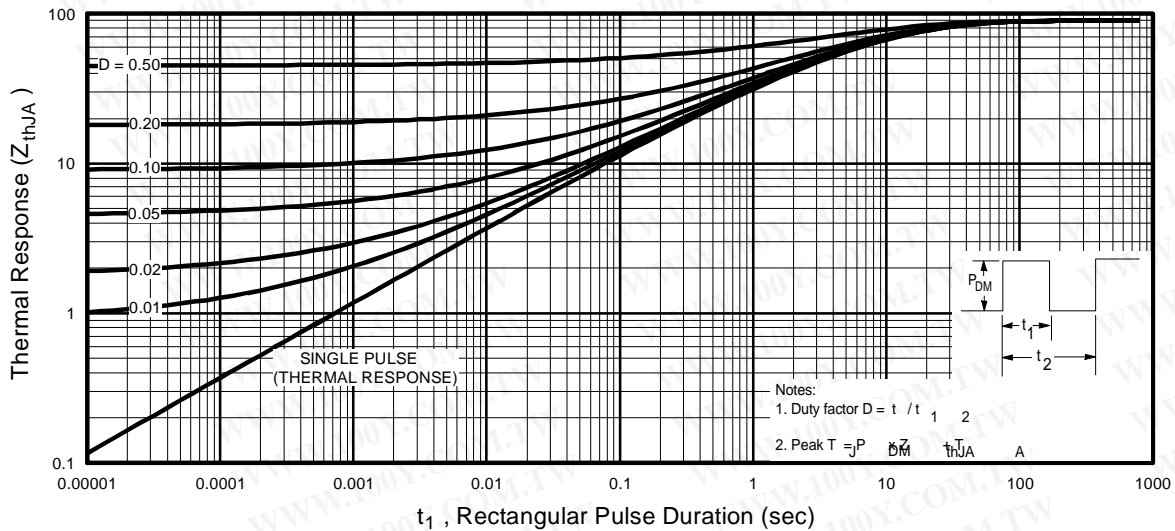


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Refer to the Appendix Section for the following:

Appendix A: Figure 24, Peak Diode Recovery dv/dt Test Circuit — See page 329.

Appendix B: Package Outline Mechanical Drawing — See page 332.

Appendix C: Part Marking Information — See page 332.

Appendix D: Tape and Reel Information — See page 336.