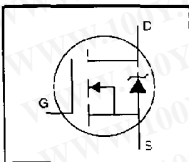


HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V_{GS} Rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Extremely High Frequency Operation
- Repetitive Avalanche Rated



$$V_{DSS} = 600V$$

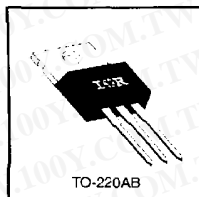
$$R_{DS(on)} = 1.2\Omega$$

$$I_D = 6.2A$$

Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new Low Charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power transistors for switching applications.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I _C @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10 V	6.2	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10 V	3.9	
I _{DM}	Pulsed Drain Current ①	25	
P _D @ T _C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS}	Single Pulse Avalanche Energy ②	530	mJ
I _{AS}	Avalanche Current ①	6.2	A
E _{AR}	Repetitive Avalanche Energy ②	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.0	V/ns
T _J	Operating Junction and Storage Temperature Range	-55 to +150	°C
T _{STG}	Soldering Temperature, for 10 seconds	300 (1.8mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	1.0	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
R _{θJA}	Junction-to-Ambient	—	—	62	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{BR(DSS)}	600	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{BR(DSS)/ΔT_J}	—	0.70	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	—	—	1.2	Ω	V _{GS} =10V, I _D =3.7A ③
V _{GS(th)}	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	3.7	—	—	S	V _{DS} =100V, I _D =3.7A ④
I _{DSS}	—	—	100	μA	V _{DS} =600V, V _{GS} =0V
I _{DSS}	—	—	500	μA	V _{DS} =460V, V _{GS} =0V, T _J =125°C
I _{DSS}	—	—	100	nA	V _{GS} =20V
I _{DSS}	—	—	-100	nA	V _{GS} =-20V
Q _g	—	—	39	nC	I _D =6.2A
Q _{gs}	—	—	10	nC	V _{DS} =360V
Q _{gd}	—	—	9	nC	V _{GS} =10V See Fig. 6 and 13 ⑤
t _{d(on)}	—	12	—	ns	V _{DD} =30CV
t _r	—	20	—	ns	I _D =6.2A
t _{d(off)}	—	27	—	ns	R _G =9.1Ω
t _f	—	17	—	ns	R _D =471Ω See Figure 10 ⑥
L _D	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	—	7.5	—	nH	
C _{iss}	—	1100	—	pF	V _{GS} =0V
C _{oss}	—	140	—	pF	V _{DS} =25V
C _{rss}	—	15	—	pF	f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	—	—	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	—	—	25	A	
V _{SD}	—	—	1.5	V	T _J =25°C, I _S =6.2A, V _{GS} =0V ⑦
t _r	—	440	680	ns	T _J =25°C, I _F =6.2A
Q _{rr}	—	2.1	3.2	μC	di/dt=100A/μs ⑧
t _{on}	—	—	—	ns	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=50V, starting T_J=25°C, L=25mH, R_G=25Ω, I_{AS}=6.2A (See Figure 12)
- ③ I_{DSS}≤6.2A, di/dt≤80A/μs, V_{DD}≤V_{BR(DSS)}, T_J≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%

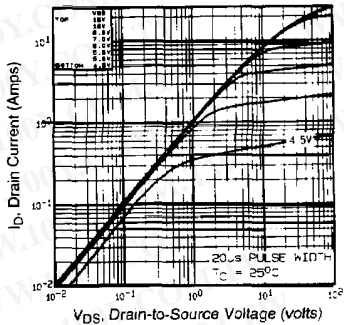


Fig 1. Typical Output Characteristics.
 $T_C=25^\circ\text{C}$

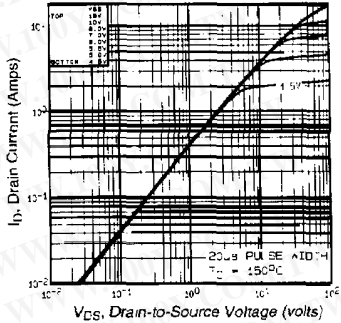


Fig 2. Typical Output Characteristics.
 $T_C=150^\circ\text{C}$

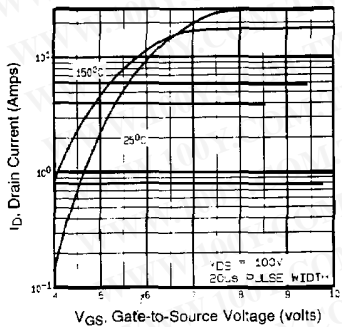


Fig 3. Typical Transfer Characteristics

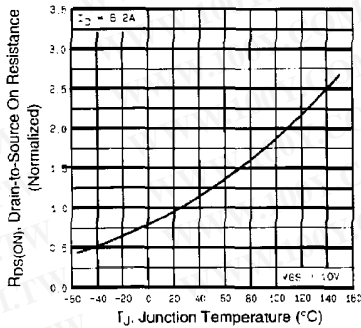


Fig 4. Normalized On-Resistance
 Vs. Temperature

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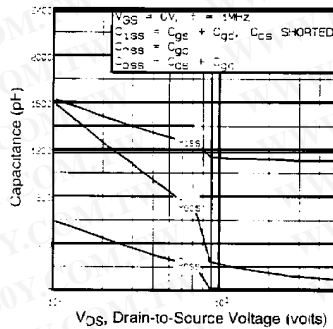


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

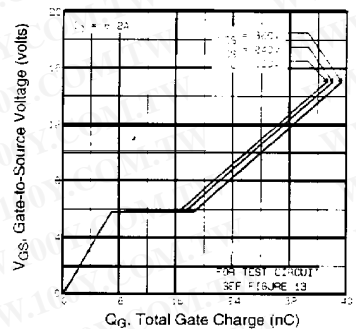


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

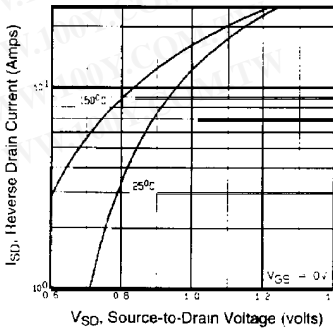


Fig 7. Typical Source-Drain Diode Forward Voltage

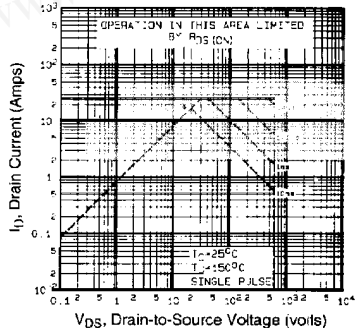


Fig 8. Maximum Safe Operating Area

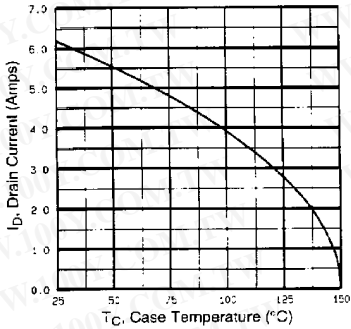


Fig 9. Maximum Drain Current Vs. Case Temperature

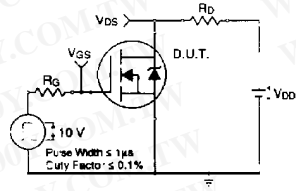


Fig 10a. Switching Time Test Circuit

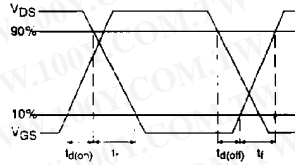


Fig 10b. Switching Time Waveforms

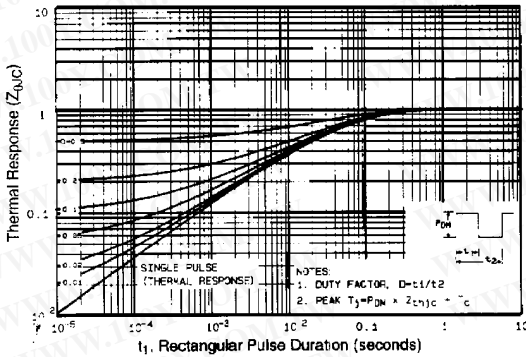


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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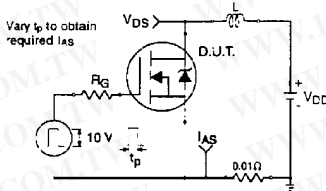


Fig 12a. Unclamped Inductive Test Circuit

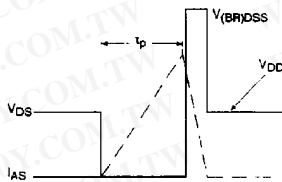


Fig 12b. Unclamped Inductive Waveforms

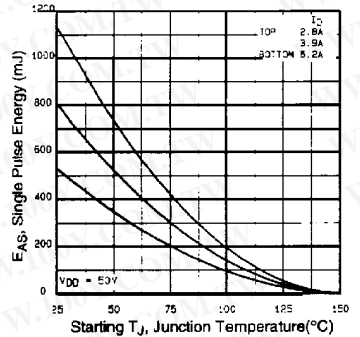


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

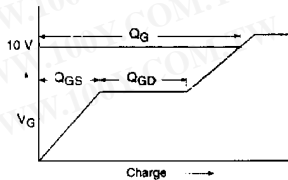


Fig 13a. Basic Gate Charge Waveform

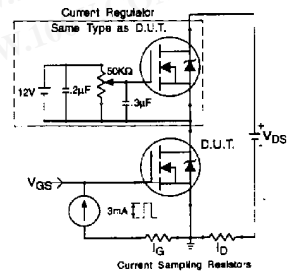


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

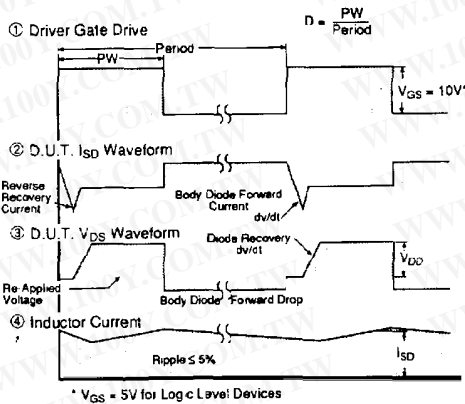
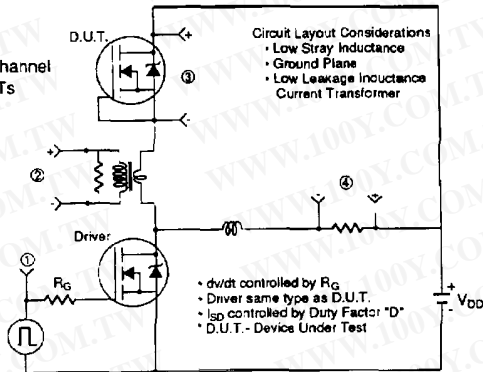
Appendix B: Package Outline Mechanical Drawing

Appendix C: Part Marking Information

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs



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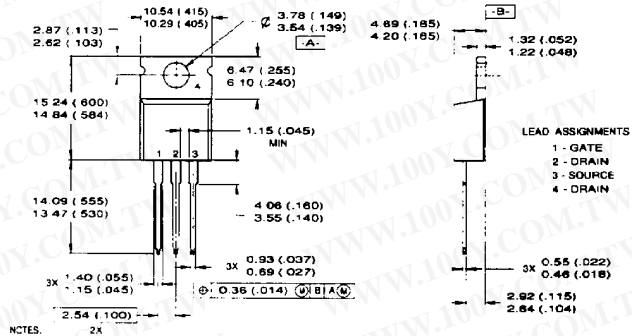


Package Outline

Appendix B

TO-220AB Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS
 1 - GATE
 2 - DRAIN
 3 - SOURCE
 4 - DRAIN

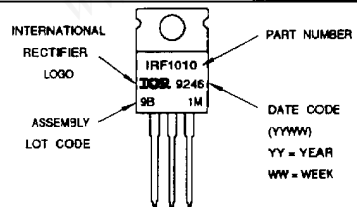
- NOTES:
 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M 1982
 2 CONTROLLING DIMENSION INCH
 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220-AB
 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

Appendix C

TO-220AB

EXAMPLE: THIS IS AN IRF1010 WITH
 ASSEMBLY LOT CODE 9B1M



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