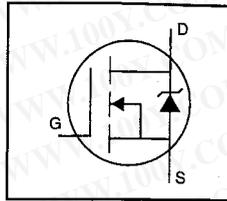


HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V_{GS} Rating
- Isolated Package
- High Voltage Isolation= 2.5KV_{RMS} ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Repetitive Avalanche Rated



$$V_{DSS} = 500V$$

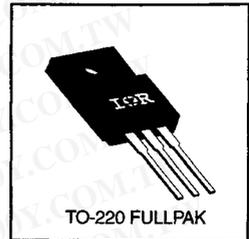
$$R_{DS(on)} = 0.85\Omega$$

$$I_D = 4.5A$$

Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced HEXFET technology, the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power transistors for switching applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware. The moulding compound used provides a high isolation capability and low thermal resistance between the tab and external heatsink.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	4.5	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.9	
I_{DM}	Pulsed Drain Current ①	18	
$P_D @ T_C = 25^\circ C$	Power Dissipation	40	W
	Linear Derating Factor	0.32	W/°C
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy ②	300	mJ
I_{AR}	Avalanche Current ①	4.5	A
E_{AR}	Repetitive Avalanche Energy ①	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to +150	°C
T_{STG}			
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.63	—	V°C	Reference to 25°C , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.85	Ω	$V_{GS}=10\text{V}$, $I_D=2.7\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
g_{fs}	Forward Transconductance	4.0	—	—	S	$V_{DS}=50\text{V}$, $I_D=4.8\text{A}$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$
		—	—	250		$V_{DS}=400\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20\text{V}$
Q_g	Total Gate Charge	—	—	39	nC	$I_D=8.0\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	10		$V_{DS}=400\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	19		$V_{GS}=10\text{V}$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD}=250\text{V}$
t_r	Rise Time	—	25	—		$I_D=8.0\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	27	—		$R_G=9.1\Omega$
t_f	Fall Time	—	19	—		$R_D=30\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1100	—	pF	$V_{GS}=0\text{V}$
C_{oss}	Output Capacitance	—	170	—		$V_{DS}=25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	18	—		$f=1.0\text{MHz}$ See Figure 5
C	Drain to Sink Capacitance	—	12	—		$f=1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	4.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	18		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J=25^\circ\text{C}$, $I_S=4.5\text{A}$, $V_{GS}=0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	490	740	ns	$T_J=25^\circ\text{C}$, $I_F=8.0\text{A}$
Q_{rr}	Reverse Recovery Charge	—	3.0	4.5	μC	$di/dt=100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② $V_{DD}=50\text{V}$, starting $T_J=25^\circ\text{C}$, $L=26\text{mH}$, $R_G=25\Omega$, $I_{AS}=4.5\text{A}$ (See Figure 12)
- ③ $I_{SD}\leq 8.0\text{A}$, $di/dt\leq 100\text{A}/\mu\text{s}$, $V_{DD}\leq V_{(BR)DSS}$, $T_J\leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$
- ⑤ $t=60\text{s}$, $f=60\text{Hz}$

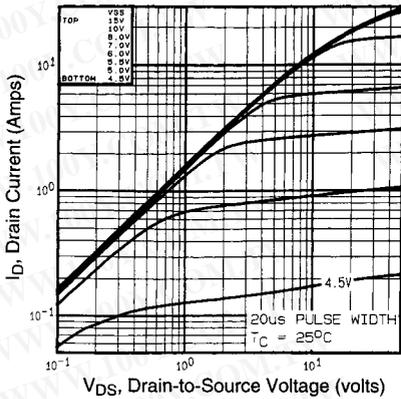


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

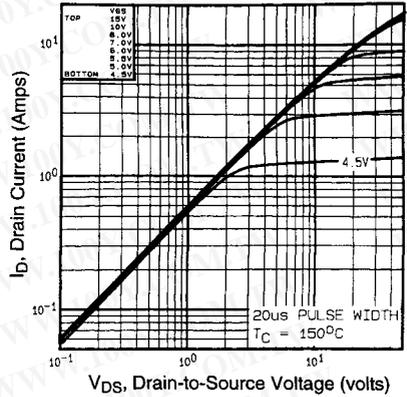


Fig 2. Typical Output Characteristics,
 $T_C=150^\circ\text{C}$

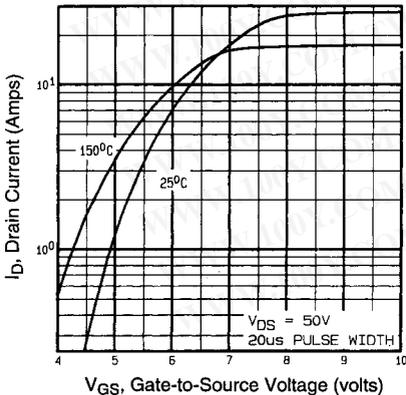


Fig 3. Typical Transfer Characteristics

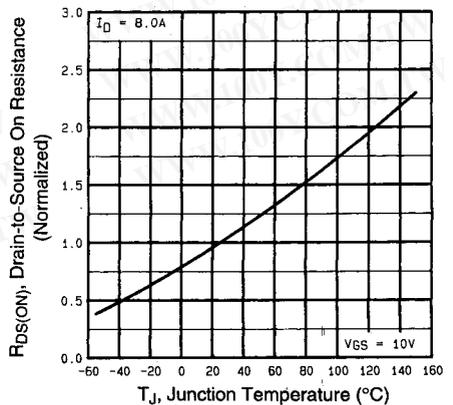


Fig 4. Normalized On-Resistance
Vs. Temperature

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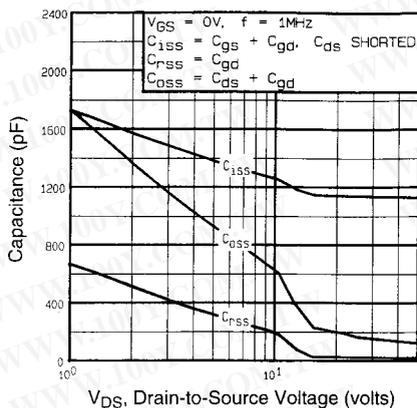


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

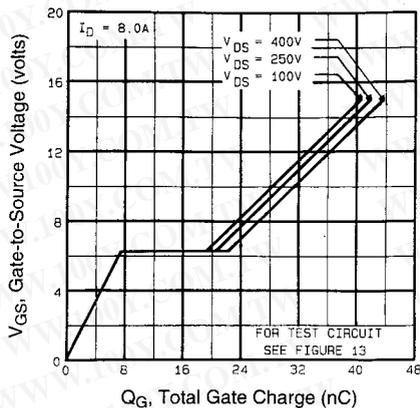


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

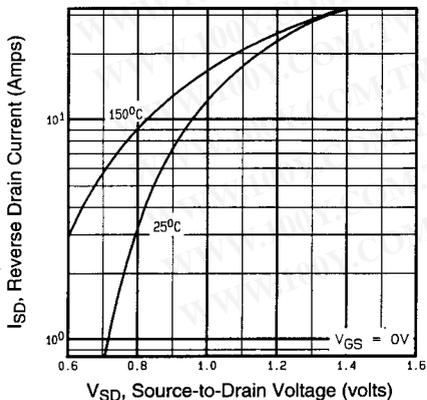


Fig 7. Typical Source-Drain Diode Forward Voltage

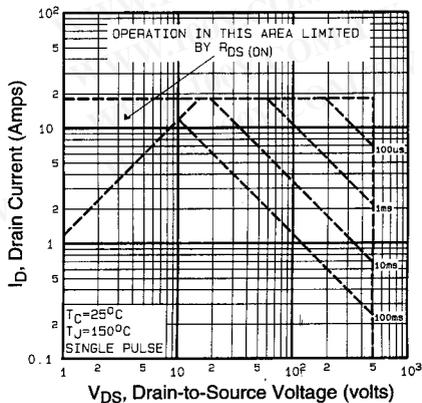


Fig 8. Maximum Safe Operating Area

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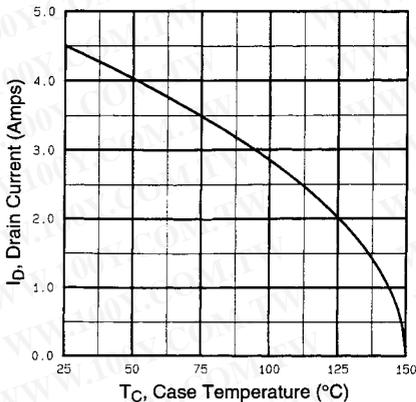


Fig 9. Maximum Drain Current Vs. Case Temperature

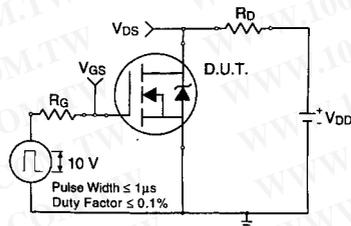


Fig 10a. Switching Time Test Circuit

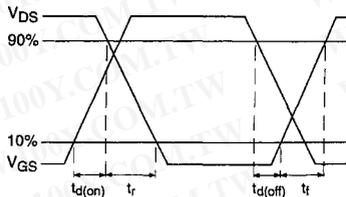


Fig 10b. Switching Time Waveforms

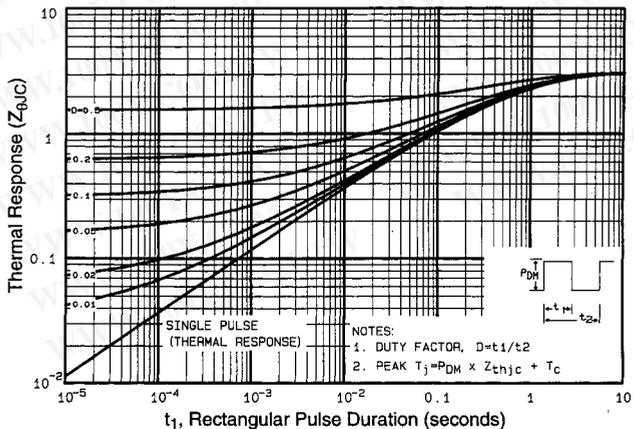


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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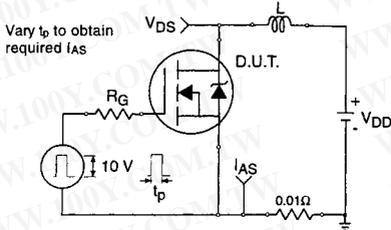


Fig 12a. Unclamped Inductive Test Circuit

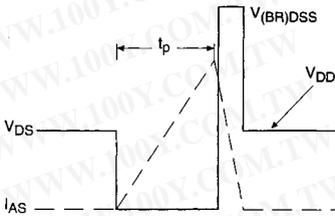


Fig 12b. Unclamped Inductive Waveforms

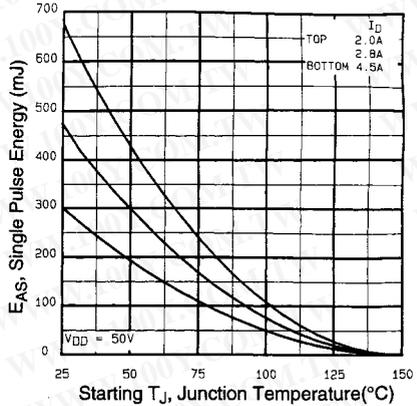


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

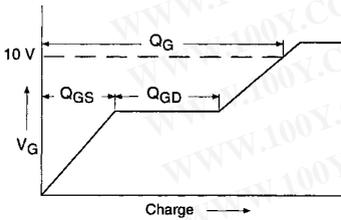


Fig 13a. Basic Gate Charge Waveform

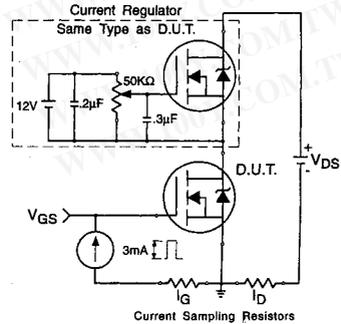


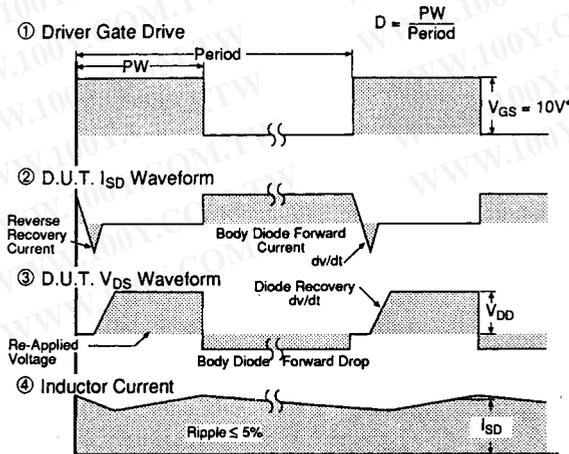
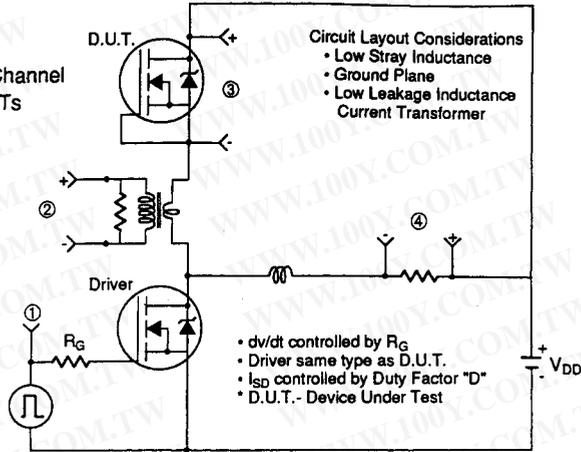
Fig 13b. Gate Charge Test Circuit

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Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs



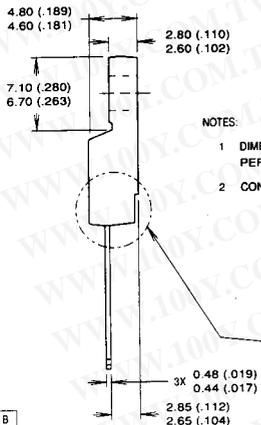
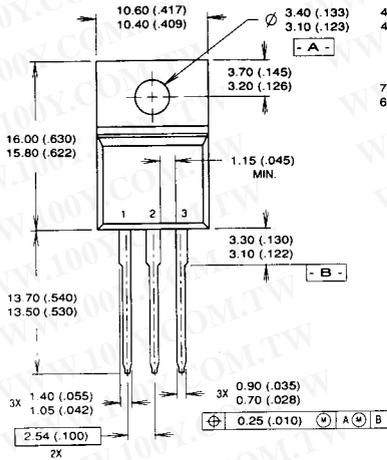
* $V_{GS} = 5V$ for Logic Level Devices

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Package Outline

TO-220 FullPak Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

NOTES:

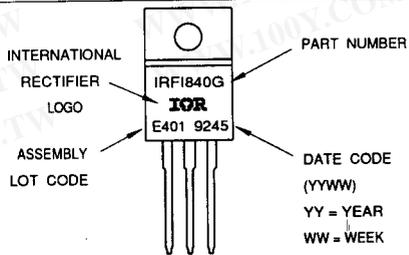
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION: INCH

MINIMUM CREEPAGE DISTANCE BETWEEN A-B-C-D = 4.80 (.189)

Part Marking Information

TO-220 FULL-PAK

EXAMPLE: THIS IS AN IRFI840G WITH ASSEMBLY LOT CODE E401



Appendix C



Printed on Signet recycled offset: made from 50% recycled waste paper, including 10% de-inked, post-consumer waste.



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