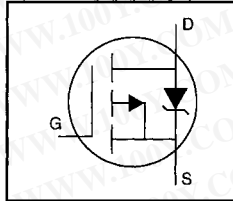


## HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ③
- Sink to Lead Creepage Dist.= 4.8mm
- P-Channel
- 175°C Operating Temperature
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = -100V$$

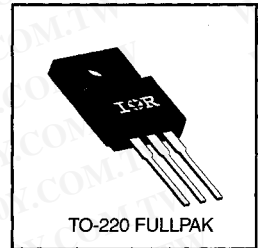
$$R_{DS(on)} = 0.60\Omega$$

$$I_D = -5.2A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



DATA SHEETS

### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-5.2	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-3.6	
$I_{DM}$	Pulsed Drain Current ①	-21	
$P_D @ T_C = 25^\circ C$	Power Dissipation	37	W
	Linear Derating Factor	0.24	W/°C
$V_{GS}$	Gate-to-Source Voltage	±20	V
$E_{AS}$	Single Pulse Avalanche Energy ②	300	mJ
$I_{AR}$	Avalanche Current ①	-5.2	A
$E_{AR}$	Repetitive Avalanche Energy ①	3.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
$T_J$	Operating Junction and	-55 to +175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS}=0\text{V}$ , $I_D=-250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.10	—	$\text{V}/^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.60	$\Omega$	$V_{GS}=-10\text{V}$ , $I_D=-3.1\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$
$g_{fs}$	Forward Transconductance	1.9	—	—	S	$V_{DS}=-50\text{V}$ , $I_D=-3.1\text{A}$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	-100	$\mu\text{A}$	$V_{DS}=-100\text{V}$ , $V_{GS}=0\text{V}$
		—	—	-500		$V_{DS}=-80\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS}=-20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS}=20\text{V}$
$Q_g$	Total Gate Charge	—	—	18	nC	$I_D=-6.8\text{A}$
$Q_{gs}$	Gate-to-Source Charge	—	—	3.0		$V_{DS}=-80\text{V}$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	9.0		$V_{GS}=-10\text{V}$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.6	—	ns	$V_{DD}=50\text{V}$
$t_r$	Rise Time	—	29	—		$I_D=-6.8\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		$R_G=18\Omega$
$t_f$	Fall Time	—	25	—		$R_D=7.1\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	390	—	pF	$V_{GS}=0\text{V}$
$C_{oss}$	Output Capacitance	—	170	—		$V_{DS}=-25\text{V}$
$C_{rSS}$	Reverse Transfer Capacitance	—	45	—		$f=1.0\text{MHz}$ See Figure 5
C	Drain to Sink Capacitance	—	12	—		$f=1.0\text{MHz}$

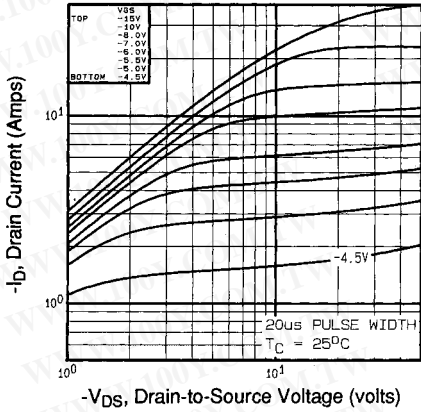

**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-5.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	-21		
$V_{SD}$	Diode Forward Voltage	—	—	-6.3	V	$T_J=25^\circ\text{C}$ , $I_S=-5.2\text{A}$ , $V_{GS}=0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	100	200	ns	$T_J=25^\circ\text{C}$ , $I_F=-6.8\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	0.33	0.66	$\mu\text{C}$	$di/dt=100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

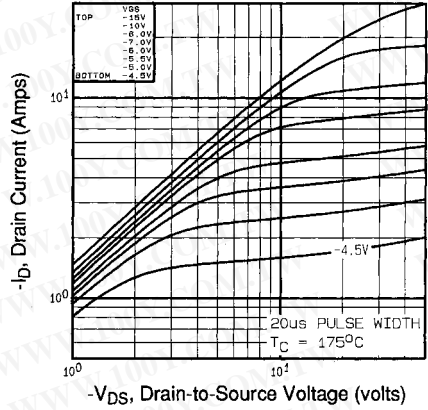
Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=-25\text{V}$ , starting  $T_J=25^\circ\text{C}$ ,  $L=16\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=-5.2\text{A}$  (See Figure 12)
- ③  $I_{SD}\leq-6.8\text{A}$ ,  $di/dt\leq 110\text{A}/\mu\text{s}$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$
- ⑤  $t=60\text{ns}$ ,  $f=60\text{Hz}$

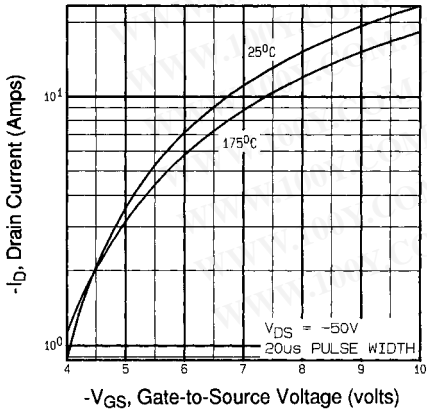
勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)



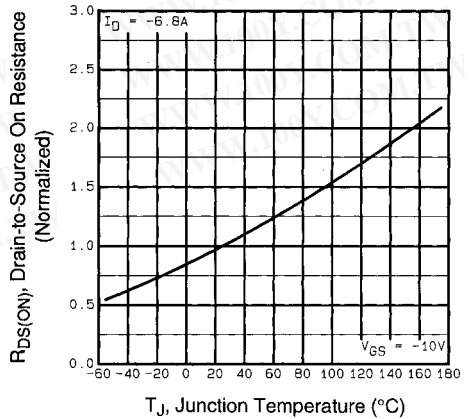
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=175^\circ\text{C}$

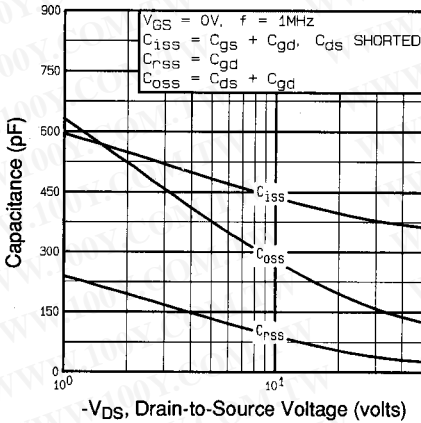


**Fig 3.** Typical Transfer Characteristics

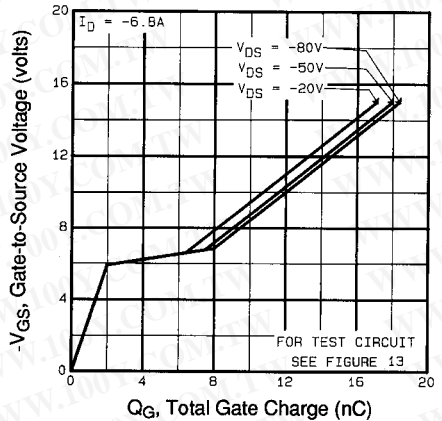


**Fig 4.** Normalized On-Resistance  
 Vs. Temperature

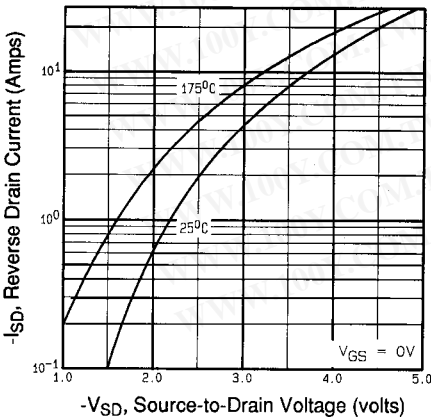
DATA SHEETS



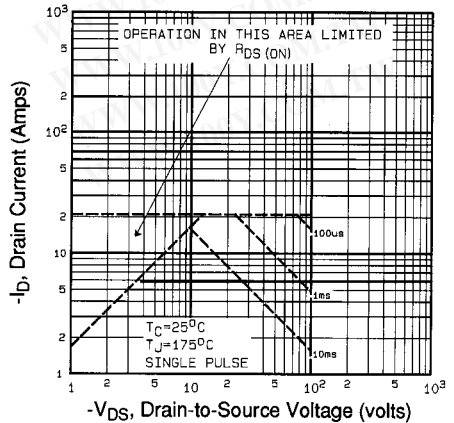
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



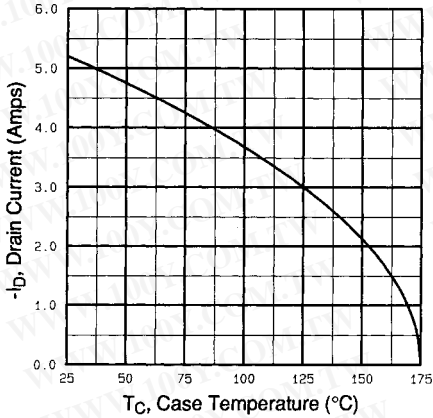
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



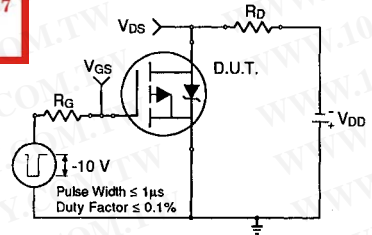
**Fig 7.** Typical Source-Drain Diode Forward Voltage



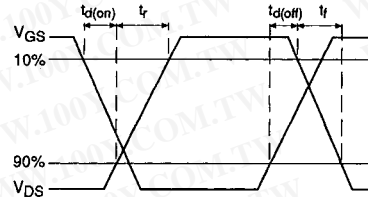
**Fig 8.** Maximum Safe Operating Area



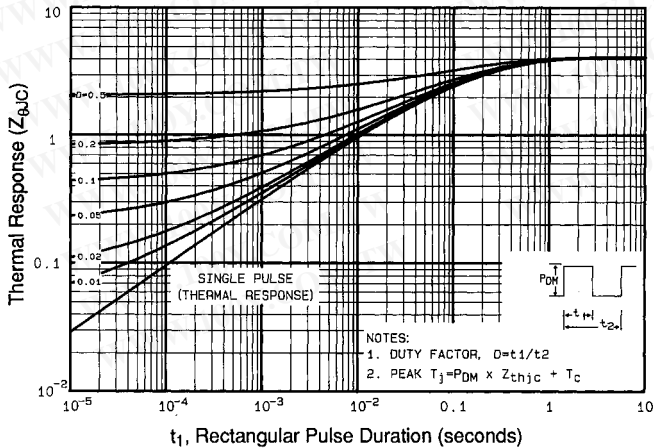
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

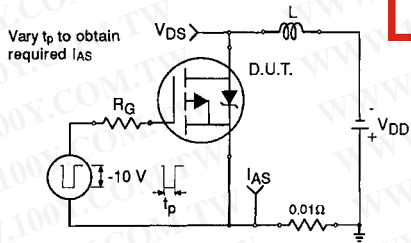


**Fig 10b.** Switching Time Waveforms

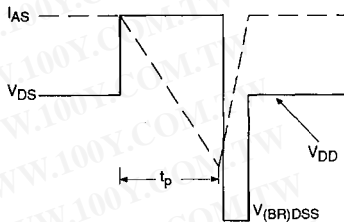


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

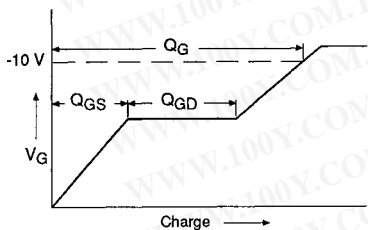
DATA SHEETS



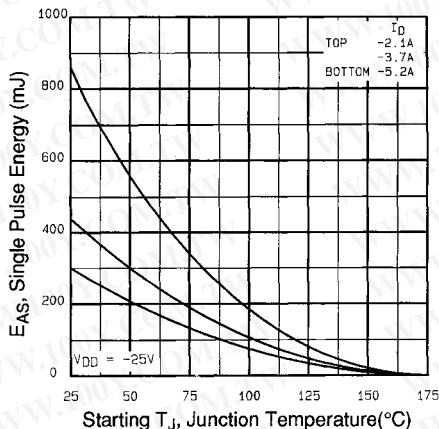
**Fig 12a.** Unclamped Inductive Test Circuit



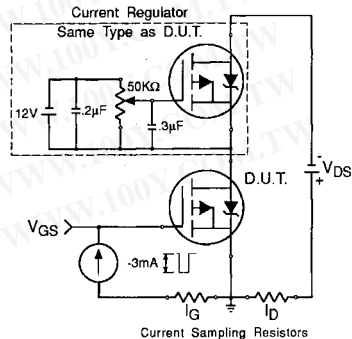
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1506

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

**Appendix C:** Part Marking Information – See page 1517