

PD - 94081B

International
IR Rectifier

SMPS MOSFET

IRFP31N50L

HEXFET® Power MOSFET

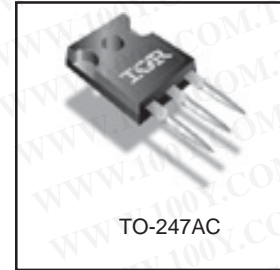
Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications

V _{DSS}	R _{DS(on) typ.}	T _{rr typ.}	I _D
500V	0.15Ω	170ns	31A

Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.



Absolute Maximum Ratings

Parameter	Max.	Units
I _D @ T _C = 25°C	31	A
I _D @ T _C = 100°C	20	
I _{DM}	124	W
P _D @ T _C = 25°C	460	
	3.7	W/°C
V _{GS}	±30	V
dv/dt	16	V/ns
T _J T _{STG}	-55 to + 150	°C
	300 (1.6mm from case)	
	10lb·in (1.1N·m)	

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	31	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	124		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 31A, V _{GS} = 0V ②
t _{rr}	Reverse Recovery Time	—	170	250	ns	T _J = 25°C, I _F = 31A
		—	220	330		T _J = 125°C, di/dt = 100A/μs ②
Q _{rr}	Reverse Recovery Charge	—	570	860	nC	T _J = 25°C, I _S = 31A, V _{GS} = 0V ②
		—	1.2	1.8		μC
I _{RSM}	Reverse Recovery Current	—	7.9	12	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.28	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.15	0.18	Ω	$V_{GS} = 10V, I_D = 19A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -30V$
R_G	Internal Gate Resistance	—	1.1	—	Ω	$f = 1MHz, \text{open drain}$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	15	—	—	S	$V_{DS} = 50V, I_D = 19A$
Q_g	Total Gate Charge	—	—	210	nC	$I_D = 31A$
Q_{gs}	Gate-to-Source Charge	—	—	58	nC	$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	100	nC	$V_{GS} = 10V, \text{See Fig. 7 \& 15 } \textcircled{4}$
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	$V_{DD} = 250V$
t_r	Rise Time	—	115	—	ns	$I_D = 31A$
$t_{d(off)}$	Turn-Off Delay Time	—	54	—	ns	$R_G = 4.3\Omega$
t_f	Fall Time	—	53	—	ns	$V_{GS} = 10V, \text{See Fig. 14a \& 14b } \textcircled{4}$
C_{iss}	Input Capacitance	—	5000	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	553	—	pF	$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	59	—	pF	$f = 1.0MHz, \text{See Fig. 5}$
C_{oss}	Output Capacitance	—	6630	—	pF	$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	155	—	pF	$V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	276	—	pF	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V \textcircled{5}$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	200	—	pF	

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	460	mJ
I_{AR}	Avalanche Current ①	—	31	A
E_{AR}	Repetitive Avalanche Energy ①	—	46	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	0.26	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ⑥	—	40	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}, L = 1mH, R_G = 25\Omega, I_{AS} = 31A$ (See Figure 12).
- ③ $I_{SD} = 31A, di/dt \leq 630A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ R_{θ} is measured at T_J approximately 90°C

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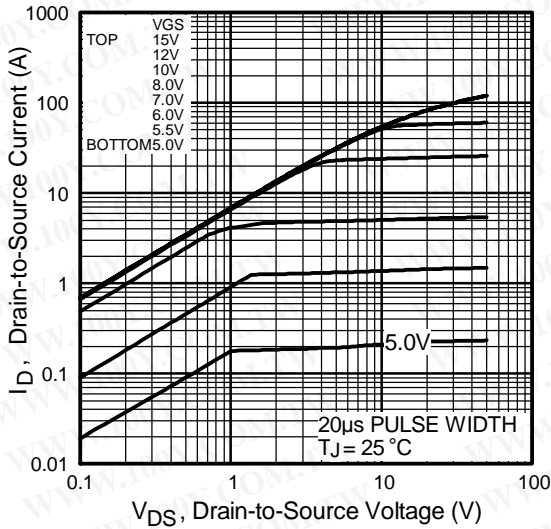


Fig 1. Typical Output Characteristics

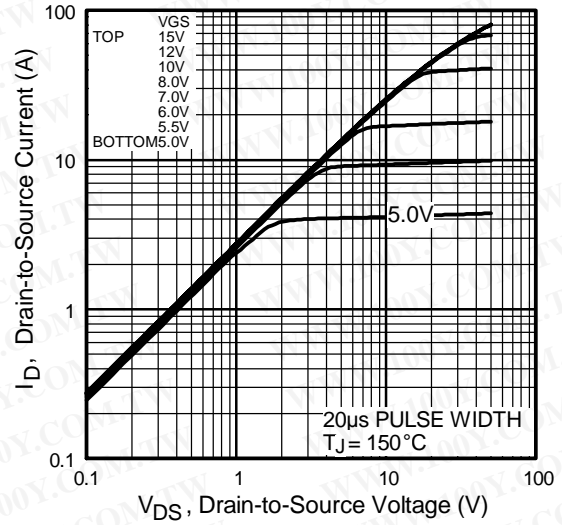


Fig 2. Typical Output Characteristics

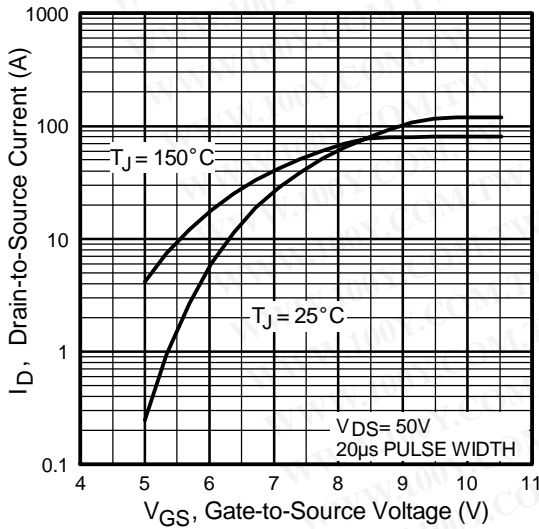


Fig 3. Typical Transfer Characteristics

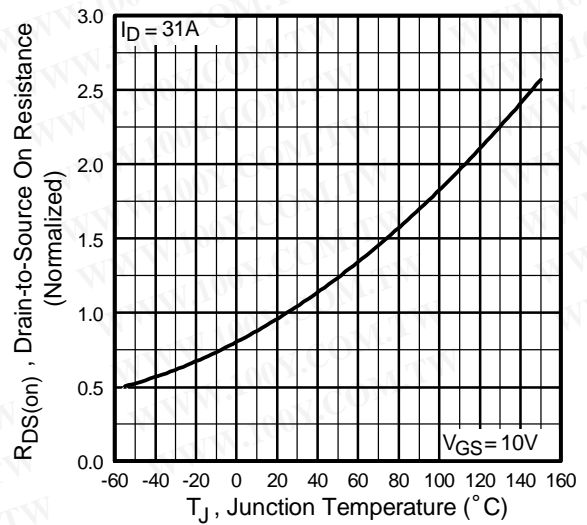


Fig 4. Normalized On-Resistance Vs. Temperature

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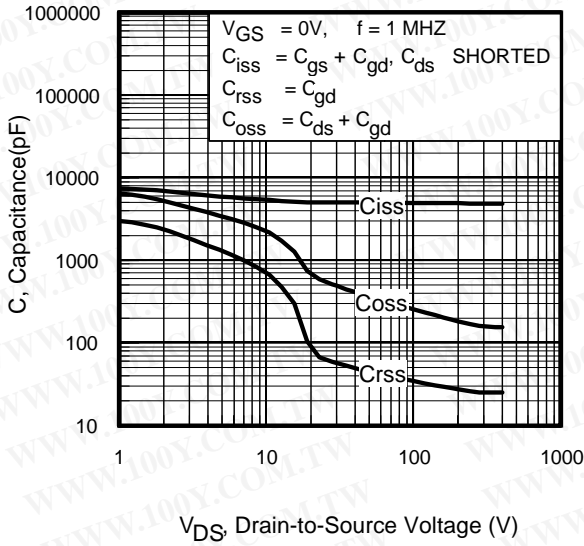


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

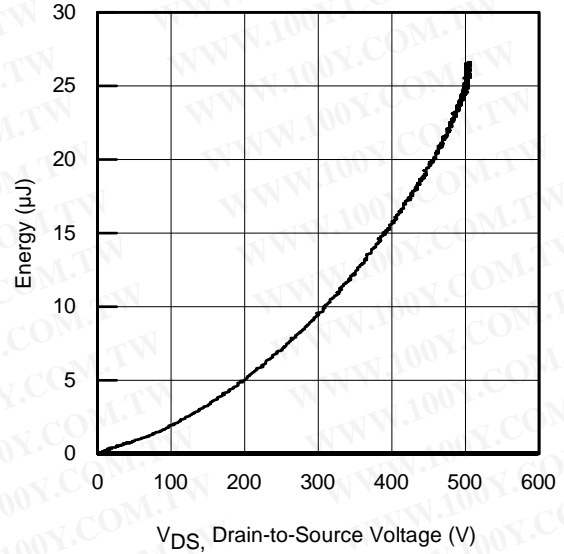


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

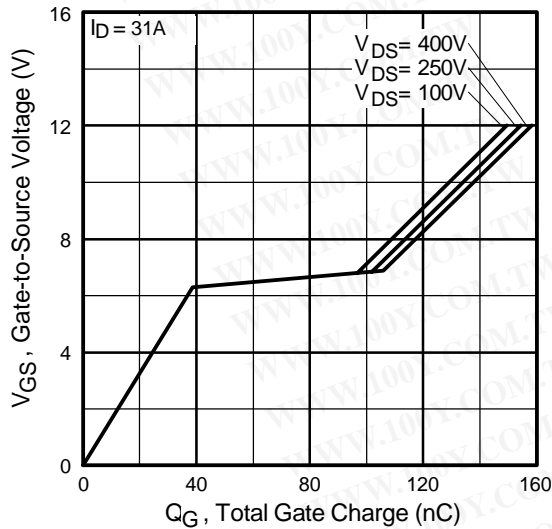


Fig 7. Typical Gate Charge vs. Gate-to-Source Voltage

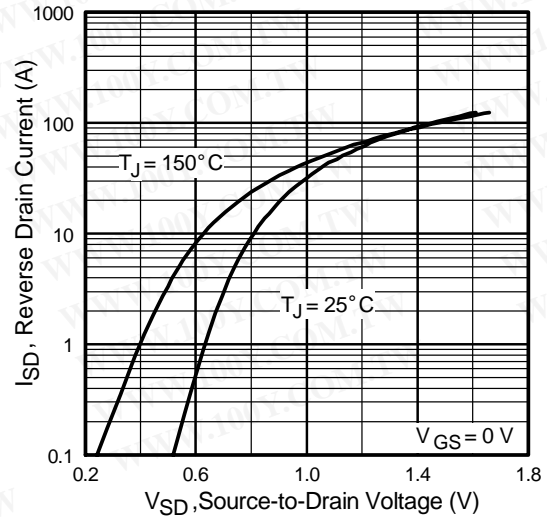


Fig 8. Typical Source-Drain Diode Forward Voltage

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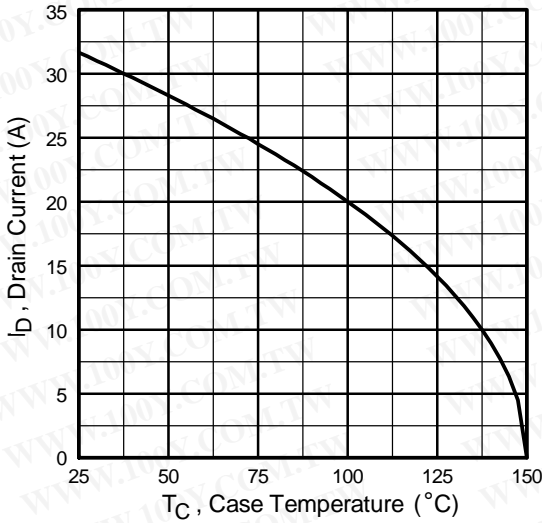


Fig 9. Maximum Drain Current vs. Case Temperature

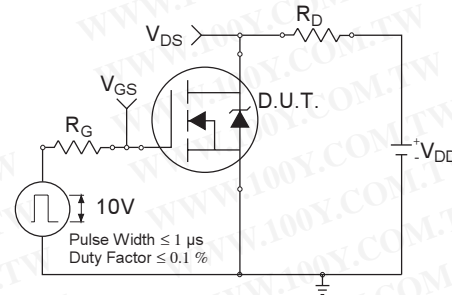


Fig 10a. Switching Time Test Circuit

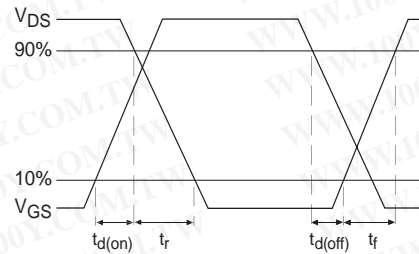


Fig 10b. Switching Time Waveforms

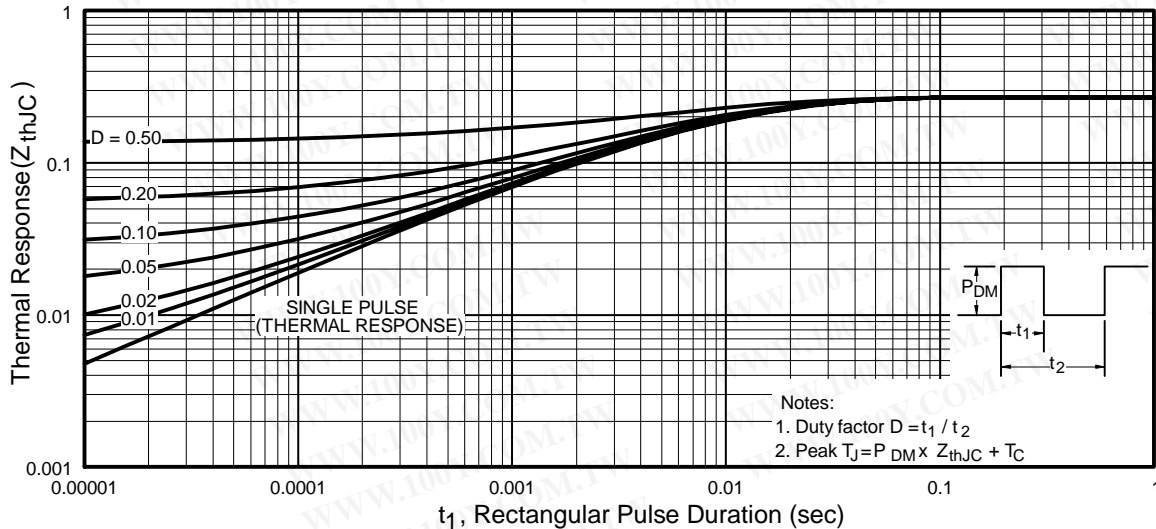


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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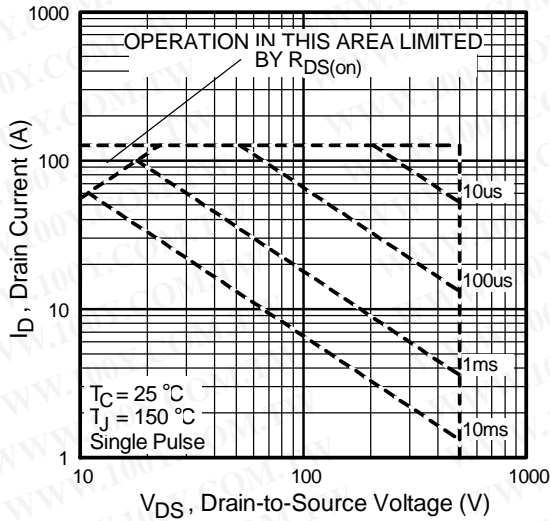


Fig 12. Maximum Safe Operating Area

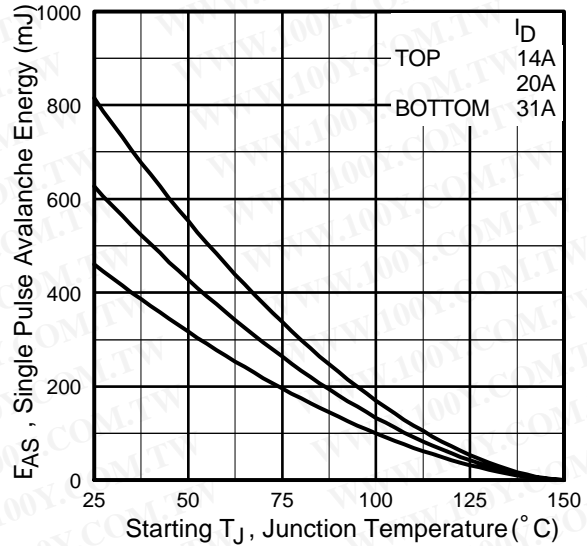


Fig 13. Maximum Avalanche Energy Vs. Drain Current

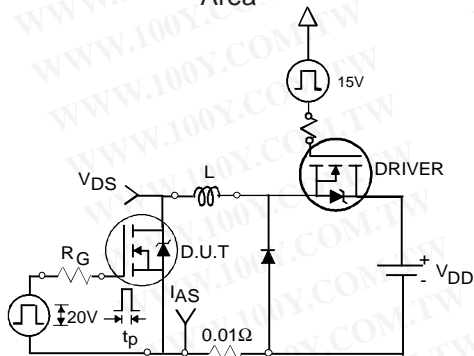


Fig 14a. Unclamped Inductive Test Circuit

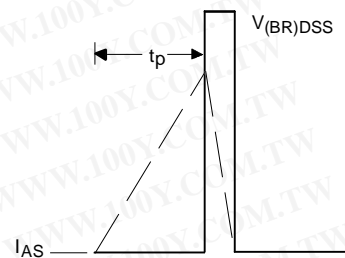


Fig 14b. Unclamped Inductive Waveforms

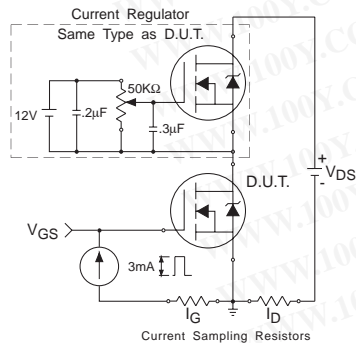


Fig 15a. Gate Charge Test Circuit

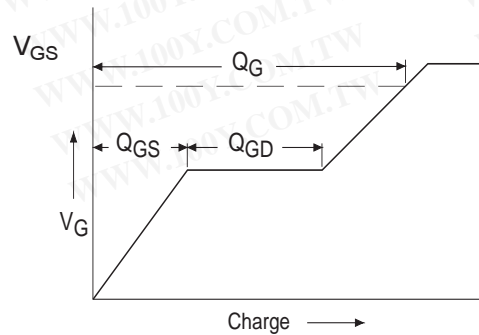
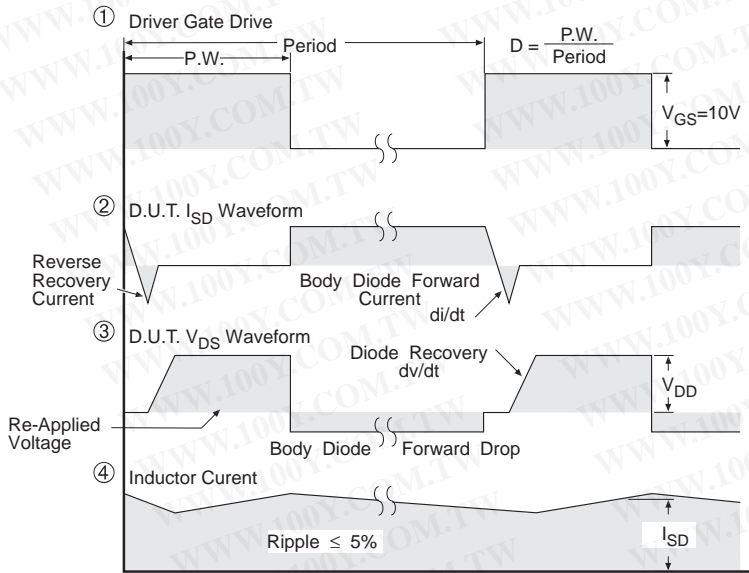
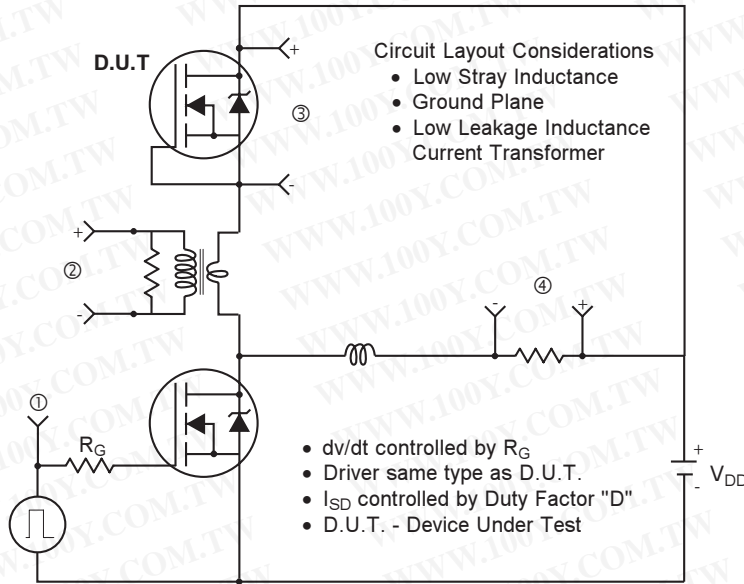


Fig 15b. Basic Gate Charge Waveform

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Peak Diode Recovery dv/dt Test Circuit



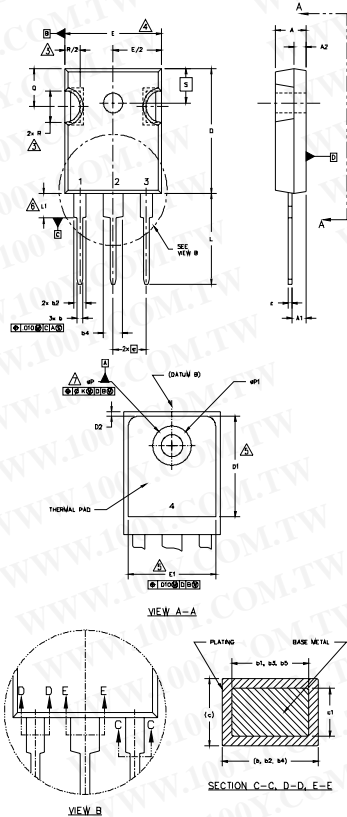
* $V_{GS} = 5V$ for Logic Level Devices

Fig 16. For N-Channel HEXFET® Power MOSFETs

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TO-247AC Package Outline Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH; MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91]
8. B. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION e.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.067	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.37	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.034	0.38	0.86	
c1	.015	.030	0.38	0.76	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.030	0.51	0.76	
E	.602	.625	15.29	15.87	4
E1	.540	-	13.72	-	
e	.215 BSC		5.46 BSC		
Øk	.010		2.54		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
N	3		7.62 BSC		
ØP	.140	.144	3.56	3.66	
ØP1	.275	-	6.99	-	
Q	.209	.224	5.31	5.69	
R	.178	.216	4.52	5.49	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

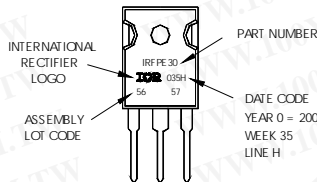
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30 WITH ASSEMBLY LOT CODE 5657 ASSEMBLED ON WW 35, 2000 IN THE ASSEMBLY LINE "H"
 Note: "P" in assembly line position indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the industrial market.
 Qualification Standards can be found on IR's Web site.

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