

International **IR** Rectifier

- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRL1004L) is available for low-profile application.

Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V ^⑥	130 ^⑤	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V ^⑥	92 ^⑤	
I _{DM}	Pulsed Drain Current ^{①⑥}	520	
P _D @ T _A = 25°C	Power Dissipation	3.8	W
P _D @ T _C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 16	V
E _{AS}	Single Pulse Avalanche Energy ^⑥	700	mJ
I _{AR}	Avalanche Current ^①	78	A
E _{AR}	Repetitive Avalanche Energy ^①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ^{③⑥}	5.0	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.75	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mounted, steady-state)*	—	40	

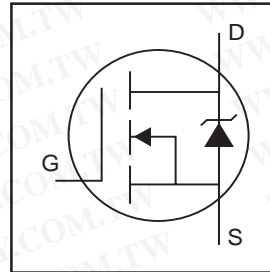
www.irf.com

PD - 91644A

IRL1004S

IRL1004L

HEXFET® Power MOSFET



V _{DSS} = 40V
R _{DS(on)} = 0.0065Ω
I _D = 130A ^⑤



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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.04	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.0065	Ω	$V_{GS} = 10V, I_D = 78A$ ④
		—	—	0.009		$V_{GS} = 4.5V, I_D = 65A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	63	—	—	S	$V_{DS} = 25V, I_D = 78A$ ⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 32V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	100	nC	$I_D = 78A$
Q_{gs}	Gate-to-Source Charge	—	—	32		$V_{DS} = 32V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	43		$V_{GS} = 4.5V$, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 20V$,
t_r	Rise Time	—	210	—		$I_D = 78A$,
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		$R_G = 2.5\Omega$,
t_f	Fall Time	—	14	—		$R_D = 0.18\Omega$, See Fig. 10 ④⑥
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	5330	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1480	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	320	—		$f = 1.0MHz$, See Fig. 5⑤⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) ⑦	—	—	130 ⑤	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑦	—	—	520		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 78A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	78	120	ns	$T_J = 25^\circ\text{C}, I_F = 78A$
Q_{rr}	Reverse Recovery Charge	—	180	270	nC	$di/dt = 100A/\mu s$ ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.23mH$
 $R_G = 25\Omega, I_{AS} = 78A$. (See Figure 12)
- ③ $I_{SD} \leq 78A, di/dt \leq 370A/\mu s, V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4
- ⑥ Uses IRL1004 data and test conditions

* When mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

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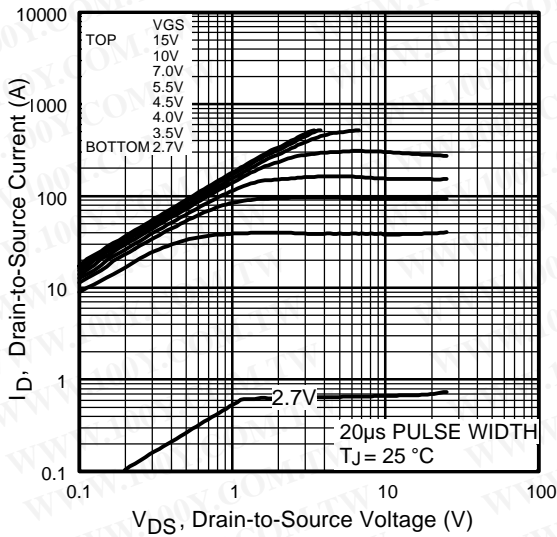


Fig 1. Typical Output Characteristics

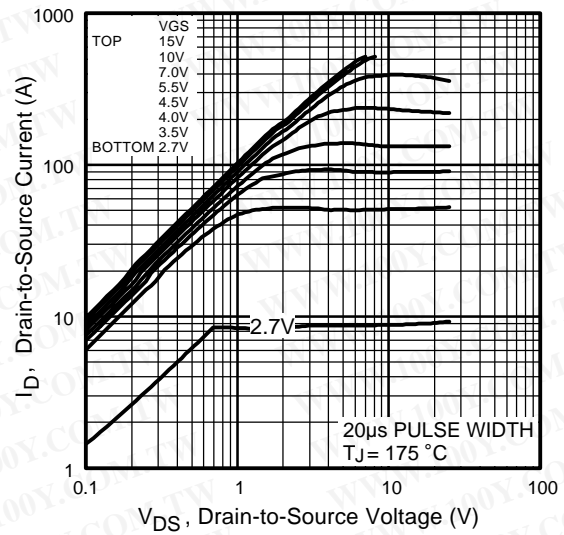


Fig 2. Typical Output Characteristics

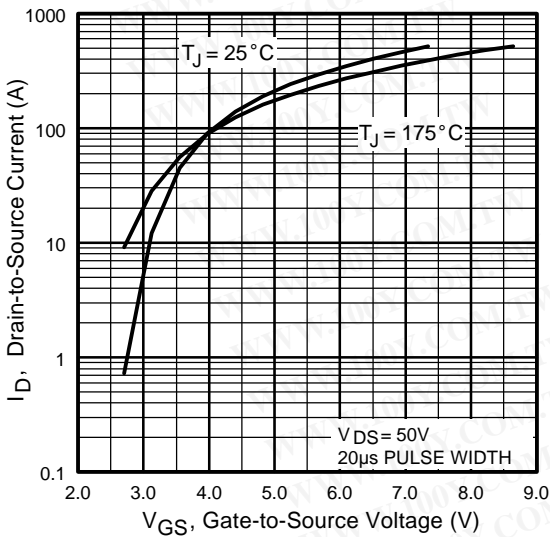


Fig 3. Typical Transfer Characteristics

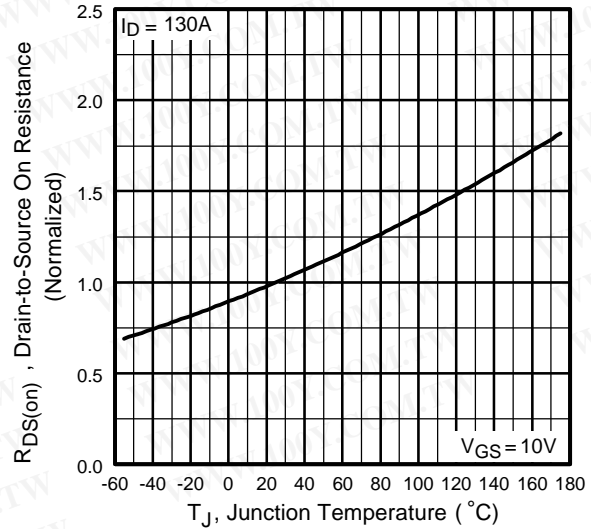


Fig 4. Normalized On-Resistance Vs. Temperature

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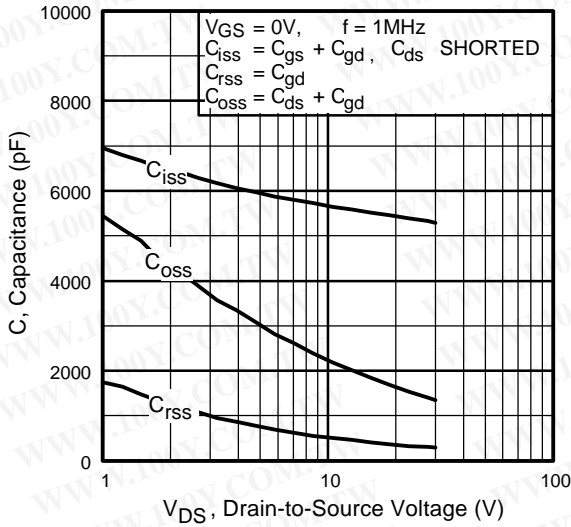


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

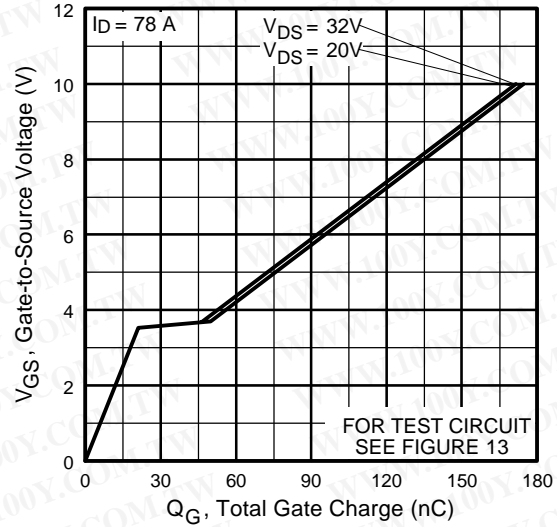


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

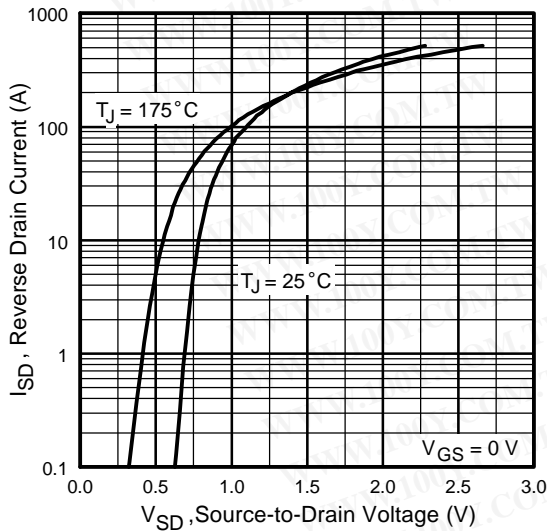


Fig 7. Typical Source-Drain Diode Forward Voltage

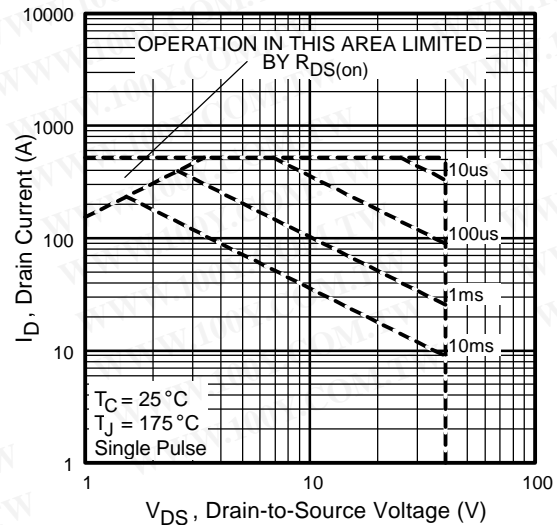


Fig 8. Maximum Safe Operating Area

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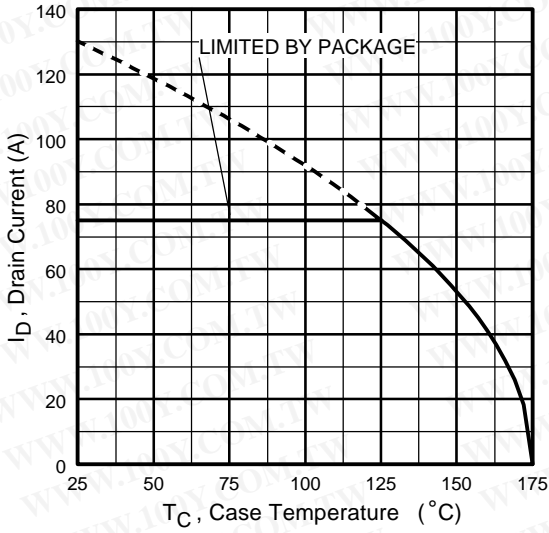


Fig 9. Maximum Drain Current Vs. Case Temperature

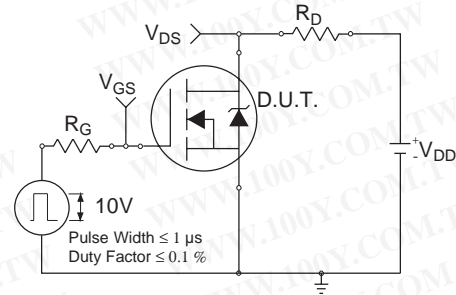


Fig 10a. Switching Time Test Circuit

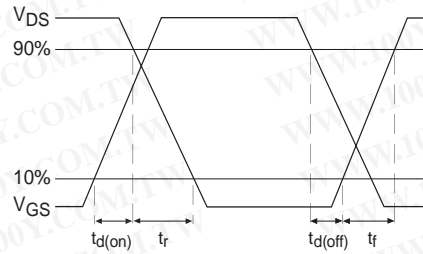


Fig 10b. Switching Time Waveforms

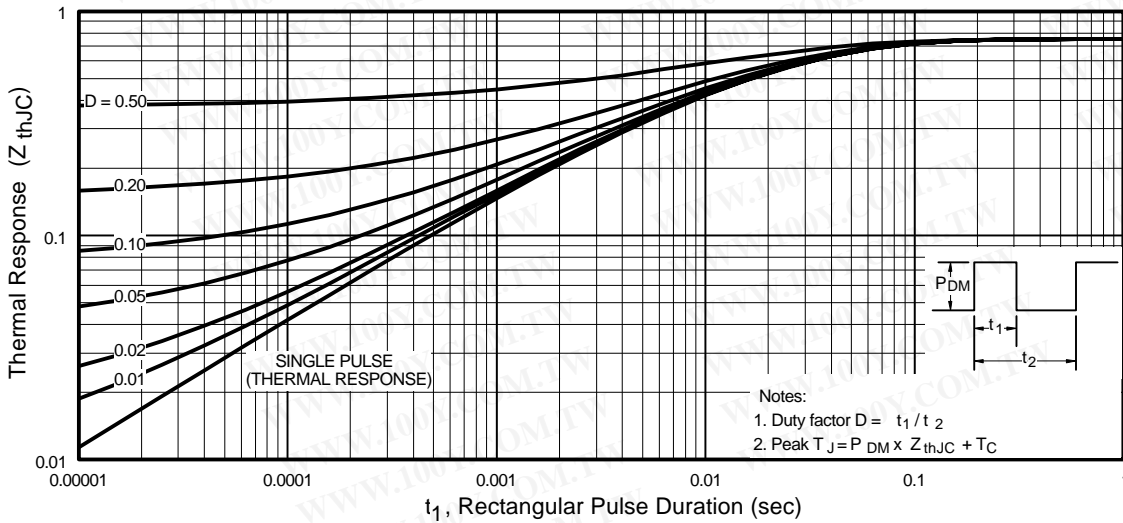


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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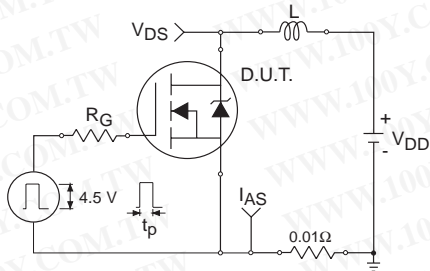


Fig 12a. Unclamped Inductive Test Circuit

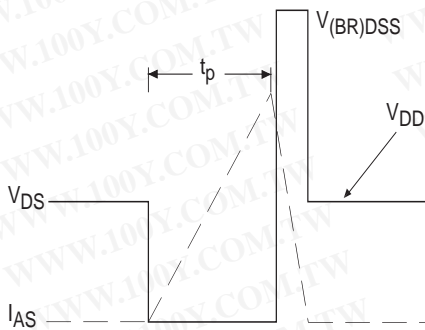


Fig 12b. Unclamped Inductive Waveforms

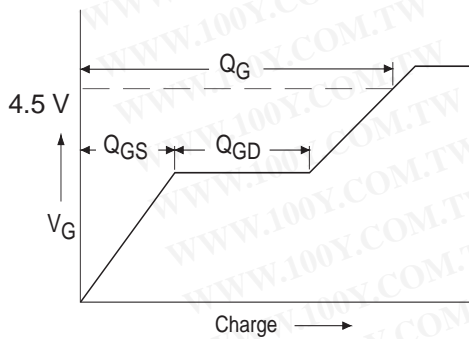


Fig 13a. Basic Gate Charge Waveform

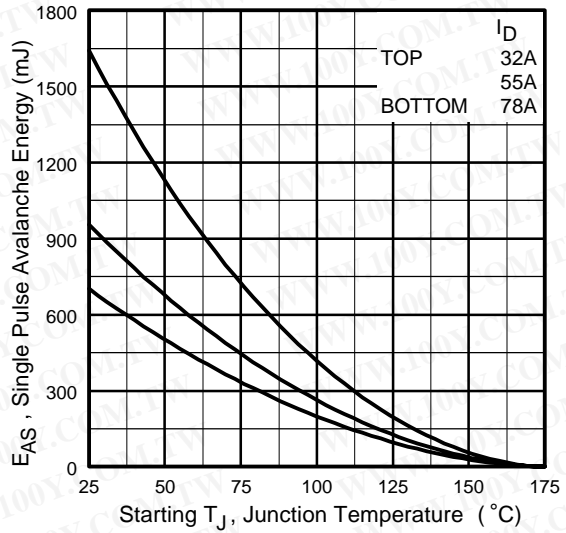


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

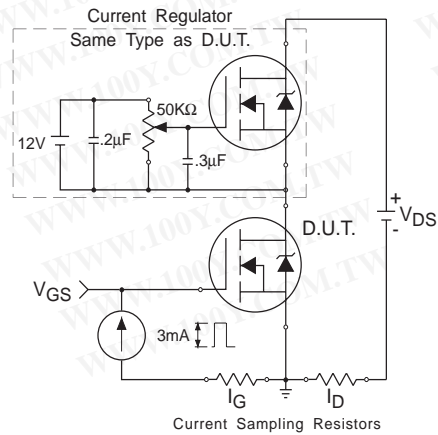
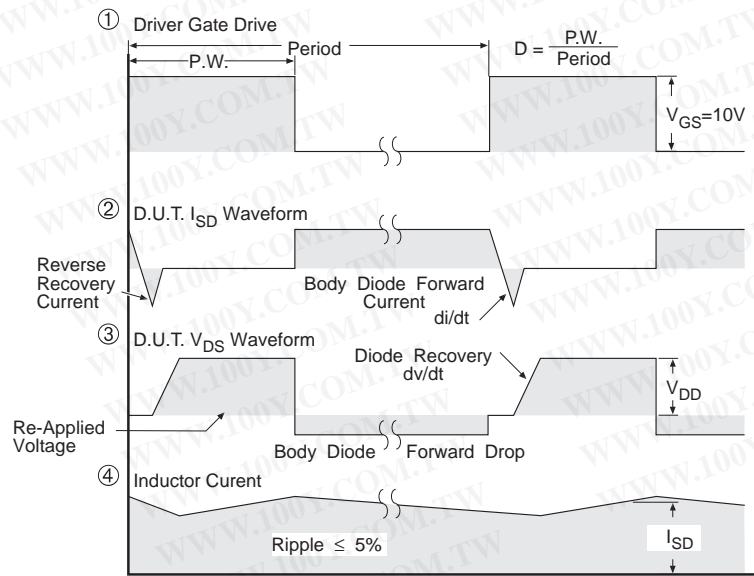
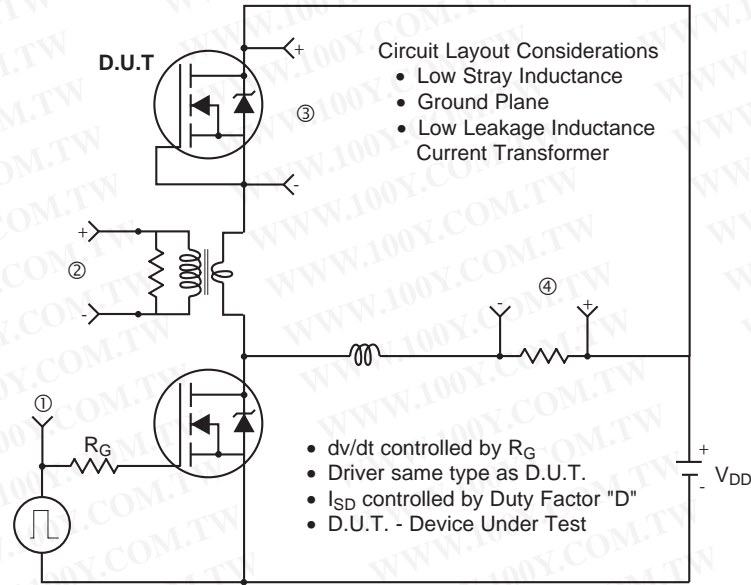


Fig 13b. Gate Charge Test Circuit

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Peak Diode Recovery dv/dt Test Circuit



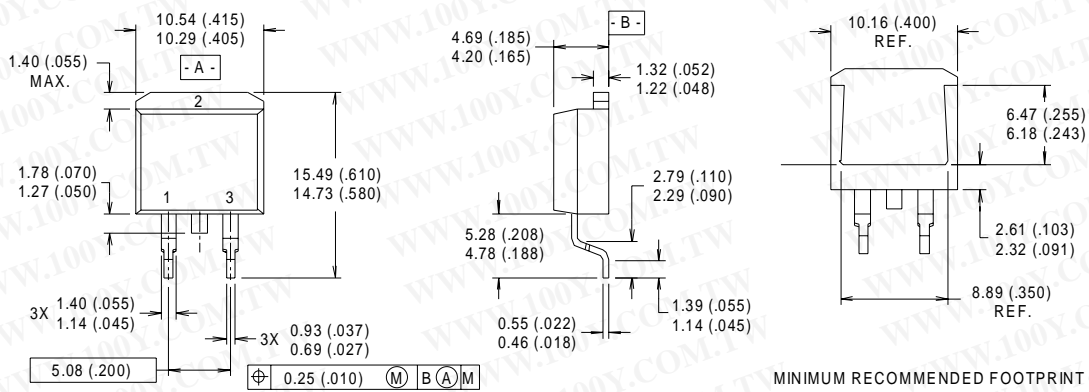
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-channel HEXFET® Power MOSFETs

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D²Pak Package Outline



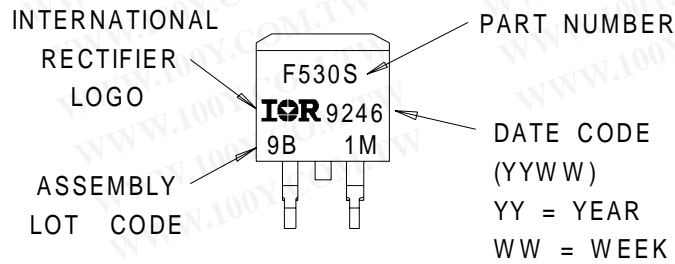
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANS Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

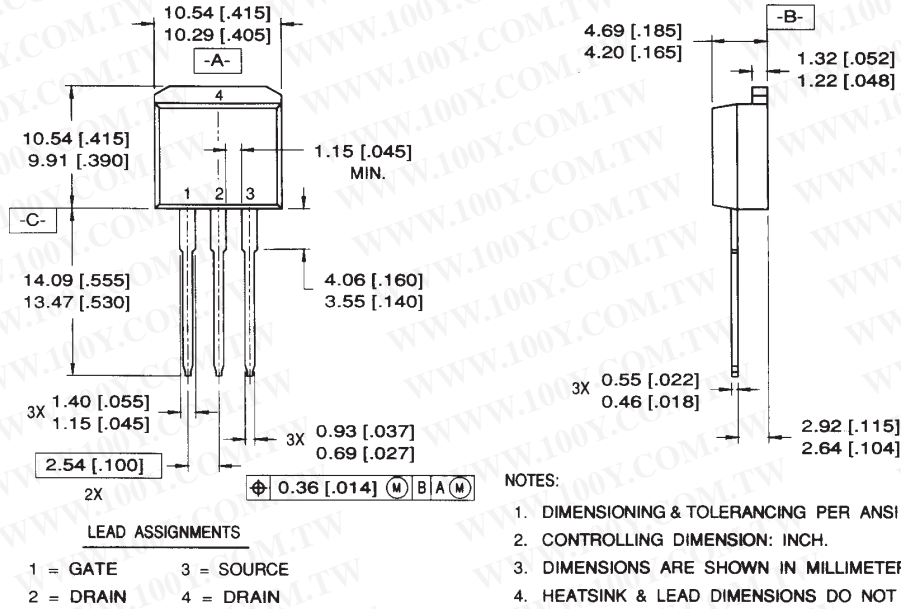
D²Pak Part Marking Information



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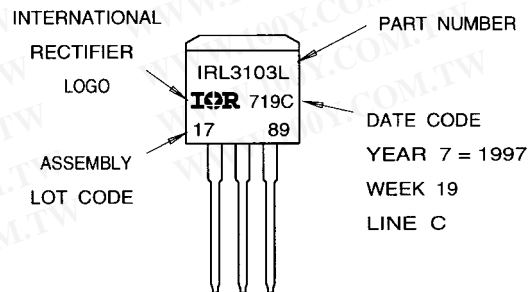
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TO-262 Package Outline



TO-262 Part Marking Information

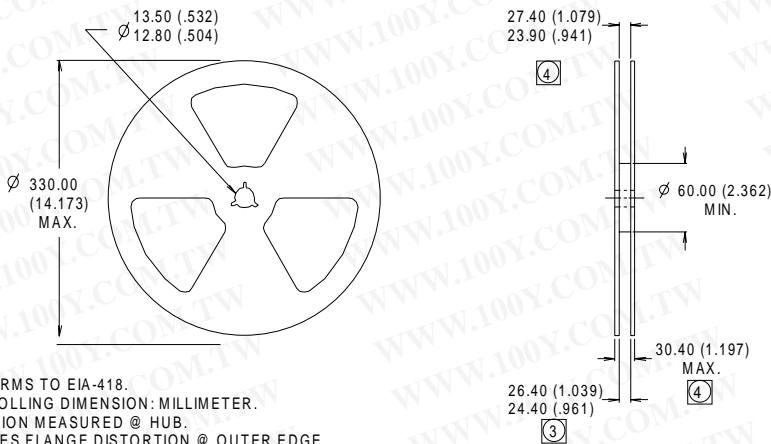
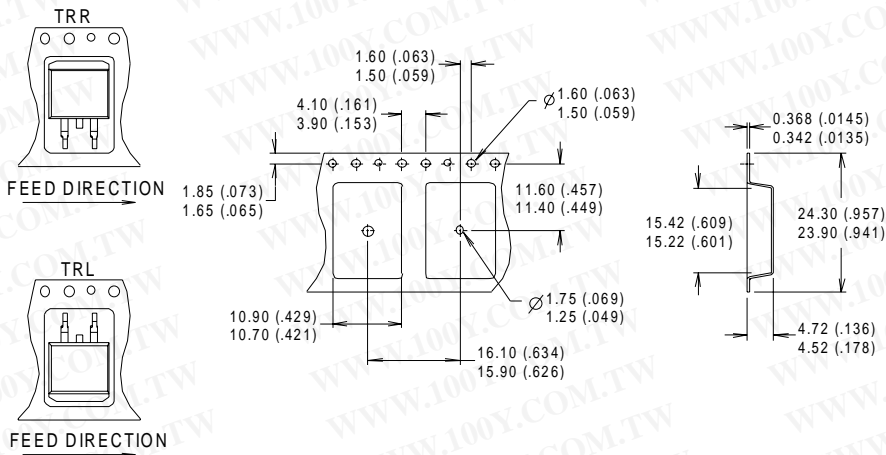
EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



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D²Pak Tape & Reel Information

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- NOTES :
1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION : MILLIMETER.
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

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Data and specifications subject to change without notice. 12/99