

- N-Channel Application-Specific MOSFET
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Minimizes Parallel MOSFETs for high current applications
- 100%  $R_G$  Tested

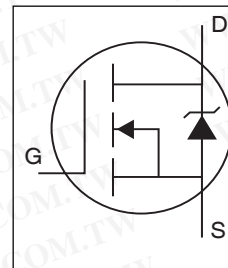
## HEXFET® MOSFET for DC-DC Converters

### Description

This new device employs advanced HEXFET Power MOSFET technology to achieve very low on-resistance. The reduced conduction losses makes it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRLR8503 has been optimized and is 100% tested for all parameters that are critical in synchronous buck converters including  $R_{DS(on)}$ , gate charge and  $C_{dv/dt}$ -induced turn-on immunity. The IRLR8503 offers an extremely low combination of  $Q_{sw}$  &  $R_{DS(on)}$  for reduced losses in control FET applications.

The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 2W is possible in a typical PCB mount application.



### DEVICE RATINGS (MAX. Values)

	IRLR8503
$V_{DS}$	30V
$R_{DS(on)}$	18 mΩ
$Q_G$	20 nC
$Q_{SW}$	8 nC
$Q_{OSS}$	29.5 nC

### Absolute Maximum Ratings

Parameter	Symbol	IRLR8503	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	±20	
Continuous Drain or Source Current	$I_D$	44	A
		32	
Pulsed Drain Current ①	$I_{DM}$	196	W
Power Dissipation ⑤	$P_D$	62	
		30	
Junction & Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C
Continuous Source Current (Body Diode)	$I_S$	15	A
Pulsed Source Current ①	$I_{SM}$	196	

### Thermal Resistance

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ③ ⑥	$R_{θJA}$	—	50	°C/W
Maximum Junction-to-Lead ⑥	$R_{θJL}$	—	2.0	

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## Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Drain-to-Source Breakdown Voltage*	$V_{(BR)DSS}$	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
Static Drain-Source On-Resistance*	$R_{DS(on)}$	—	11	16	m $\Omega$	$V_{GS} = 10V, I_D = 15A$ ②
		—	13	18		$V_{GS} = 4.5V, I_D = 15A$
Gate Threshold Voltage*	$V_{GS(th)}$	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-Source Leakage Current	$I_{DSS}$	—	—	1.0	$\mu A$	$V_{DS} = 30V, V_{GS} = 0$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0, T_J = 100^\circ C$
Gate-Source Leakage Current*	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20V$
Total Gate Charge, Control FET*	$Q_g$	—	15	20	nC	$V_{GS} = 5V, I_D = 15A, V_{DS} = 16V$
Total Gate Charge, Synch FET*	$Q_g$	—	13	17		$V_{GS} = 5V, V_{DS} < 100mV$
Pre-V <sub>th</sub> Gate-to-Source Charge	$Q_{gs1}$	—	3.7	—		$V_{DS} = 16V, I_D = 15A$
Post-V <sub>th</sub> Gate-to-Source Charge	$Q_{gs2}$	—	1.3	—		
Gate-to-Drain Charge	$Q_{gd}$	—	4.1	—		
Switch Charge* ( $Q_{gs2} + Q_{gd}$ )	$Q_{SW}$	—	5.4	8		
Output Charge*	$Q_{OSS}$	—	23	29.5		$V_{DS} = 16V, V_{GS} = 0$
Gate Resistance	$R_G$	0.4	—	1.1	$\Omega$	
Turn-On Delay Time	$t_{d(on)}$	—	10	—	ns	$V_{DD} = 16V, I_D = 15A$ $V_{GS} = 5.0V$ Clamped Inductive Load See Test Diagram Fig. 14
Drain Voltage Rise Time	$t_{rV}$	—	18	—		
Turn-Off Delay Time	$t_{d(off)}$	—	11	—		
Drain Voltage Fall Time	$t_{fV}$	—	3	—		
Input Capacitance	$C_{iss}$	—	1650	—	pF	$V_{DS} = 25V$
Output Capacitance	$C_{oss}$	—	650	—		$V_{GS} = 0$
Reverse Transfer Capacitance	$C_{rss}$	—	58	—		

## Source-Drain Rating & Characteristics

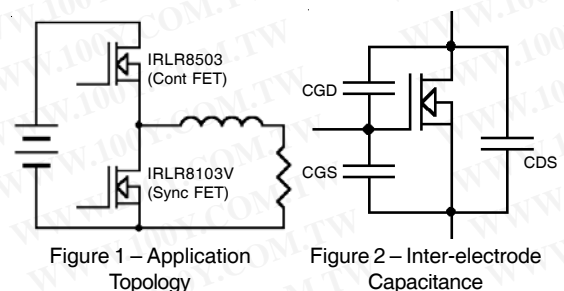
Parameter	Symbol	Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	$V_{SD}$	—	—	1.0	V	$I_S = 15A$ ②, $V_{GS} = 0V$
Reverse Recovery Charge ④	$Q_{rr}$	—	76	—	nC	$di/dt = 700A/\mu s$ $V_{DD} = 16V, V_{GS} = 0V, I_S = 15A$
Reverse Recovery Charge (with Parallel Schottky) ④	$Q_{rr(s)}$	—	67	—		$di/dt = 700A/\mu s$ (with 10BQ040) $V_{DD} = 16V, V_{GS} = 0V, I_S = 15A$

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ⑤ Calculated continuous current based on maximum allowable Junction temperature; switching and other losses will decrease RMS current capability; package limitation current = 20A.  
 ② Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .  
 ③ When mounted on 1 inch square copper board,  $t < 10$  sec.  
 ④ Typ = measured -  $Q_{oss}$   
 ⑥  $R_{\theta}$  is measured at  $T_J$  approximately at  $90^\circ C$

\*Devices are 100% tested to these parameters.

**Power MOSFET Optimization for DC-DC Converters**  
 While the IRLR8103V and IRLR8503 can and are being used in a variety of applications, they were designed and optimized for low voltage DC-DC conversion in a synchronous buck converter topology, specifically, microprocessor power applications. The IRLR8503 (Figure 1) was optimized for the control FET socket, while the IRLR8103V was optimized for the synchronous FET function.



Because of the inter-electrode capacitance (Figure 2) of the Power MOSFET, specifying the  $R_{DS(on)}$  of the device is not enough to ensure good performance. An optimization between  $R_{DS(on)}$  and charge must be performed to insure the best performing MOSFET for a given application. Both die size and device architecture must be varied to achieve the minimum possible in-circuit losses. This is independently true for both control FET and synchronous FET. Unfortunately, the capacitances of a FET are non-linear and voltage dependent. Therefore, it is inconvenient to specify and use them effectively in switching power supply power loss estimations. This was well understood years ago and resulted in changing the emphasis from capacitance to gate charge on Power MOSFET data sheets.

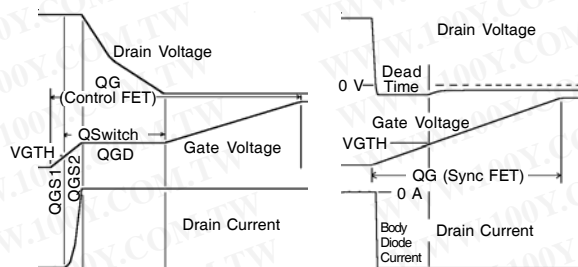
Table 1 – Traditional Charge Parameters

Device Capacitance	Corresponding Charge Parameter
$C_{GS}$	$Q_{GS}$
$C_{GS} + C_{GD}$	$Q_G$
$C_{GD}$	$Q_{GD}$

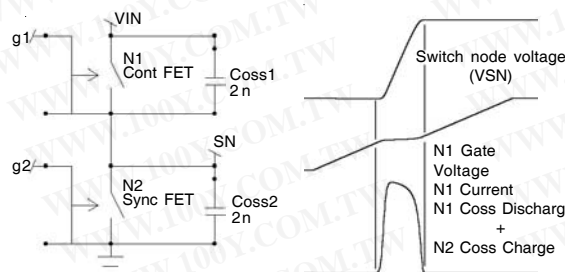
International Rectifier has recently taken the industry a step further by specifying new charge parameters that are even more specific to DC-DC converter design (Table 2). In order to understand these parameters, it is best to start with the in-circuit waveforms in Figure 3 & Figure 4.

Table 2 – New Charge Parameters

New Charge Parameter	Description	Waveform
$Q_{GS1}$	Pre-Threshold Gate Charge	Figure 3
$Q_{GS2}$	Post-Threshold Gate Charge	
$Q_{GCONT}$	Control FET Total $Q_G$	
$Q_{SWITCH}$	Charge during control FET switching Combines $Q_{GS2}$ and $Q_{GD}$	Figure 5 Figure 6
$Q_{OSS}$	Output charge Charge supplied to $C_{OSS}$ during the $Q_{GD}$ period of control FET switching	
$Q_{Gsync}$	Synchronous FET Total $Q_G$ ( $V_{DS} \leq 0$ )	



The waveforms are broken into segments corresponding to charge parameters. These, in turn, correspond to discrete time segments of the switching waveform.



Losses may be broken into four categories: conduction loss, gate drive loss, switching loss, and output loss. The following simplified power loss equation is true for both MOSFETs in a synchronous buck converter:

$$P_{LOSS} = P_{CONDUCTION} + P_{GATE\ DRIVE} + P_{SWITCH} + P_{OUTPUT}$$

For the synchronous FET, the  $P_{SWITCH}$  term becomes virtually zero and is ignored.



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Table 3 and Table 4 describes the event during the various charge segments and shows an approximation of losses during that period.

Table 3 – Control FET Losses

	Description	Segment Losses
Conduction Loss	Losses associated with MOSFET on time. $I_{RMS}$ is a function of load current and duty cycle.	$P_{COND} = I_{RMS}^2 \times R_{DS(on)}$
Gate Drive Loss	Losses associated with charging and discharging the gate of the MOSFET every cycle. Use the control FET $Q_G$ .	$P_{IN} = V_G \times Q_G \times f$
Switching Loss	Losses during the drain voltage and drain current transitions for every full cycle. Losses occur during the $Q_{GS2}$ and $Q_{GD}$ time period and can be simplified by using $Q_{switch}^*$	$P_{QGS2} \approx V_{IN} \times I_L \times \frac{Q_{GS2}}{I_G} \times f$ $P_{QGD} \approx V_{IN} \times I_L \times \frac{Q_{GD}}{I_G} \times f$ $P_{SWITCH} \approx V_{IN} \times I_L \times \frac{Q_{SW}}{I_G} \times f$
Output Loss	Losses associated with the $Q_{OSS}$ of the device every cycle when the control FET turns on. Losses are caused by both FETs, but are dissipated by the control FET.	$P_{OUTPUT} = \frac{Q_{OSS}}{2} \times V_{IN} \times F$

Table 4 – Synchronous FET Losses

	Description	Segment Losses
Conduction Loss	Losses associated with MOSFET on time. $I_{RMS}$ is a function of load current and duty cycle.	$P_{COND} = I_{RMS}^2 \times R_{DS(on)}$
Gate Drive Loss	Losses associated with charging and discharging the gate of the MOSFET every cycle. Use the Sync FET $Q_G$ .	$P_{IN} = V_G \times Q_G \times f$
Switching Loss	Generally small enough to ignore except at light loads when the current reverses in the output inductor. Under these conditions various light load power saving techniques are employed by the control IC to maintain switching losses to a negligible level.	$P_{SWITCH} \approx 0$
Output Loss	Losses associated with the $Q_{OSS}$ of the device every cycle when the control FET turns on. They are caused by the synchronous FET, but are dissipated in the control FET.	$P_{OUTPUT} = \frac{Q_{OSS}}{2} \times V_{IN} \times f$

## Typical PC Application

The IRLR8103V and the IRLR8503 are suitable for Synchronous Buck DC-DC Converters, and are optimized for use in next generation CPU applications. The IRLR8103V is primarily optimized for use as the low side synchronous FET (Q2) with low  $R_{DS(on)}$  and high  $Cdv/dt$  immunity. The IRLR8503 is primarily optimized for use as the high side control FET (Q1) with low combined  $Q_{sw}$  and  $R_{DS(on)}$ , but can also be used as a synchronous FET. The IRLR8503 is also tested for  $Cdv/dt$  immunity, critical for the low side socket. The typical configuration in which these devices may be used is shown in Figure 7.

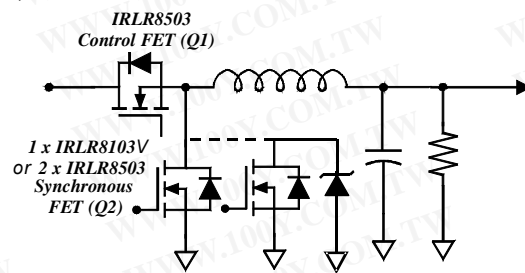


Figure 7. 2 & 3-FET solution for Synchronous Buck Topology.

## Typical Characteristics IRLR8503

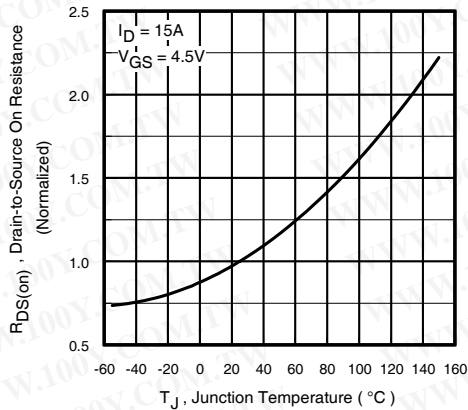


Figure 8. Normalized On-Resistance vs. Temperature

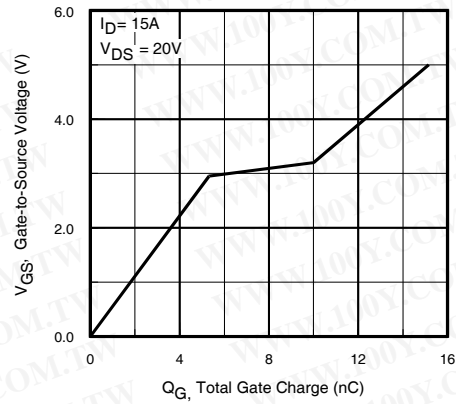


Figure 9. Gate-to-Source Voltage vs. Typical Gate Charge

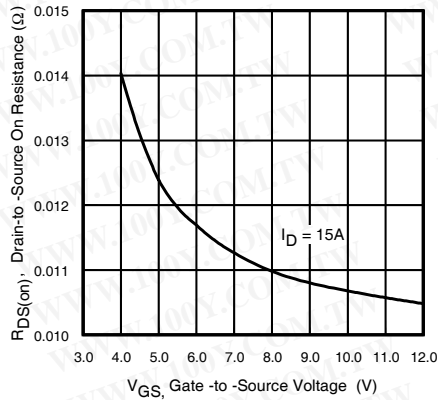


Figure 10. Typical  $R_{DS(on)}$  vs. Gate-to-Source Voltage

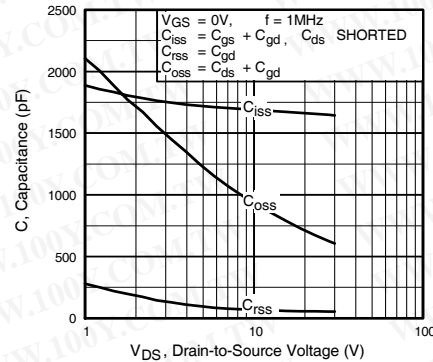


Figure 11. Typical Capacitance vs. Drain-to-Source Voltage

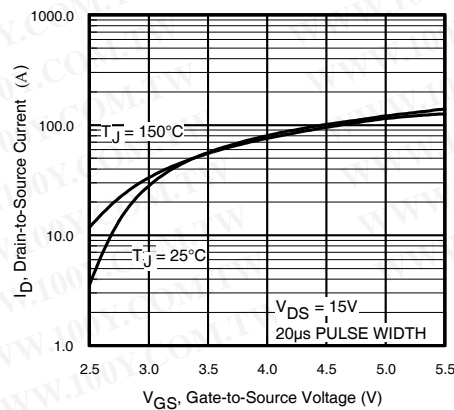


Figure 12. Typical Transfer Characteristics

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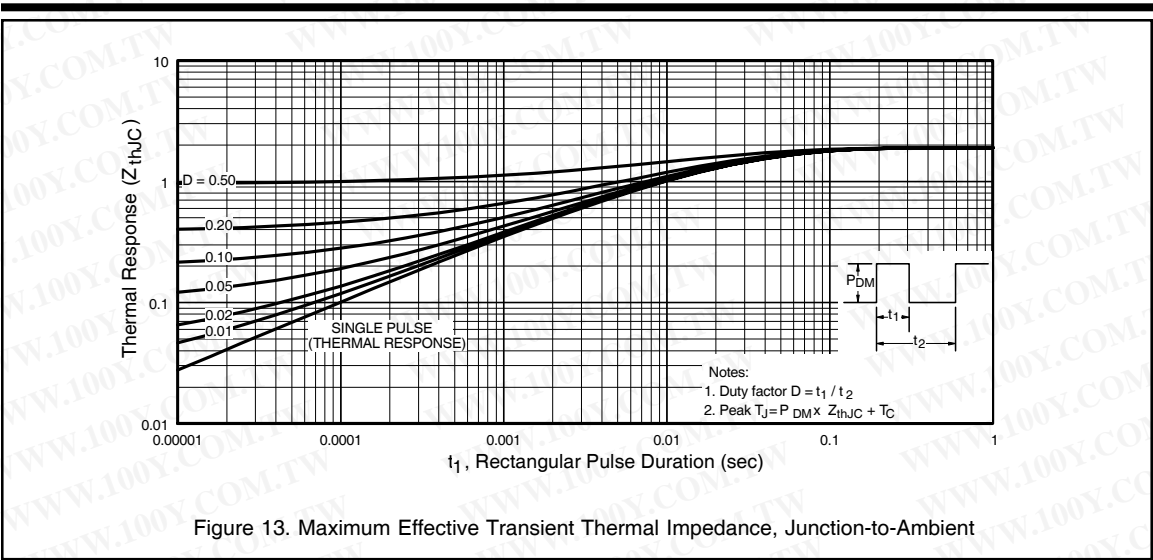


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

## Inductive Load Circuit

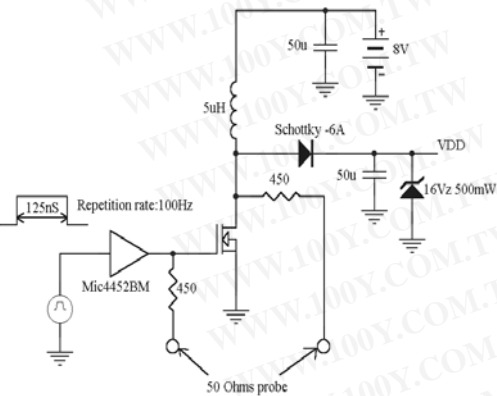


Figure 14. Clamped Inductive Load test diagram

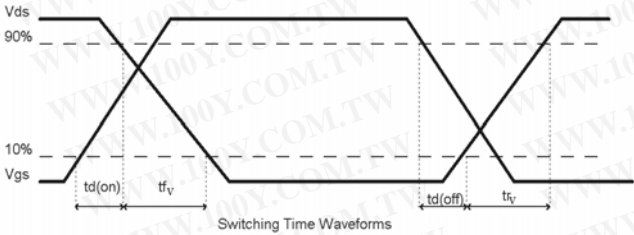


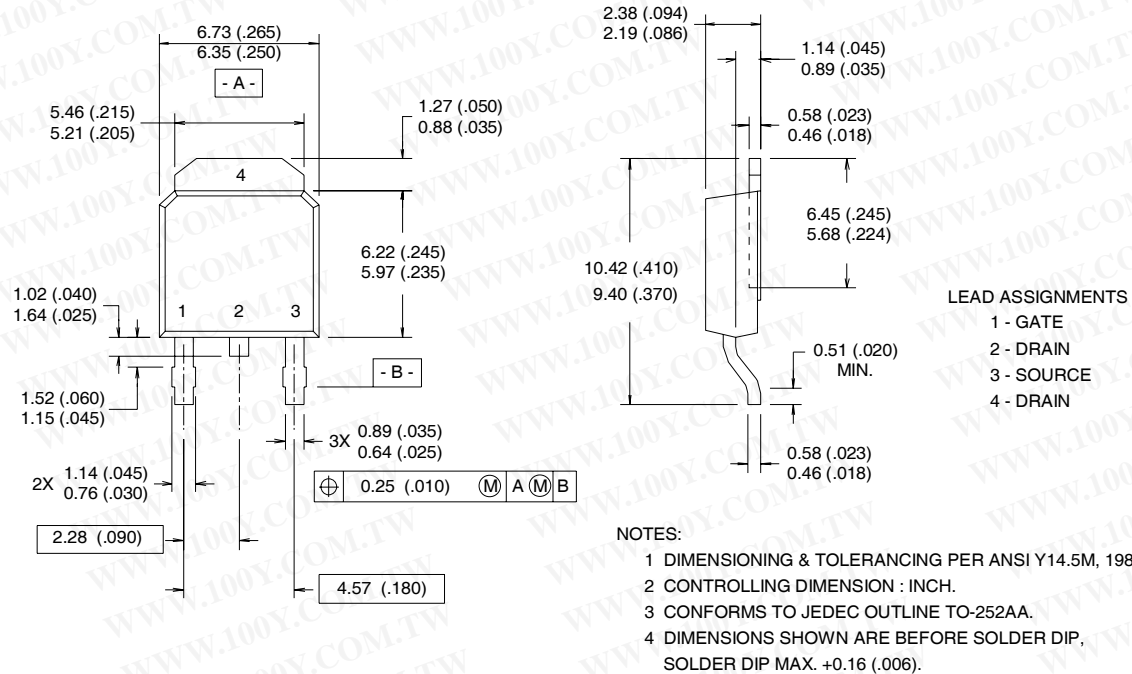
Figure 15. Switching waveform

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IRLR8503

## D-Pak (TO-252AA) Package Outline

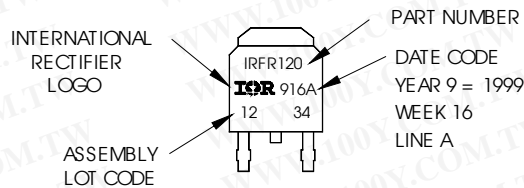
Dimensions are shown in millimeters (inches)



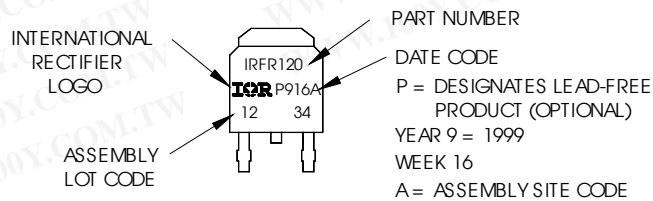
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
 WITH ASSEMBLY  
 LOT CODE 1234  
 ASSEMBLED ON WW 16, 1999  
 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line  
 position indicates "Lead-Free"



OR



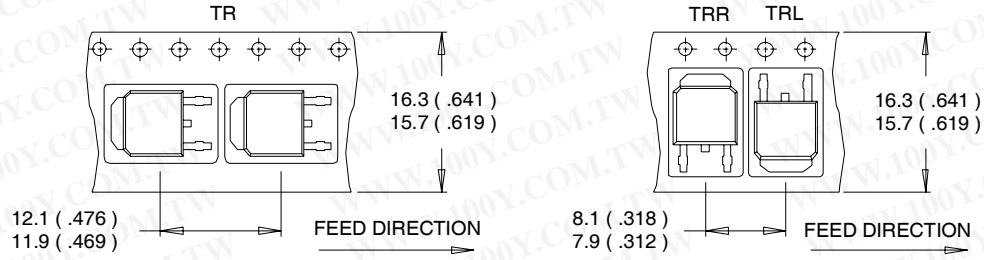


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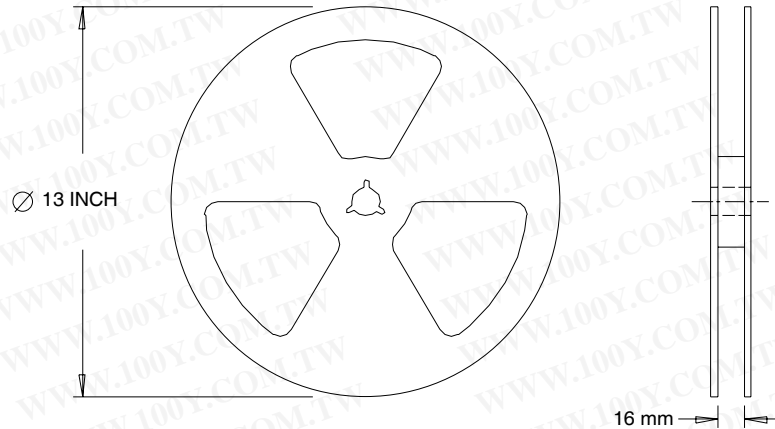
## Tape & Reel Information

### TO-252AA



#### NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



#### NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the commercial market.  
 Qualification Standards can be found on IR's Web site.

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