

## VRM 8.5 COMPATIBLE 5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC WITH TRIPLE LDO CONTROLLER

### FEATURES

- Meets Latest VRM 8.5 Specification
- Provides Single Chip Solution for Vcore, 1.2V AGTL+, 1.8V and V<sub>DDQ</sub>
- On-Board 5-Bit DAC and Decoder programs the output voltage from 1.050V to 1.825V
- Loss-less Short Circuit Protection
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle when operating with a changing load
- Minimum Part Count, No External Compensation
- Soft-Start
- High current totem pole driver for directly driving an external Power MOSFET
- Power Good Function

### APPLICATIONS

- Pentium III with VRM 8.5 Specification
- DC to DC Converters

### DESCRIPTION

The IRU3013 controller IC is specifically designed for Intel Pentium III™ microprocessor applications as described in the VRM 8.5 specification. **The IC provides a single chip solution for the Vcore, 1.2V AGTL+, 1.8V and a third uncommitted LDO controller that can be used either as 1.2V power good detector or to provide 1.5V AGP bus in applications that this voltage is required.** The IRU3013 features a patented topology that, in combination with a few external components, (\*Note: See application current in figure 3) will provide in excess of 30A of output current for an on-board Vcore synchronous converter while automatically providing the output voltage specified in VRM 8.5 specification. The IRU3013 also features, **loss-less current sensing by using the R<sub>DS(ON)</sub> of the high side Power MOSFET as the sensing resistor**, a Power Good window comparator that switches its open collector output low when the output is outside of a ±10% window. Other features of the device are: Under-voltage lockout for both 5V and 12V supplies, an external programmable soft-start function, and the ability to program the oscillator frequency by connecting an external capacitor.

### TYPICAL APPLICATION

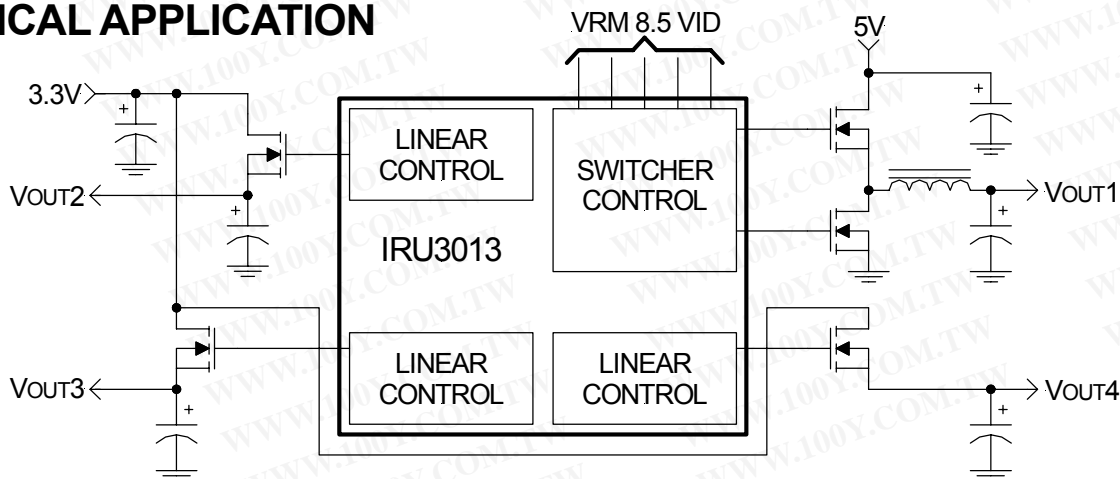


Figure 1 - Typical application of IRU3013.

Note: Pentium III is trade mark of Intel Corp.

### PACKAGE ORDER INFORMATION

| T <sub>A</sub> (°C) | DEVICE    | PACKAGE                |
|---------------------|-----------|------------------------|
| 0 To 70             | IRU3013CW | 24-Pin Plastic SOIC WB |
| 0 To 70             | IRU3013CQ | 24-Pin Plastic QSOP    |

# IRU3013

## ABSOLUTE MAXIMUM RATINGS

|  |                |
|--|----------------|
| V5 Supply Voltage .....                    | 10V            |
| V12 Supply Voltage .....                   | 20V            |
| All Other Pins .....                       | 7V             |
| Storage Temperature Range .....            | -65°C To 150°C |
| Operating Junction Temperature Range ..... | 0°C To 125°C   |

## PACKAGE INFORMATION

| 24-PIN WIDE BODY PLASTIC SOIC (W)  | 24-PIN PLASTIC QSOP (Q)  |
|--|--|
| <p style="text-align: center;">TOP VIEW</p> <p style="text-align: center;"><math>\theta_{JA} = 80^{\circ}\text{C/W}</math></p> | <p style="text-align: center;">TOP VIEW</p> <p style="text-align: center;"><math>\theta_{JA} = 88^{\circ}\text{C/W}</math></p> |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T<sub>A</sub>=0 to 70°C. Typical values refer to T<sub>A</sub>=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

| PARAMETER                                 | SYM | TEST CONDITION                           | MIN    | TYP    | MAX    | UNITS |
|---|-----|--|--------|--------|--------|-------|
| <b>VID Section</b>                        |     |  |        |        |        |       |
| DAC Output Voltage (Note 1)               |     |  | 0.98Vs | Vs     | 1.02Vs | V     |
| DAC Output Line Regulation                |     | 4.5<V <sub>CC</sub> <5.5<br>10.5<V12<13V |        | 0.2    |        | %     |
| DAC Output Temp Variation                 |     |  |        | 0.5    |        | %     |
| VID Input LO                              |     |  |        |        | 0.4    | V     |
| VID Input HI                              |     |  | 2      |        |        | V     |
| VID Input Internal Pull-up Resistor to 5V |     |  |        | 27     |        | KΩ    |
| <b>Power Good Section</b>                 |     |  |        |        |        |       |
| Under-Voltage Lower Trip Point            |     | V <sub>OUT</sub> Ramping Down            |        | 0.90Vs |        | V     |
| Under-Voltage Upper Trip Point            |     | V <sub>OUT</sub> Ramping Up              |        | 0.92Vs |        | V     |
| UV Hysteresis                             |     |  |        | 0.02Vs |        | V     |
| Over-Voltage Upper Trip Point             |     | V <sub>OUT</sub> Ramping Up              |        | 1.10Vs |        | V     |
| Over-Voltage Lower Trip Point             |     | V <sub>OUT</sub> Ramping Down            |        | 1.08Vs |        | V     |
| OV Hysteresis                             |     |  |        | 0.02Vs |        | V     |
| Power Good Output LO                      |     | R <sub>L</sub> = 3mA                     |        | 0.3    |        | V     |
| Power Good Output HI                      |     | R <sub>L</sub> = 5K Pull-Up to 5V        |        | 4.95   |        | V     |
| <b>Soft-Start Section</b>                 |     |  |        |        |        |       |
| Soft-Start Current                        |     | CS+ = 0V, CS- = 5V                       |        | 10     |        | μA    |

| PARAMETER   | SYM | TEST CONDITION                       | MIN | TYP            | MAX | UNITS |
|---|-----|--------------------------------------|-----|----------------|-----|-------|
| <b>UVLO Section</b>   |     |                                      |     |                |     |       |
| UVLO Threshold - 12V  |     | Supply Ramping Up                    |     | 9              |     | V     |
| UVLO Hysteresis - 12V   |     |                                      |     | 0.5            |     | V     |
| UVLO Threshold - 5V   |     | Supply Ramping Up                    |     | 4              |     | V     |
| UVLO Hysteresis - 5V  |     |                                      |     | 0.3            |     | V     |
| <b>Error Comparator Section</b>   |     |                                      |     |                |     |       |
| Input Offset Voltage  |     |                                      | -2  |                | +2  | mV    |
| Delay to Output   |     | V <sub>DIFF</sub> = 10mV             |     |                | 100 | ns    |
| <b>Current Limit Section</b>  |     |                                      |     |                |     |       |
| CS Threshold Set Current  |     |                                      | 120 | 150            | 200 | μA    |
| CS Comp Offset Voltage  |     |                                      | -5  |                | +5  | mV    |
| Hiccup Duty Cycle   |     | C <sub>SS</sub> = 0.1μF              |     |                | 2   | %     |
| <b>Supply Current Section</b>   |     |                                      |     |                |     |       |
| Operating Supply Current  |     | C <sub>L</sub> = 3000pF<br>V5<br>V12 |     | 20<br>14       |     | mA    |
| <b>Output Drivers Section</b>   |     |                                      |     |                |     |       |
| Rise Time   |     | C <sub>L</sub> = 3000pF              |     | 70             | 100 | ns    |
| Fall Time   |     | C <sub>L</sub> = 3000pF              |     | 70             | 130 | ns    |
| Dead Band Time  |     | C <sub>L</sub> = 3000pF              |     | 200            |     | ns    |
| <b>Oscillator Section</b>   |     |                                      |     |                |     |       |
| Osc Frequency   |     | C <sub>t</sub> = 150pF               |     | 220            |     | KHz   |
| Osc Valley  |     |                                      |     |                | 0.2 | V     |
| Osc Peak  |     |                                      |     | V5             |     | V     |
| <b>LDO Controller Section</b>   |     |                                      |     |                |     |       |
| V <sub>FB1</sub> and V <sub>FB2</sub> (Pins 3 and 4)<br>V <sub>FB4</sub> (Pin 15) |     |                                      |     | 1.200<br>0.800 |     | V     |
| Input Bias Current  |     |                                      |     |                | 2   | μA    |
| Lin 1, 2, 3 Drive Current   |     |                                      |     | 30             |     | mA    |
| <b>OVP Section</b>  |     |                                      |     |                |     |       |
| OVP Threshold   |     |                                      |     | 1.17Vs         |     | V     |
| OVP Source Current  |     |                                      |     | 5              |     | mA    |

**Note:** Vs refers to the set point voltage given in table 1.

| D25 | D3 | D2 | D1 | D0 | Vs    |
|-----|----|----|----|----|-------|
| 0   | 1  | 1  | 1  | 1  | 1.300 |
| 0   | 1  | 1  | 1  | 0  | 1.350 |
| 0   | 1  | 1  | 0  | 1  | 1.400 |
| 0   | 1  | 1  | 0  | 0  | 1.450 |
| 0   | 1  | 0  | 1  | 1  | 1.500 |
| 0   | 1  | 0  | 1  | 0  | 1.550 |
| 0   | 1  | 0  | 0  | 1  | 1.600 |
| 0   | 1  | 0  | 0  | 0  | 1.650 |
| 0   | 0  | 1  | 1  | 1  | 1.700 |
| 0   | 0  | 1  | 1  | 0  | 1.750 |
| 0   | 0  | 1  | 0  | 1  | 1.800 |
| 0   | 0  | 1  | 0  | 0  | 1.050 |
| 0   | 0  | 0  | 1  | 1  | 1.100 |
| 0   | 0  | 0  | 1  | 0  | 1.150 |
| 0   | 0  | 0  | 0  | 1  | 2.200 |
| 0   | 0  | 0  | 0  | 0  | 2.250 |

| D25 | D3 | D2 | D1 | D0 | Vs    |
|-----|----|----|----|----|-------|
| 1   | 1  | 1  | 1  | 1  | 1.325 |
| 1   | 1  | 1  | 1  | 0  | 1.375 |
| 1   | 1  | 1  | 0  | 1  | 1.425 |
| 1   | 1  | 1  | 0  | 0  | 1.475 |
| 1   | 1  | 0  | 1  | 1  | 1.525 |
| 1   | 1  | 0  | 1  | 0  | 1.575 |
| 1   | 1  | 0  | 0  | 1  | 1.625 |
| 1   | 1  | 0  | 0  | 0  | 1.675 |
| 1   | 0  | 1  | 1  | 1  | 1.725 |
| 1   | 0  | 1  | 1  | 0  | 1.775 |
| 1   | 0  | 1  | 0  | 1  | 1.825 |
| 1   | 0  | 1  | 0  | 0  | 1.075 |
| 1   | 0  | 0  | 1  | 1  | 1.125 |
| 1   | 0  | 0  | 1  | 0  | 1.175 |
| 1   | 0  | 0  | 0  | 1  | 1.225 |
| 1   | 0  | 0  | 0  | 0  | 1.275 |

Table 1 - Set point voltage vs. VID codes.

## PIN DESCRIPTIONS

| PIN# | PIN SYMBOL       | PIN DESCRIPTION   |
|------|------------------|---|
| 1    | Ct               | This pin programs the oscillator frequency in the range of 50 KHz to 500KHz by means of an external capacitor connected from this pin to the ground.  |
| 2    | Lin1             | Controls the gate of an external MOSFET for the AGTL+ linear regulator or 1.8V supply.  |
| 3    | V <sub>FB1</sub> | This pin provides the feedback for the linear regulator that its output drive is Lin1 pin.  |
| 4    | V <sub>FB2</sub> | This pin provides the feedback for the linear regulator that its output drive is Lin2 pin.  |
| 5    | V5               | 5V supply voltage.  |
| 6    | OVP              | This pin provides an over voltage flag when the feedback pin V <sub>FB3</sub> voltage exceeds 17%(Typical) of the set point for the Vcore output.   |
| 7    | PGd              | This pin is an open collector output that switches LO when the output of the converter is not within $\pm 10\%$ (typ) of the nominal output voltage. When PGd pin switches LO the output saturation voltage is less than 0.4V at 3mA.   |
| 8    | CS-              | This pin is connected to the Source of the power MOSFET for the Core supply and it is the negative input for the internal current sensing circuitry.  |
| 9    | CS+              | This pin is connected to the Drain of the power MOSFET of the Core supply. It provides the positive sensing input for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R <sub>DS</sub> of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.   |
| 10   | HDrv             | Output driver for the high side power MOSFET.   |
| 11   | PGnd             | This is the power ground pin and must be connected directly to the gnd plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1 $\mu$ F) must be connected from V12 pin to this pin for noise free operation.   |
| 12   | Gnd              | This pin must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1 $\mu$ F) must be connected from V5 and V12 pins to this pin for noise free operation.   |
| 13   | LDrv             | Output driver for the power MOSFET, which is used as a synchronous switched rectifier.  |
| 14   | V12              | This pin is connected to the 12V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (0.1 to 1 $\mu$ F) must be connected directly from this pin to Gnd pin in order to supply large instantaneous current pulses to the power MOSFET during the transitions.   |
| 15   | V <sub>FB4</sub> | This pin provides the feedback for the linear regulator that its output drive is Lin4 pin.  |
| 16   | Lin4             | This pin controls the gate of an external MOSFET for either the AGP Bus linear regulator or can be used as Power good detector for 1.2V AGTL+ bus.  |
| 17   | SS               | This pin provides the soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to the ground which ramps up the outputs of the switching regulator, preventing the outputs from overshooting as well as limiting the inrush current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting. |
| 18   | V <sub>FB3</sub> | This pin is connected directly to the output of the Core supply to provide feedback to the Error comparator.  |
| 19   | D25              | This pin programs the output voltage in 25mV steps based on the VID table. 40K internal pull-up to Vcc.   |
| 20   | D3               | MSB input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply. 40K internal pull-up to Vcc.   |
| 21   | D2               | Input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply. 40K internal pull-up to Vcc.   |
| 22   | D1               | Input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K $\Omega$ resistor to either 3.3V or 5V supply. 40K internal pull-up to Vcc.  |
| 23   | D0               | LSB input to the DAC that programs the output voltage. This pin can be pulled-up externally by a 10K resistor to either 3.3V or 5V supply. 40K internal pull-up to Vcc.   |
| 24   | Lin2             | Controls the gate of an external MOSFET for the AGTL+ linear regulator or 1.8V supply.  |

**BLOCK DIAGRAM**

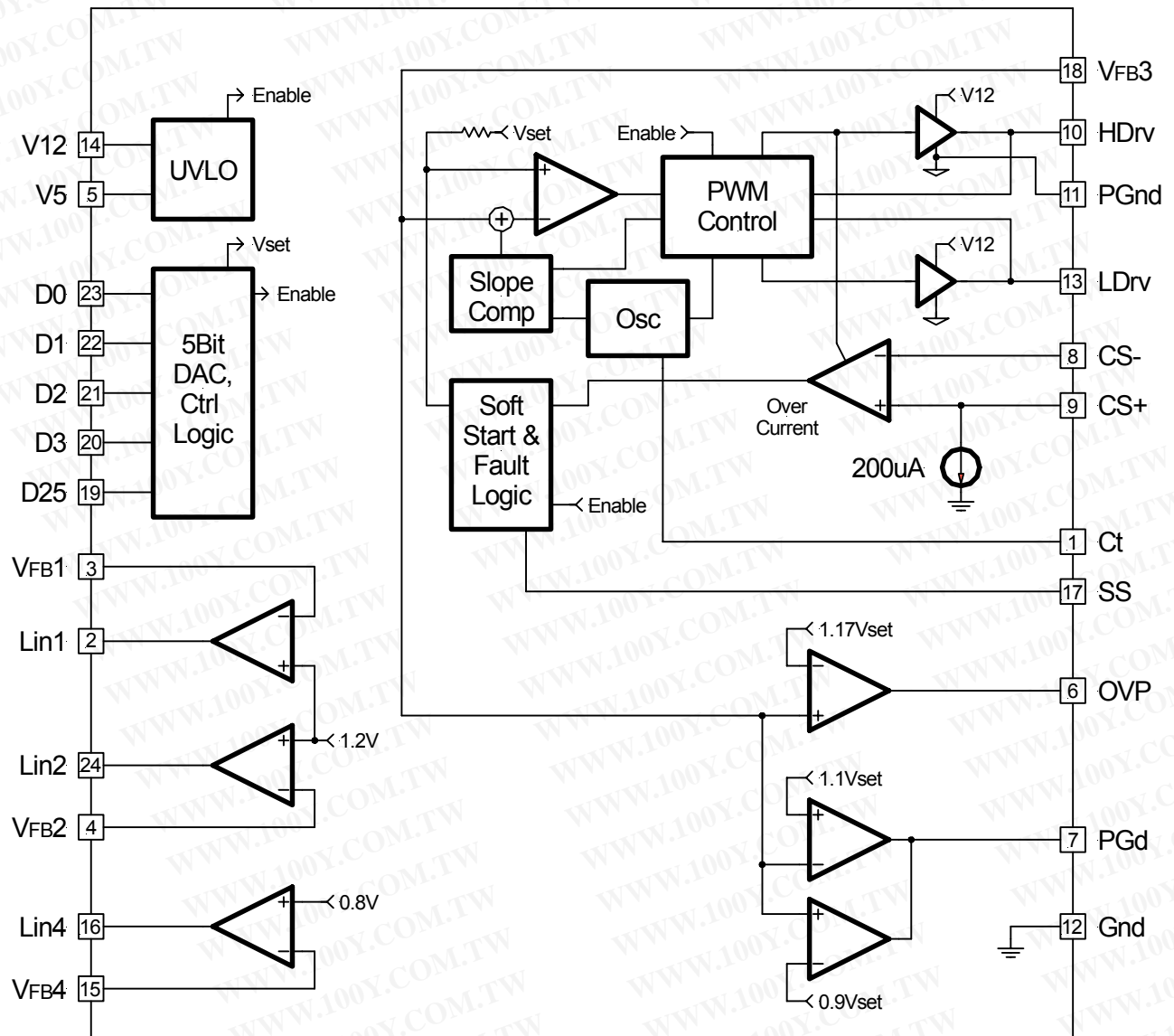


Figure 2 - Simplified block diagram of the IRU3013.

# IRU3013

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 勝特力电子(深圳) 86-755-83298787  
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International  
**IGOR** Rectifier

## TYPICAL APPLICATION

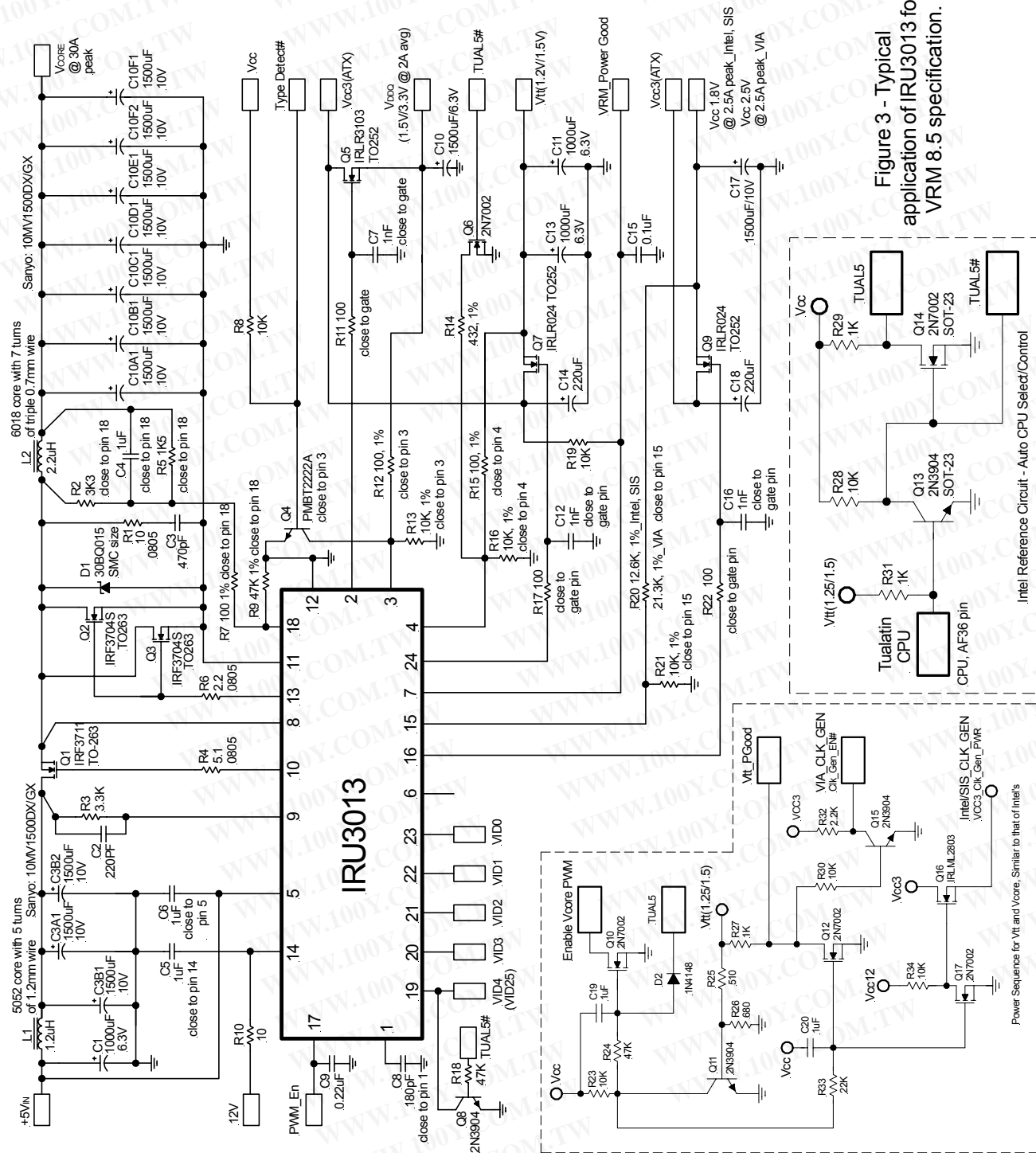


Figure 3 - Typical application of IRU3013 for VRM 8.5 specification.

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