Data Sheet No. PD94146

IRU3027

5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC WITH TRIPLE LDO CONTROLLER

FEATURES

- Designed to meet VRM 9.0 specification for next generation microprocessors
- On-Board 5-Bit DAC programs the output voltage from 1.075V to 1.850V in 25mV steps
- Linear Regulator Controller On-Board for 1.8V
- Provides single chip solution for Vcore, GTL+, AGP bus, and 1.8V
- Automatic Voltage Selection for AGP Slot V_{DDQ} Supply
- Linear Regulator Controller On-Board for 1.5V GTL+ Supply
- Loss-less Short Circuit Protection for all Outputs
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Minimum Part Count
- Soft-Start
- High current totem pole driver for direct driving of the external power MOSFET
- Power Good function monitors all outputs
- Over-Voltage Protection Circuitry protects the switcher output and generates a fault output

APPLICATIONS

- Total power solution for next generation Intel processor application
- AMD K7 Low Cost Solution

DESCRIPTION

The IRU3027 controller IC is specifically designed to meet VRM 9.0 specification for next generation microprocessor applications requiring multiple on-board regulators. The IRU3027 provides a single chip controller IC for the Vcore, three LDO controllers, one with an automatic select pin that connects to the Type Detect pin of the AGP slot for the AGP V_{DDQ} supply, one for GTL+ and the other for the 1.8V chip set regulator as required for the next generation PC applications. The IRU3027 is designed to use either bipolar transistors for $V_{OUT}3$(1.5V) and $V_{OUT}4$(1.8V). No external resistor divider is necessary for any of the regulators. The switching regulator features a patented topology that in combination with a few external components as shown in the typical application circuit, will provide well in excess of 20A of output current for an on-board DC-DC converter while automatically providing the right output voltage via the 5-bit internal DAC. The IRU3027 also features loss-less current sensing for both switchers by using the $R_{DS(ON)}$ of the high side power MOSFET as the sensing resistor, an output under-voltage shutdown that detects short circuit condition for the linear outputs and latches the system off, and a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre-programmed window.

TYPICAL APPLICATION

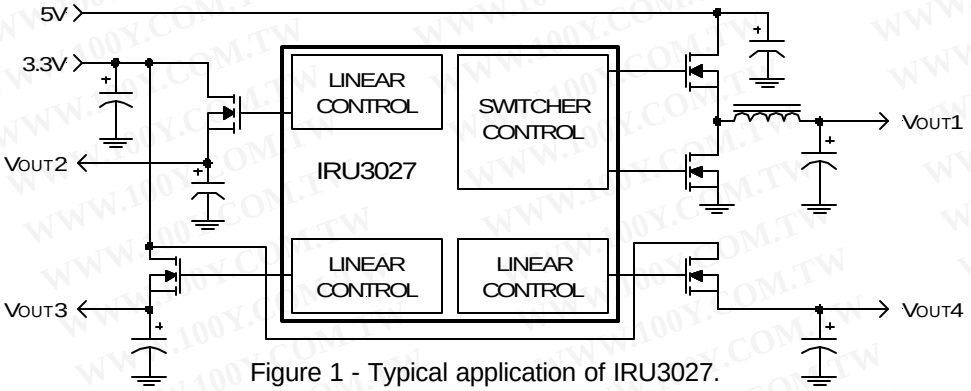


Figure 1 - Typical application of IRU3027.

PACKAGE ORDER INFORMATION

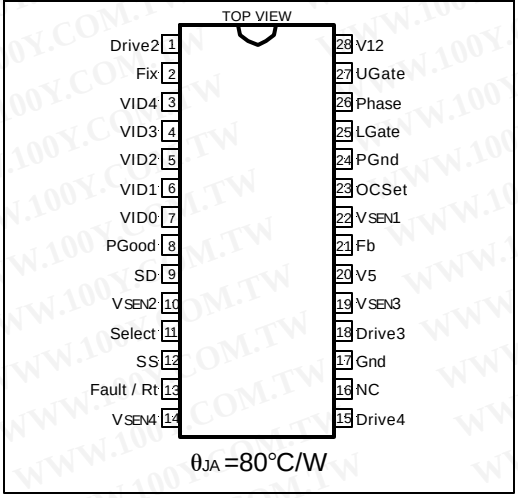
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3027CW	28-Pin Plastic SOIC WB

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 7V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65 To 150°C
Operating Junction Temperature Range ..... 0 To 125°C

PACKAGE INFORMATION

28 PIN WIDE BODY PLASTIC SOIC (W)



θ_{JA} =80°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply Ramping Up		10		V
UVLO Hysteresis-12V				0.6		V
UVLO Threshold-5V		Supply Ramping Up		4.4		V
UVLO Hysteresis-5V				0.3		V
Supply Current						
Operating Supply Current		V12 V5		6 30		mA
Switching Controllers; Vcore (V_{SEN}1) and AGP (V_{SEN}2)						
VID Section (Vcore only)						
DAC Output Voltage (Note 1)			0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation				0.1		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.8	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5				27		KΩ
V_{SEN}2 Voltage		Select <0.8V Select >2V		1.5 3.3		V

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Comparator Section						
Input Bias Current					2	µA
Input Offset Voltage			-2		+2	mV
Delay to Outout		V_{DIFF}=10mV			100	ns
Current Limit Section						
CS Threshold Set Current				200		µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1µF		10		%
Output Drivers Section						
Rise Time		C_L=3000pF		70		ns
Fall Time		C_L=3000pF		70		ns
Dead Band Time Between High Side and Synch Drive (Vcore Switcher Only)		C_L=3000pF		200		ns
Oscillator Section (Internal)						
Osc Frequency		Rt=Open		217		KHz
1.8V Regulator (V_{SEN}4)						
V_{SEN} Voltage	V_O4	T_A=25°C, Drive4=V_{SEN}4		1.800		V
V_{SEN} Voltage				1.800		V
Input Bias Current					2	µA
Output Drive Current			50			mA
1.5V Regulator (V_{SEN}3)						
V_{SEN} Voltage	V_O3	T_A=25°C, Drive3=V_{SEN}3		1.500		V
V_{SEN} Voltage				1.500		V
Input Bias Current					2	µA
Output Drive Current			50			mA
Power Good Section						
V_{SEN}1 UV Lower Trip Point		V_{SEN}1 Ramping Down		0.90Vs		V
V_{SEN}1 UV Upper Trip Point		V_{SEN}1 Ramping Up		0.92Vs		V
V_{SEN}1 UV Hysterises				0.02Vs		V
V_{SEN}1 HV Upper Trip Point		V_{SEN}1 Ramping Up		1.10Vs		V
V_{SEN}1 HV Lower Trip Point		V_{SEN}1 Ramping Down		1.08Vs		V
V_{SEN}1 HV Hysterises				0.02Vs		V
V_{SEN}2 Trip Point		Select <0.8V Select >2V		1.100 2.560		V
V_{SEN}3 Trip Point		Fix=Gnd Fix=Open		0.920 1.320		V
V_{SEN}4 Trip Point		Fix=Gnd Fix=Open		0.920 1.140		V
Power Good Output LO		R_L=3mA		0.4		V
Power Good Output HI		R_L=5K, Pull-Up to 5V		4.8		V
Fault (Overvoltage) Section						
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.17Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.15Vs		V
Fault Output HI		Io=3mA		10		V
Soft-Start Section						
Pull-Up Resistor to 5V		OCSet=0V, Phase=5V		20		µA

Note 1: Vs refers to the set point voltage given in Table 1.

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	1.075
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

Table 1 - Set point voltage vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Drive2	This pin controls the gate of an external MOSFET for the AGP linear regulator.
2	Fix	Leaving this pin open provides fixed output voltages of the 1.5V and 1.8V for the #3 and #4 linear regulators. When this pin is grounded the reference to the linear regulators are set to 1.26V and therefore the output of the regulators can be programmed to any voltages above the 1.26V using: $V_{OUT} = 1.26 \times (1 + R_{TOP}/R_{BOT})$ Where: R_{TOP}=Top resistor connected from the output to the V_{SENSE} pin R_{BOT}=Bottom resistor connected from the V_{SENSE} pin to ground.
3	VID4	This pin selects a range of output voltages for the DAC. When in the LOW state the range is 1.3V to 2.05V and when it switches to HI state the range is 2V to 3.5V. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
4	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
5	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
6	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
7	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
8	PGood	This pin is an open collector output that switches LO when any of the outputs are outside of the specified under-voltage trip point. It also switches low when $V_{SEN}1$ pin is more than 10% above the DAC voltage setting.

PIN#	PIN SYMBOL	PIN DESCRIPTION
9	SD	This pin provides shutdown for all the regulators. A TTL compatible, logic level high applied to this pin disables all the outputs and discharges the soft-start capacitor. The SD signal turns off the synchronous allowing the body diode to conduct and discharge the output capacitor.
10	$V_{SEN}2$	This pin provides the feedback for the AGP linear regulator. The Select pin when connected to the "Type Detect" pin of the AGP slot automatically selects the right voltage for the AGP V_{DDQ}.
11	Select	This pin provides automatic voltage selection for the AGP switching regulator. When it is pulled LO, the voltage is 1.5V and when left open or pulled to HI, the voltage is 3.3V.
12	SS	This pin provides the soft-start for all the regulators. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the outputs of the regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
13	Fault / Rt	This pin has dual function. It acts as an output of the over-voltage protection circuitry or it can be used to program the frequency using an external resistor . When used as a fault detector, if any of the switcher outputs exceed the OVP trip point, the Fault pin switches to 12V and the soft-start cap is discharged. If the Fault pin is to be connected to any external circuitry, it needs to be buffered.
14	$V_{SEN}4$	This pin provides the feedback for the linear regulator that its output drive is Drive4.
15	Drive4	This pin controls the gate of an external MOSFET for the 1.8V chip set linear regulator.
16	NC	This pin has no connection.
17	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane.
18	Drive3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
19	$V_{SEN}3$	This pin provides the feedback for the linear regulator that its output drive is Drive3.
20	V5	5V supply voltage. A high frequency capacitor (0.1 to 1μF) must be placed close to this pin and connected from this pin to the ground plane for noise free operation.
21	Fb	This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to $V_{OUT}1$ and ground to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from $V_{OUT}1$ to Fb1 must be less than 1000Ω.
22	$V_{SEN}1$	This pin is internally connected to the under-voltage and over-voltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply.
23	OCSet	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the current sense threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
24	PGnd	This pin serves as the Power ground pin and must be connected directly to the ground plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1μF) must be connected from V12 pin to this pin for noise free operation.
25	LGate	Output driver for the synchronous power MOSFET for the Core supply.
26	Phase	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
27	UGate	Output driver for the high side power MOSFET for the Core supply.
28	V12	This pin is connected to the 12V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1μF) must be placed close to this pin and PGnd pin and be connected directly from this pin to the ground plane for the noise free operation.

BLOCK DIAGRAM

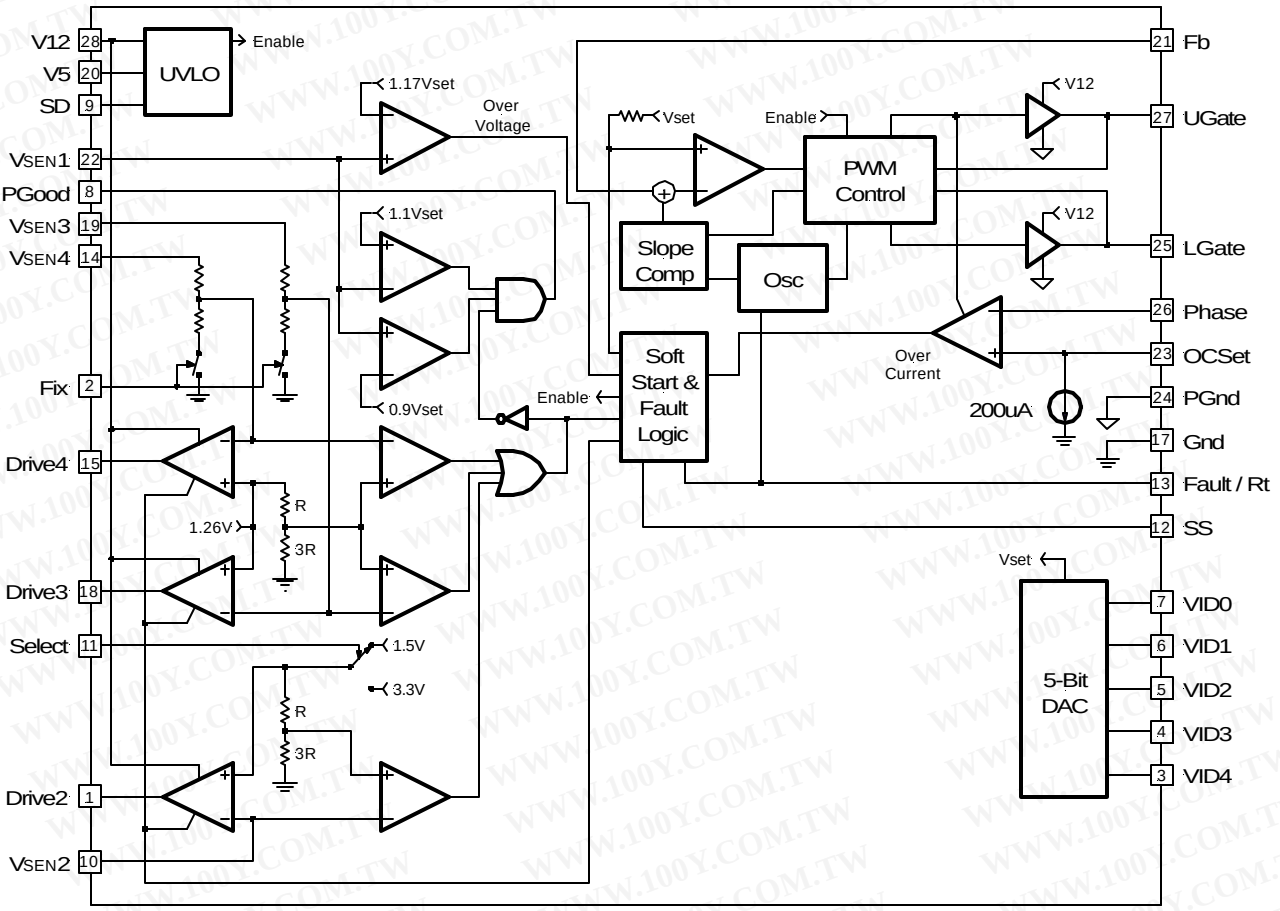


Figure 2 - Simplified block diagram of the IRU3027.

TYPICAL APPLICATION

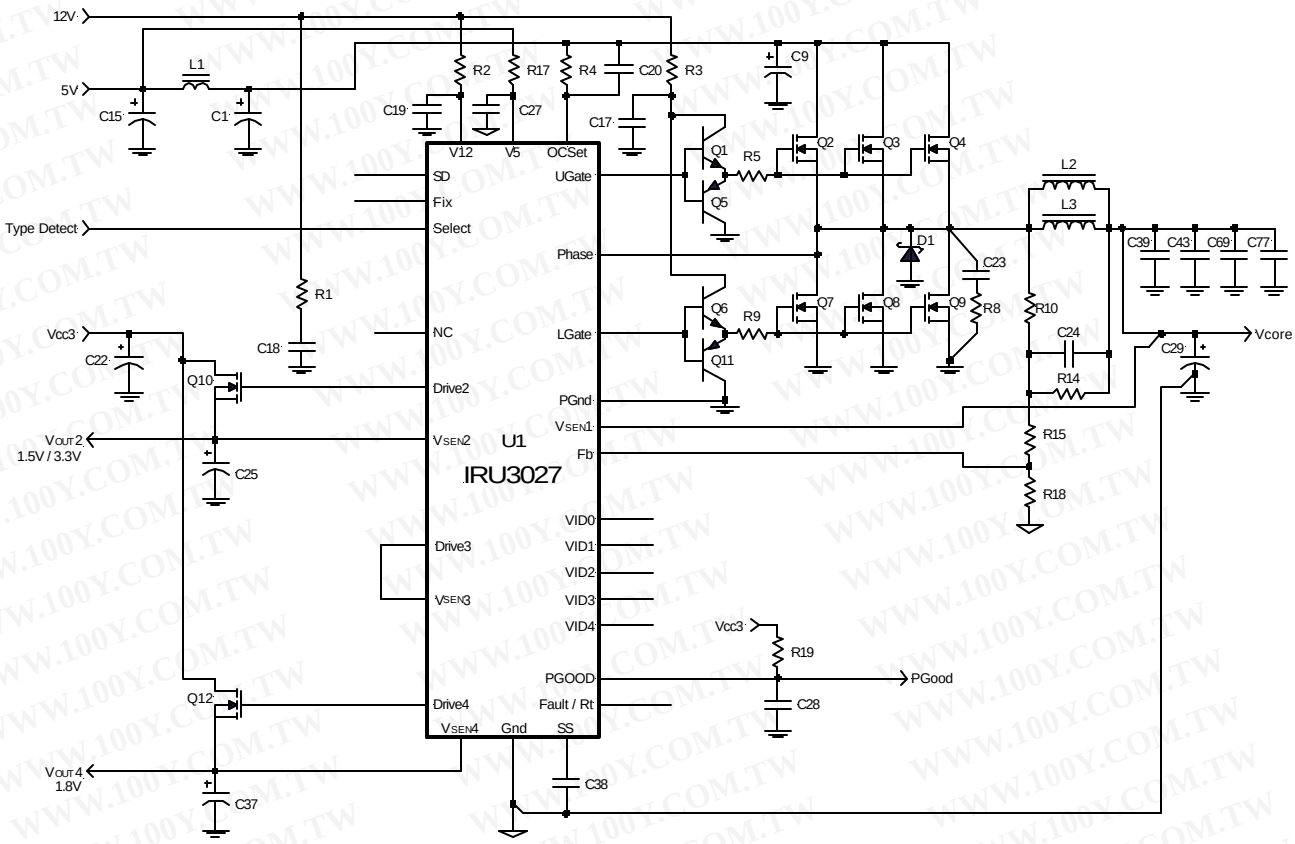


Figure 3 - Typical application of IRU3027 for the AMD Slot A socket.

IRU3027 APPLICATION PARTS LIST

Dual Layout with HIP6019

Ref Desig	Description	Qty	Part #	Manuf
Q1, 6	Transistor	2	2SD882, TO-226 package	Fairchild
Q2, 3, 4	MOSFET	3	IRF3706S, TO-263 package	IR
Q5, 11	Transistor	2	2SB772, TO-226 package	Fairchild
Q7, 8, 9	MOSFET	3	IRL2203NS, TO-263 package	IR
Q10	MOSFET	1	IRLR3103S, TO-252 package	IR
Q12	MOSFET	1	IRLR024, TO-252 package	IR
D1	Diode	1	MBR1535CT, TO-220 package	IR
L1	Inductor	1	L=1μH, 5052B core with 5 turns of triple 0.8mm wire	Micro Metal
L2, 3	Inductor	2	L=1.8μH, 6018 core with 6 turns of triple 0.8mm wire	Micro Metal
C1	Capacitor, Ceramic	8	1μF, 0603	
C9	Capacitor, Electrolytic	6	10MV1500GX, 1500μF, 10V	Sanyo
C15	Capacitor, Electrolytic	1	10MV1500GX, 1500μF, 10V	Sanyo
C16	Capacitor, Ceramic	1	1μF, 0603	
C17, 18, 19, 21	Capacitor, Ceramic	4	1μF, 0805	
C20	Capacitor, Ceramic	1	220pF, 0603	
C22, 26	Capacitor, Electrolytic	2	6MV1000GX, 1000μF, 6.3V	Sanyo
C23	Capacitor, Ceramic	1	1000pF, 0805	
C24, 27	Capacitor, Ceramic	2	1μF, 0603	
C25, 37	Capacitor, Electrolytic	2	6MV1500GX, 1500μF, 6.3V	Sanyo
C28, 38	Capacitor, Ceramic	2	0.1μF, 0603	
C29	Capacitor, Electrolytic	8	6MV2200GX, 2200μF, 6.3V	Sanyo
C39	Capacitor, Ceramic	4	4.7μF, 0805	
C43	Capacitor, Ceramic	26	1μF, 0603	
C69	Capacitor, Ceramic	8	0.01μF, 0603	
C77	Capacitor, Ceramic	8	39pF, 0603	
R1, 2, 3, 7, 16, 21	Resistor	6	10Ω, 5%, 0603	
R4	Resistor	1	2KΩ, 5%, 0603	
R5, 9	Resistor	4	1Ω, 5%, 0805	
R8	Resistor	1	4.7Ω, 5%, 0805	
R10, 14	Resistor	2	3.3KΩ, 1%, 0603	
R11, 20	Resistor	2	0Ω, 0603	
R12	Resistor	1	47KΩ, 5%, 0603	
R15	Resistor	1	2.2KΩ, 1%, 0603	
R17	Resistor	1	1Ω, 0603	
R18	Resistor	1	100KΩ, 1%, 0603	
R19	Resistor	1	10KΩ, 5%, 0603	

International
IOR Rectifier

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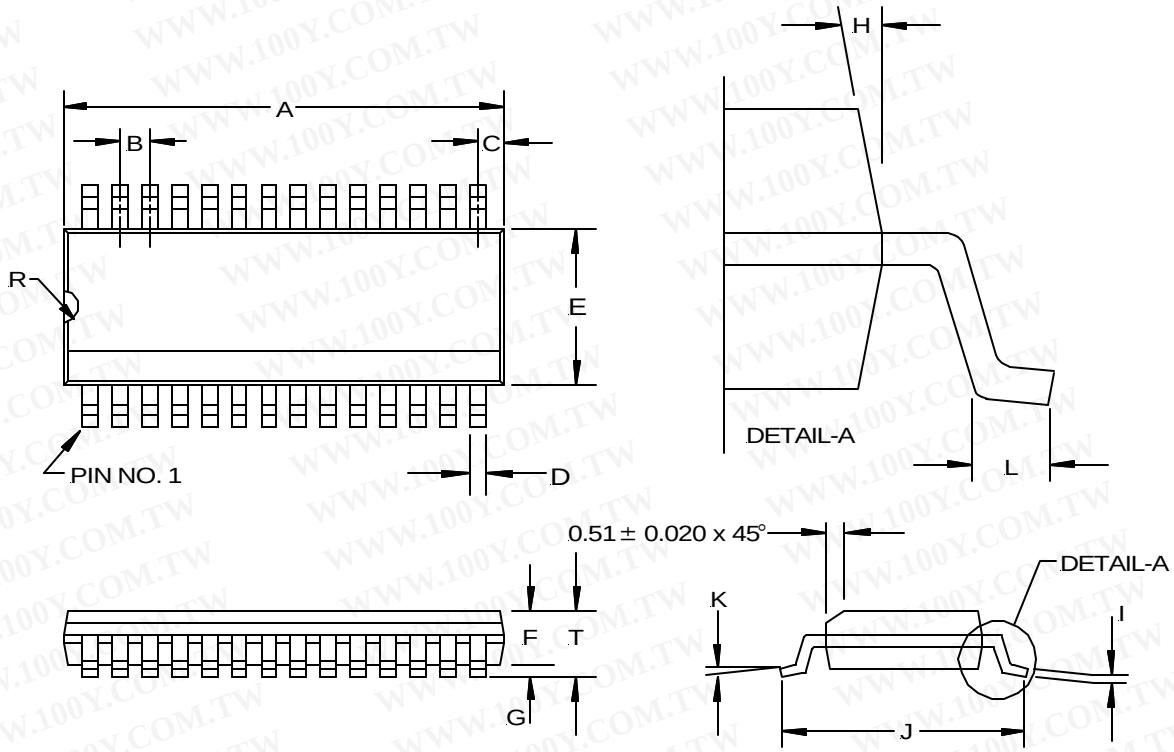
(W) SOIC Package
28-Pin Surface Mount, Wide Body

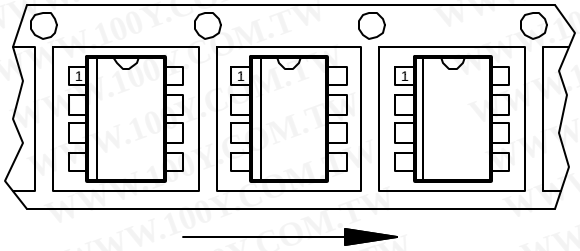


SYMBOL	28-PIN	
	MIN	MAX
A	17.73	17.93
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
W	SOIC, Wide Body	28	27	1000	Fig A



Feed Direction
Figure A