Document Title

128M x 8 Bit NAND Flash Memory

Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	Aug. 24. 2003	Advance
0.1	1. The tADL(Address to Data Loading Time) is added. - tADL Minimum 100ns (Page 11, 23~26) - tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle at program operation. 2. Added Addressing method for program operation	Jan. 27. 2004	Preliminary
0.2	1. Add the Protrusion/Burr value in WSOP1 PKG Diagram.	Apr. 23. 2004	Preliminary
0.3	1. PKG(TSOP1, WSOP1) Dimension Change	May. 19. 2004	

128M x 8 Bit NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9F1G08Q0A	1.70 ~ 1.95V	X8	Only available in MCP
K9F1G08U0A-Y,P	2.7 ~ 3.6V		TSOP1
K9F1G08U0A-V,F			WSOP1

FEATURES

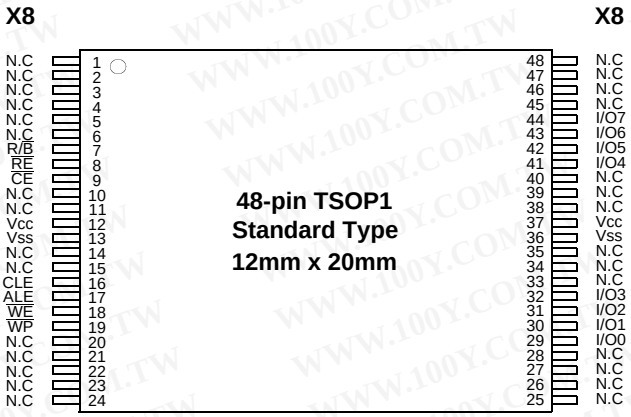
- Voltage Supply
  - -1.8V device(K9F1G08Q0A): 1.70V~1.95V
  - -3.3V device(K9F1G08U0A): 2.7 V ~3.6 V
- Organization
  - Memory Cell Array : (128M + 4,096K)bit x 8bit
  - Data Register : (2K + 64)bit x8bit
  - Cache Register : (2K + 64)bit x8bit
- Automatic Program and Erase
  - Page Program : (2K + 64)Byte
  - Block Erase : (128K + 4K)Byte
- Page Read Operation
  - Page Size : 2K-Byte
  - Random Read : 25µs(Max.)
  - Serial Access : 30ns(Min.) : (K9F1G08U0A)
    50ns(Min.) : (K9F1G08Q0A)
- Fast Write Cycle Time
  - Program time : 300µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Cache Program Operation for High Performance Program
- Intelligent Copy-Back Operation
- Unique ID for Copyright Protection
- Package :
  - K9F1G08U0A-YCB0/YIB0
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9F1G08U0A-VIB0
    48 - Pin WSOP I (12X17X0.7mm)
  - K9F1G08U0A-PCB0/PIB0
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)- Pb-free Package
  - K9F1G08U0A-FIB0
    48 - Pin WSOP I (12X17X0.7mm)- Pb-free Package
    * K9F1G08U0A-V,F(WSOPI) is the same device as K9F1G08U0A-Y,P(TSOP1) except package type.

GENERAL DESCRIPTION

Offered in 128Mx8bit the K9F1G08X0A is 1G bit with spare 32M bit capacity. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 300µs on the 2112-byte page and an erase operation can be performed in typical 2ms on a 128K-byte block. Data in the data page can be read out at 50ns (30ns, K9F1G08U0A) cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F1G08X0A's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9F1G08X0A is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

PIN CONFIGURATION (TSOP1)

K9F1G08X0A-YCB0,PCB0/YIB0,PIB0

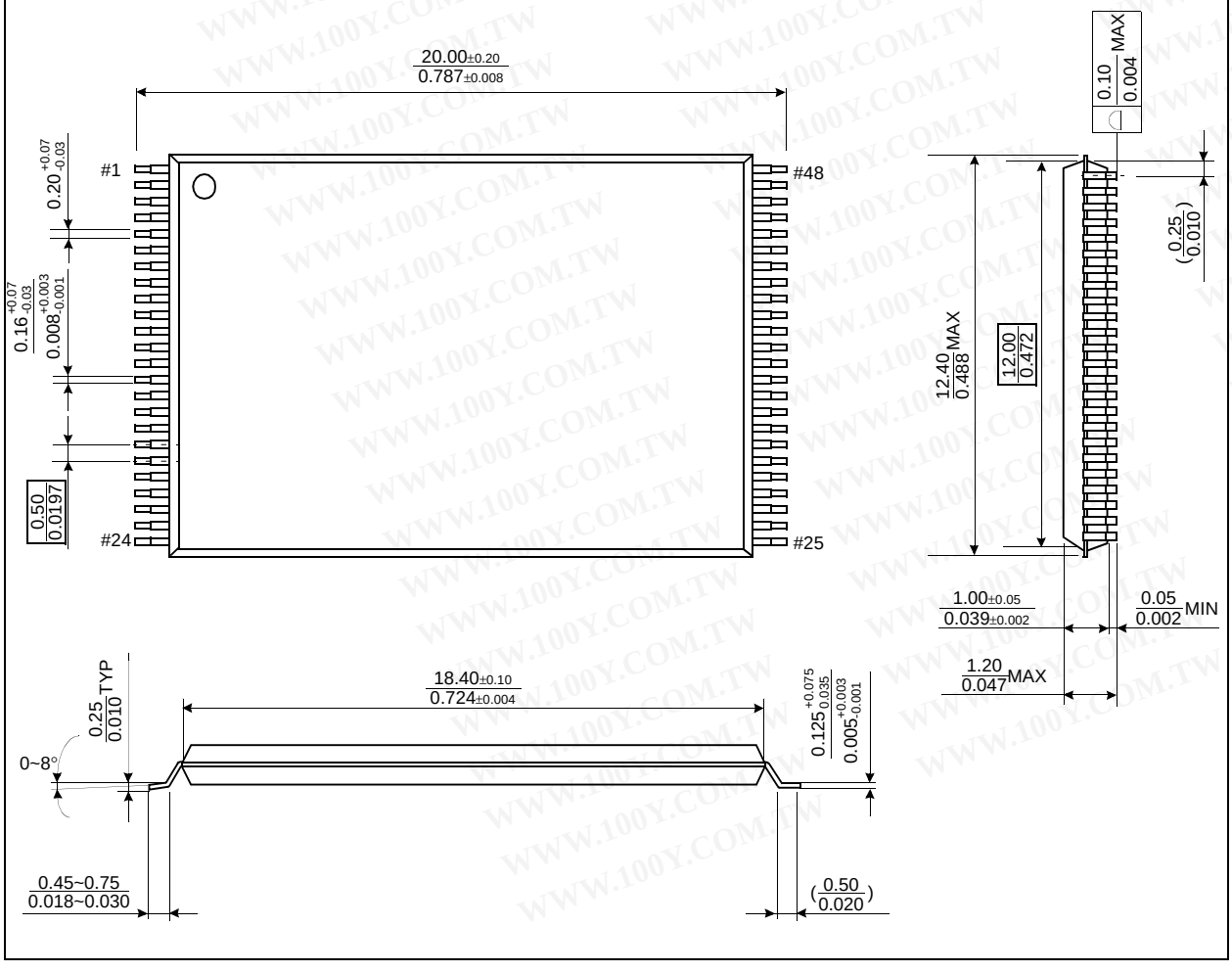


PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

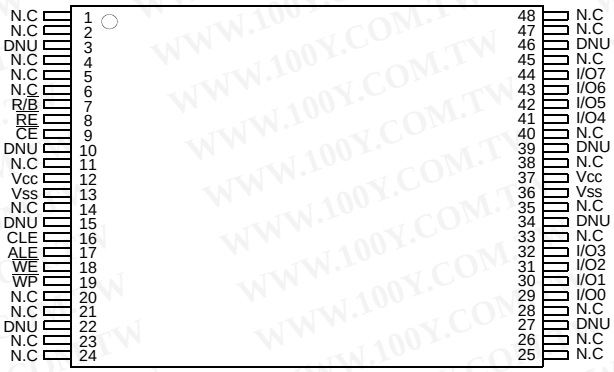
48 - TSOP1 - 1220AF

Unit :mm/Inch



PIN CONFIGURATION (WSOP1)

K9F1G08U0A-VIB0,FIB0

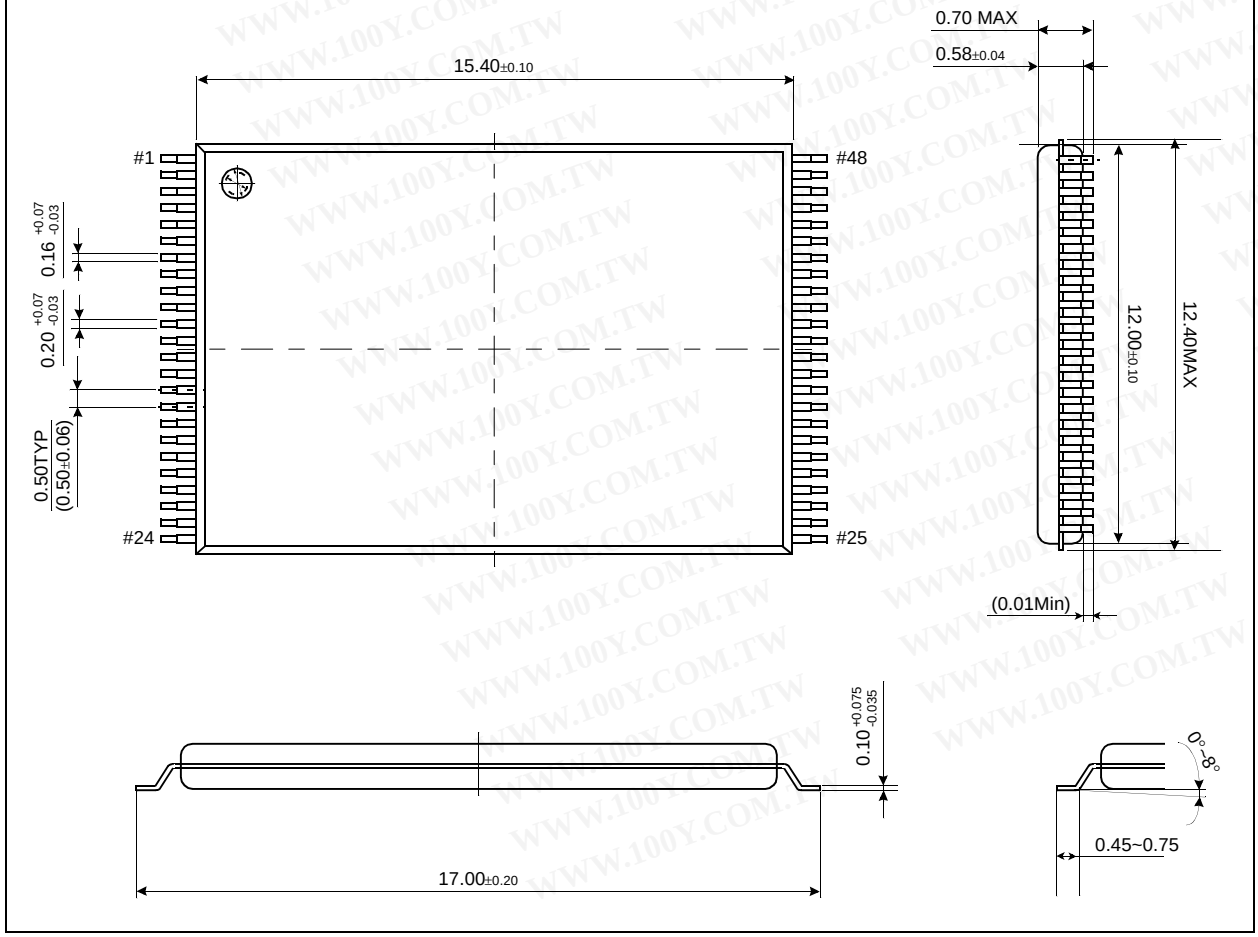


PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC VERY VERY THIN SMALL OUT-LINE PACKAGE TYPE (I)

48 - WSOP1 - 1217F

Unit :mm



PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
V_{CC}	**POWER** V_{CC} is the power supply for device.
V_{SS}	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.

NOTE : Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
Do not leave V_{CC} or V_{SS} disconnected.

Figure 1-1. K9F1G08X0A (X8) Functional Block Diagram

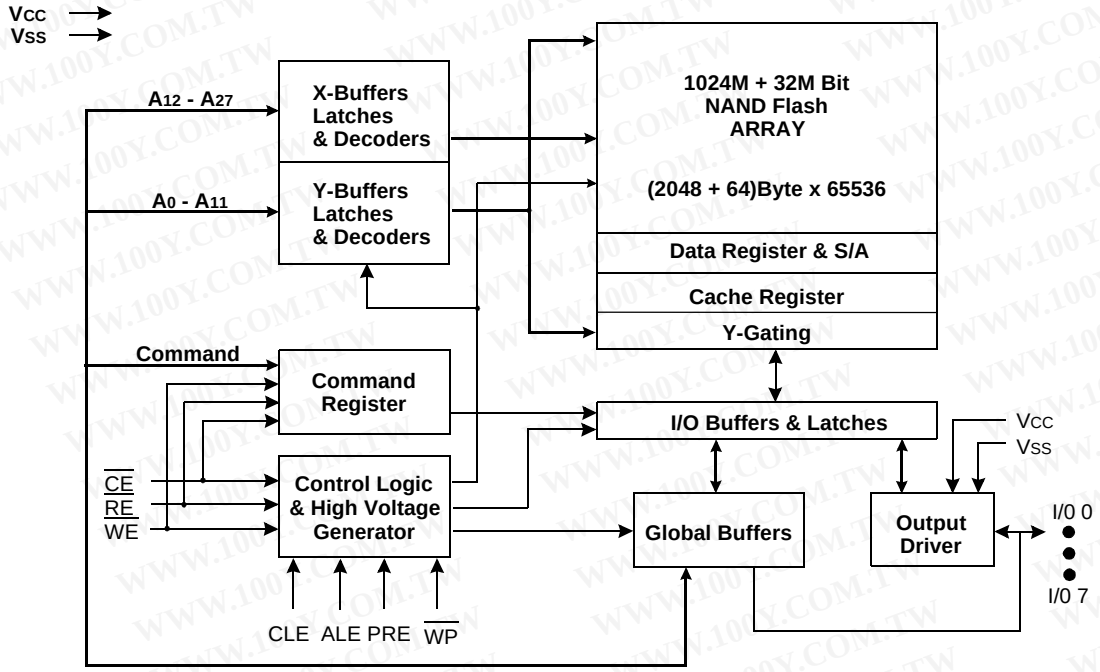
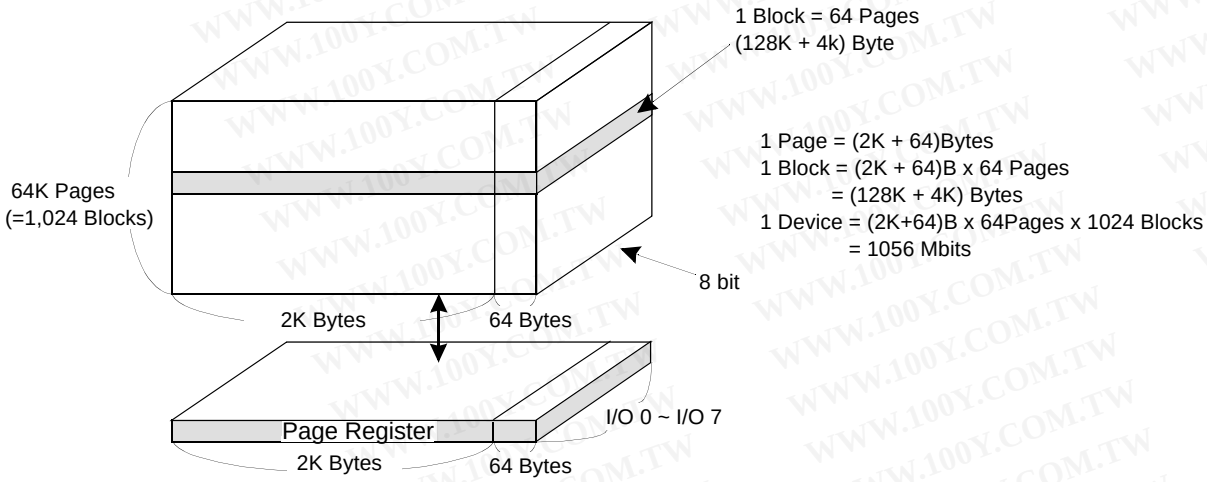


Figure 2-1. K9F1G08X0A (X8) Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	Column Address
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	Row Address

NOTE : Column Address : Starting Address of the Register.

* L must be set to "Low".

* The device ignores any additional input of address cycles than required.

Product Introduction

The K9F1G08X0A is a 1056Mbit(1,107,296,256 bit) memory organized as 65,536 rows(pages) by 2112x8 columns. Spare 64 columns are located from column address of 2048~2111. A 2112-byte data register and a 2112-byte cache register are serially connected to each other. Those serially connected registers are connected to memory cell arrays for accommodating data transfer between the I/O buffers and memory cells during page read and page program operations. The memory array is made up of 32 cells that are serially connected to form a NAND structure. Each of the 32 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 32 cells. Total 1081344 NAND cells reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1024 separately erasable 128K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9F1G08X0A.

The K9F1G08X0A has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE to low while CE is low. Those are latched on the rising edge of WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. The 128M byte physical space requires 28 addresses, thereby requiring four cycles for addressing: 2 cycles of column address, 2 cycles of row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9F1G08X0A.

The device provides cache program in a block. It is possible to write data into the cache registers while data stored in data registers are being programmed into memory cells in cache program mode. The program performace may be dramatically improved by cache program when there are lots of pages of data to be programmed.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory. Since the time-consuming serial access and data-input cycles are removed, system performance for solid-state disk application is significantly increased.

Table 1. Command Sets

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Cache Program	80h	15h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input*	85h	-	
Random Data Output*	05h	E0h	
Read Status	70h		O

NOTE : 1. Random Data Input/Output can be executed in a page.
2. Command not specified in command sets table is not permitted to be entered to the device, which can raise erroneous operation.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			1.8V DEVICE	3.3V/2.65V DEVICE	
Voltage on any pin relative to V_{SS}		$V_{IN/OUT}$	-0.6 to + 2.45	-0.6 to + 4.6	V
		V_{CC}	-0.2 to + 2.45	-0.6 to + 4.6	
Temperature Under Bias	K9F1G08X0A-XCB0	T_{BIAS}	-10 to +125		°C
	K9F1G08X0A-XIB0		-40 to +125		
Storage Temperature	K9F1G08X0A-XCB0	T_{STG}	-65 to +150		°C
	K9F1G08X0A-XIB0				
Short Circuit Current		Ios	5		mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9F1G08X0A-XCB0 :T_A=0 to 70°C, K9F1G08X0A-XIB0:T_A=-40 to 85°C)

Parameter	Symbol	K9F1G08Q0A(1.8V)			K9F1G08U0A(3.3V)			Unit
		Min	Typ.	Max	Min	Typ.	Max	
Supply Voltage	V_{CC}	1.70	1.8	1.95	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	K9F1G08Q0A			K9F1G08U0A			Unit
				1.8V			3.3V			
				Min	Typ	Max	Min	Typ	Max	
Operating Current	Page Read with Serial Access	ICC1	tRC=50ns, $\overline{CE}$=VIL IOUT=0mA	-	10	20	-	15	30	mA
	Program	ICC2	-	-	10	20	-	15	30	
	Erase	ICC3	-	-	10	20	-	15	30	
Stand-by Current(TTL)		ISB1	$\overline{CE}$=VIH, $\overline{WP}$=0V/VCC	-	-	1	-	-	1	
Stand-by Current(CMOS)		ISB2	$\overline{CE}$=VCC-0.2, $\overline{WP}$=0V/VCC	-	10	50	-	10	50	µA
Input Leakage Current		ILI	VIN=0 to Vcc(max)	-	-	±10	-	-	±10	
Output Leakage Current		ILO	VOUT=0 to Vcc(max)	-	-	±10	-	-	±10	
Input High Voltage		VIH*	-	0.8xVCC	-	VCC +0.3	0.8xVcc	-	VCC +0.3	V
Input Low Voltage, All inputs		VIL*	-	-0.3	-	0.2xVcc	-0.3	-	0.2xVcc	
Output High Voltage Level		VOH	K9F1G08Q0A :IOH=-100µA K9F1G08U0A :IOH=-400µA	Vcc -0.1	-	-	2.4	-	-	
Output Low Voltage Level		VOL	K9F1G08Q0A :IOL=100uA K9F1G08U0A :IOL=2.1mA	-	-	0.1	-	-	0.4	
Output Low Current(R/$\overline{B}$)		IOL(R/$\overline{B}$)	K9F1G08Q0A :VOL=0.1V K9F1G08U0A :VOL=0.4V	3	4	-	8	10	-	mA

NOTE : VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20 ns or less.

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	1004	-	1024	Blocks

NOTE :
1. The K9F1G08X0A may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.

AC TEST CONDITION

(K9F1G08X0A-XCB0 :TA=0 to 70°C, K9F1G08X0A-XIB0:TA=-40 to 85°C

K9F1G08Q0A : Vcc=1.70V~1.95V, K9F1G08U0A : Vcc=2.7V~3.6V unless otherwise noted)

Parameter	K9F1G08Q0A	K9F1G08U0A
Input Pulse Levels	0V to Vcc	0V to Vcc
Input Rise and Fall Times	5ns	5ns
Input and Output Timing Levels	Vcc/2	Vcc/2
Output Load	1 TTL GATE and CL=30pF	1 TTL GATE and CL=50pF

CAPACITANCE (T_A=25°C, V_{CC}=1.8V/3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(4clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(4clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	300	700	µs
Dummy Busy Time for Cache Program		t_{CBSY}		3	700	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	4	cycles
	Spare Array		-	-	4	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

NOTE : 1. Max. time of t_{CBSY} depends on timing between internal program completion and data in

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min		Max		Unit
		K9F1G08Q0A	K9F1G08U0A	K9F1G08Q0A	K9F1G08U0A	
CLE setup Time	t_{CLS}	25	10	-	-	ns
CLE Hold Time	t_{CLH}	10	5	-	-	ns
$\overline{CE}$ setup Time	t_{CS}	35	15	-	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	5	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25	15	-	-	ns
ALE setup Time	t_{ALS}	25	10	-	-	ns
ALE Hold Time	t_{ALH}	10	5	-	-	ns
Data setup Time	t_{DS}	20	10	-	-	ns
Data Hold Time	t_{DH}	10	5	-	-	ns
Write Cycle Time	t_{WC}	45	30	-	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	10	-	-	ns
ALE to Data Loading Time	t_{ADL}	100(1)	100(1)	-	-	ns

NOTE : 1. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

AC Characteristics for Operation

Parameter	Symbol	Min		Max		Unit
		K9F1G08Q0A	K9F1G08U0A	K9F1G08Q0A	K9F1G08U0A	
Data Transfer from Cell to Register	t_R	-	-	25	25	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	10	-	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	10	-	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	20	-	-	ns
RE Pulse Width	t_{RP}	25	15	-	-	ns
WE High to Busy	t_{WB}	-	-	100	100	ns
Read Cycle Time	t_{RC}	50	30	-	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	-	30	18	ns
$\overline{CE}$ Access Time	t_{CEA}	-	-	45	23	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	-	30	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	-	20	20	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold	t_{OH}	15	15	-	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	10	-	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	0	-	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	60	-	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	-	5/10/500(1)	5/10/500(1)	µs

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFh data at the column address of 2048. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the original invalid block information is prohibited.

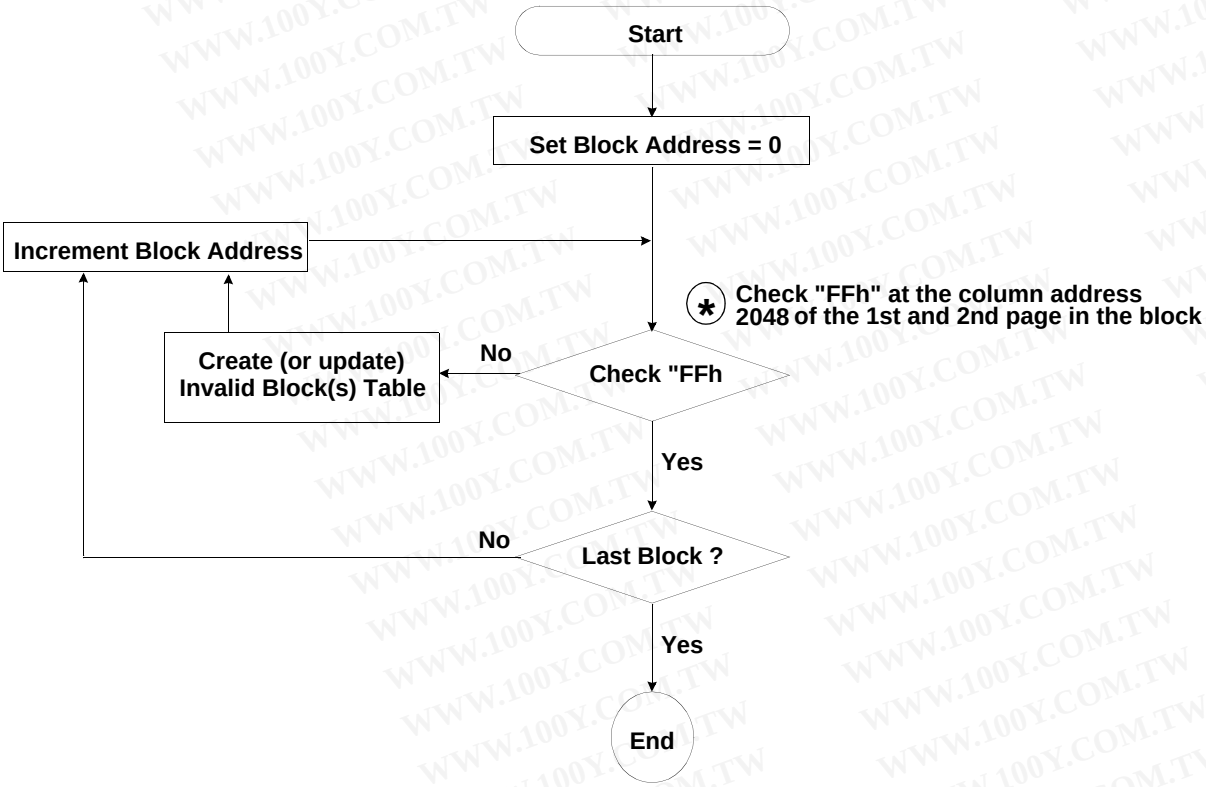


Figure 3. Flow chart to create invalid block table.

NAND Flash Technical Notes *(Continued)*

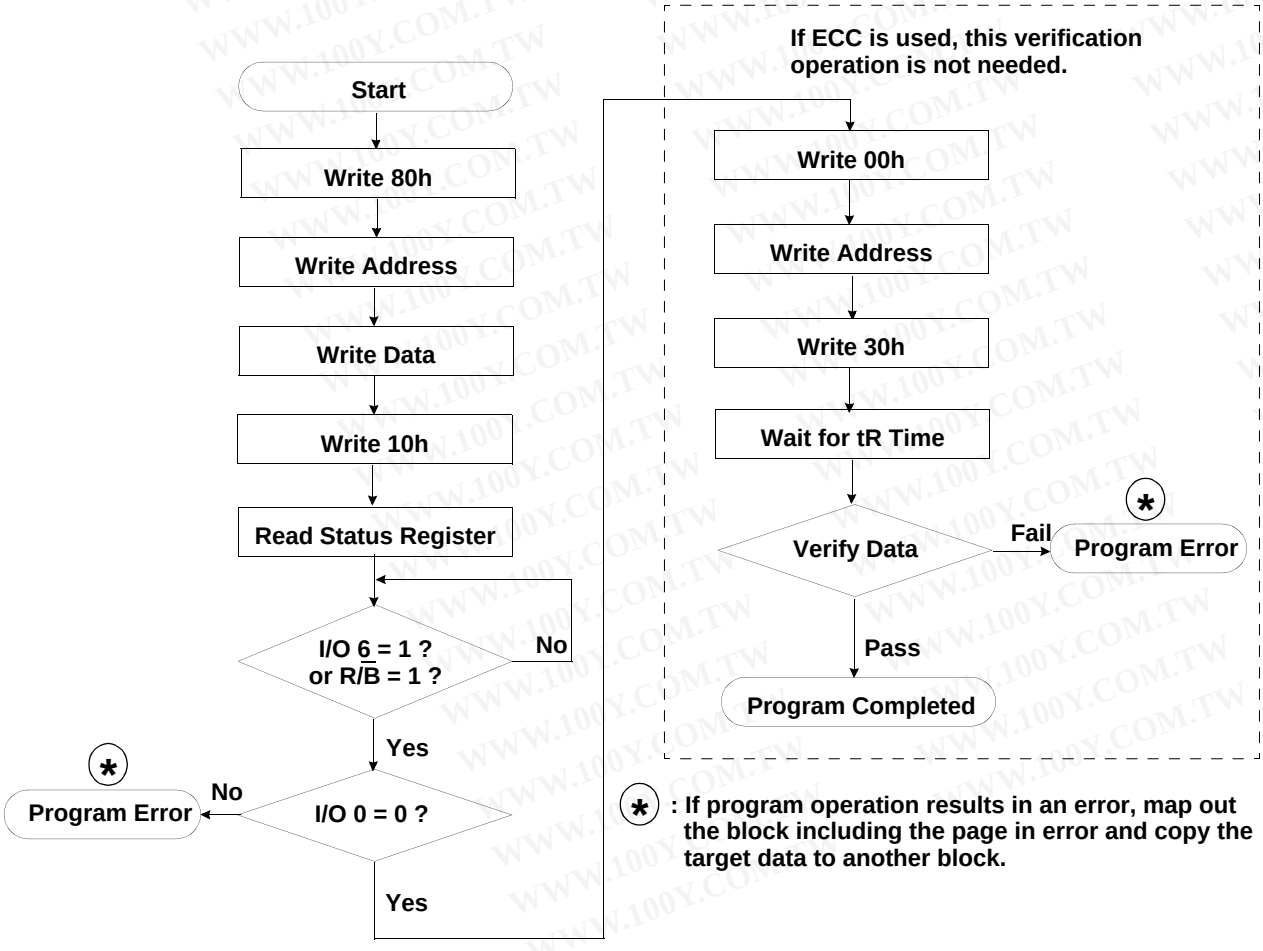
Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

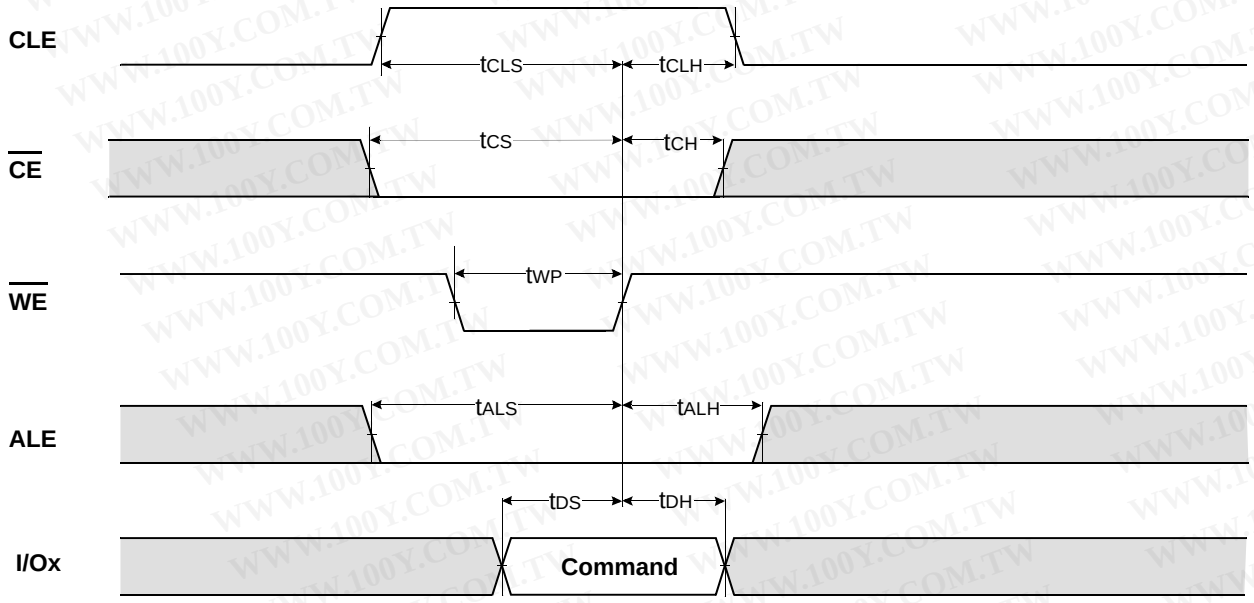
Program Flow Chart



NOTE

Device	I/O	DATA	ADDRESS			
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2
K9F1G08X0A	I/O 0 ~ I/O 7	~2112byte	A0~A7	A8~A11	A12~A19	A20~A27

Command Latch Cycle



Address Latch Cycle