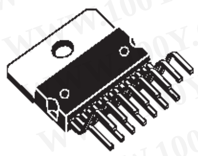
L4975A

5A SWITCHING REGULATOR

- 5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



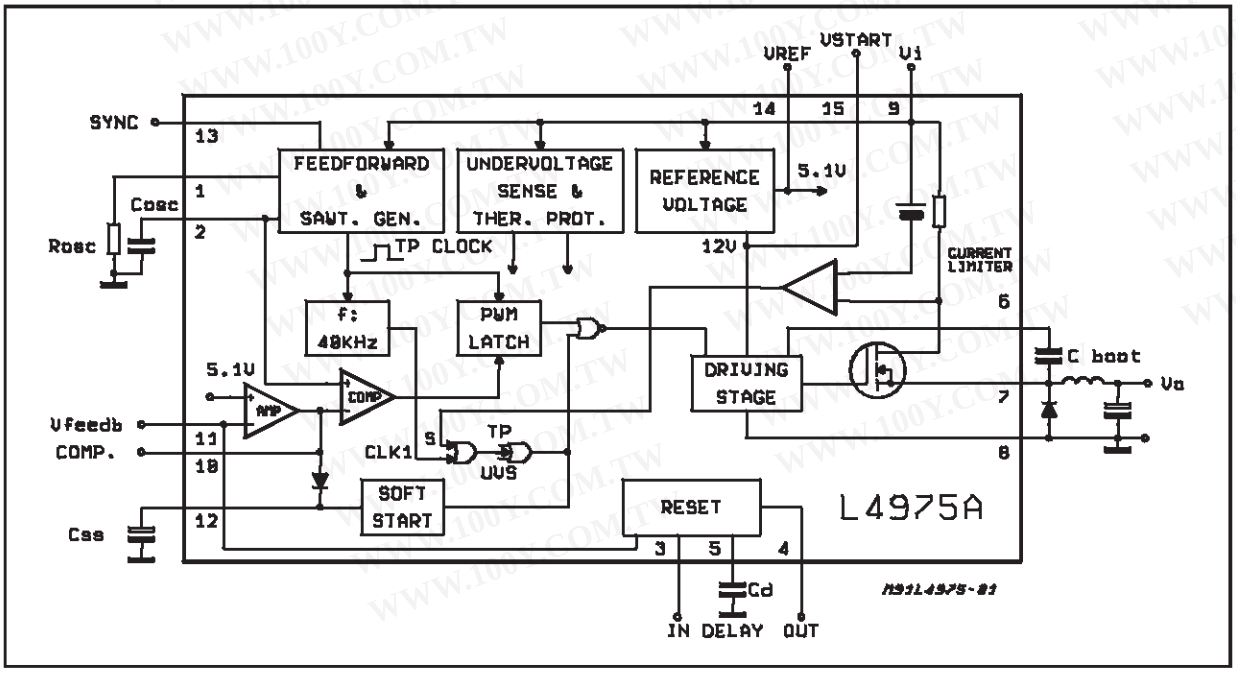
Multiwatt15V
ORDERING NUMBER: L4975A

DESCRIPTION

The L4975A is a stepdown monolithic power switching regulator delivering 5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4975A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

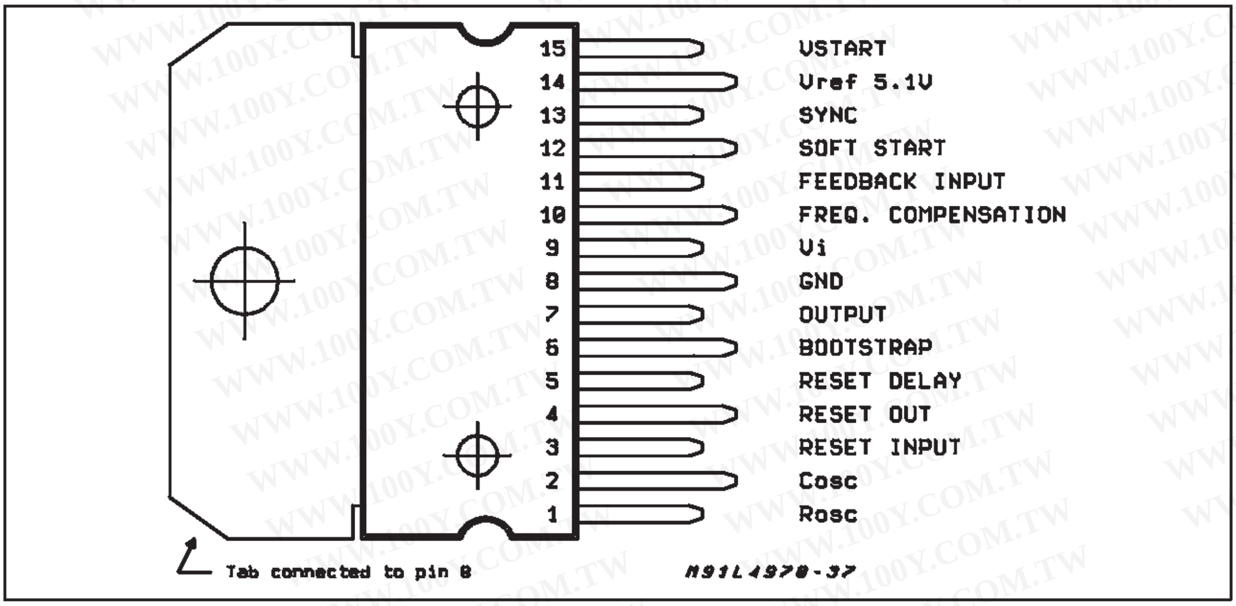
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$ $R_{th\ j\text{-}amb}$	Thermal Resistance Junction-case Thermal Resistance Junction-ambient	max max	1 35	°C/W °C/W

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D-MOS transistor.
7	OUTPUT	Regulator Output.
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage.
10	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation; It is connected via a divider for higher voltages.
12	SOFT START	Soft Start Time Constant. A capacitor is connected between thi sterminal and ground to define the soft start time constant.
13	SYNC INPUT	Multiple L4975A are synchronized by connecting pin 13 inputs together or via an external syncr. pulse.
14	V_{ref}	5.1V V_{ref} Device Reference Voltage.
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage.

CIRCUIT OPERATION (refer to the block diagram)

The L4975A is a 5A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 5A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

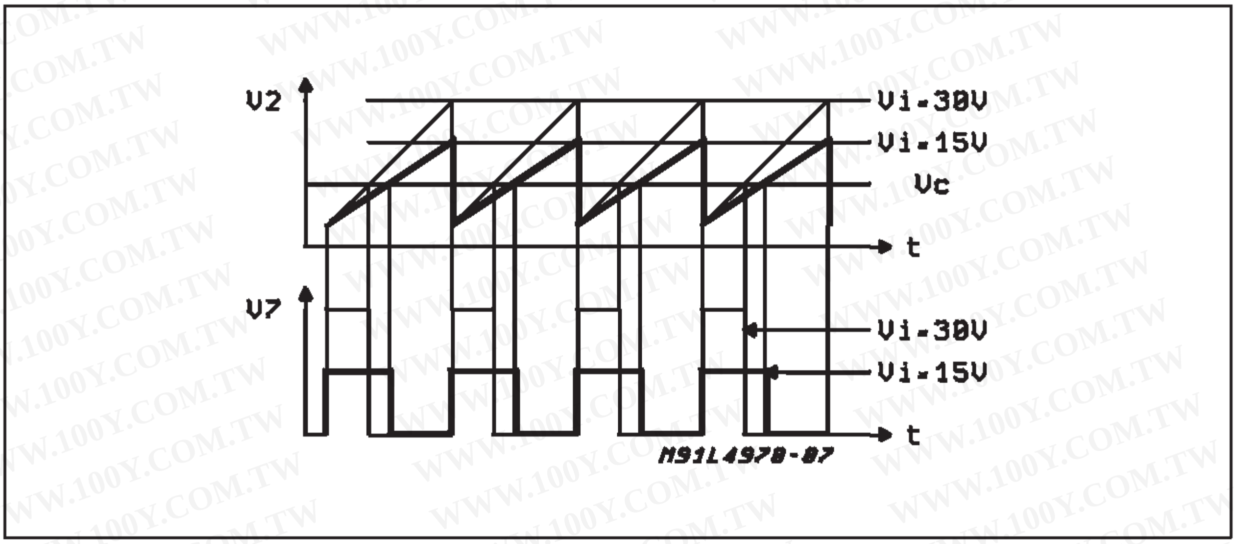


Figure 2: Soft Start Function

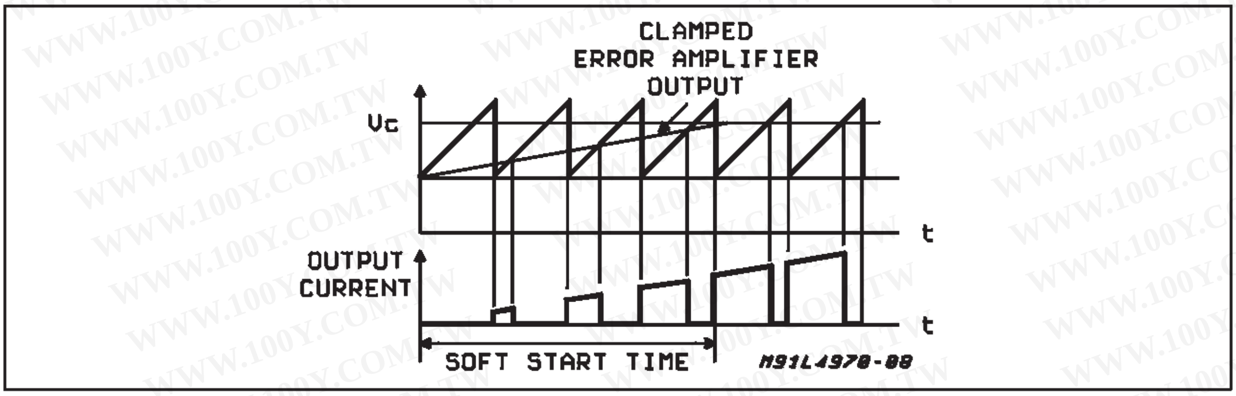
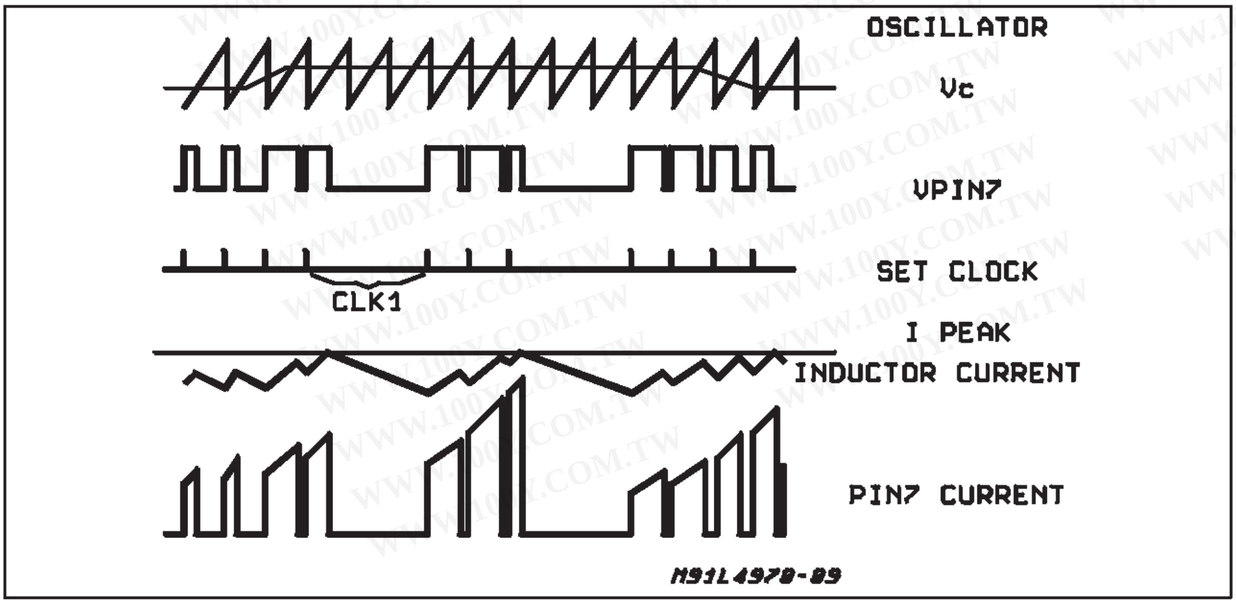


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

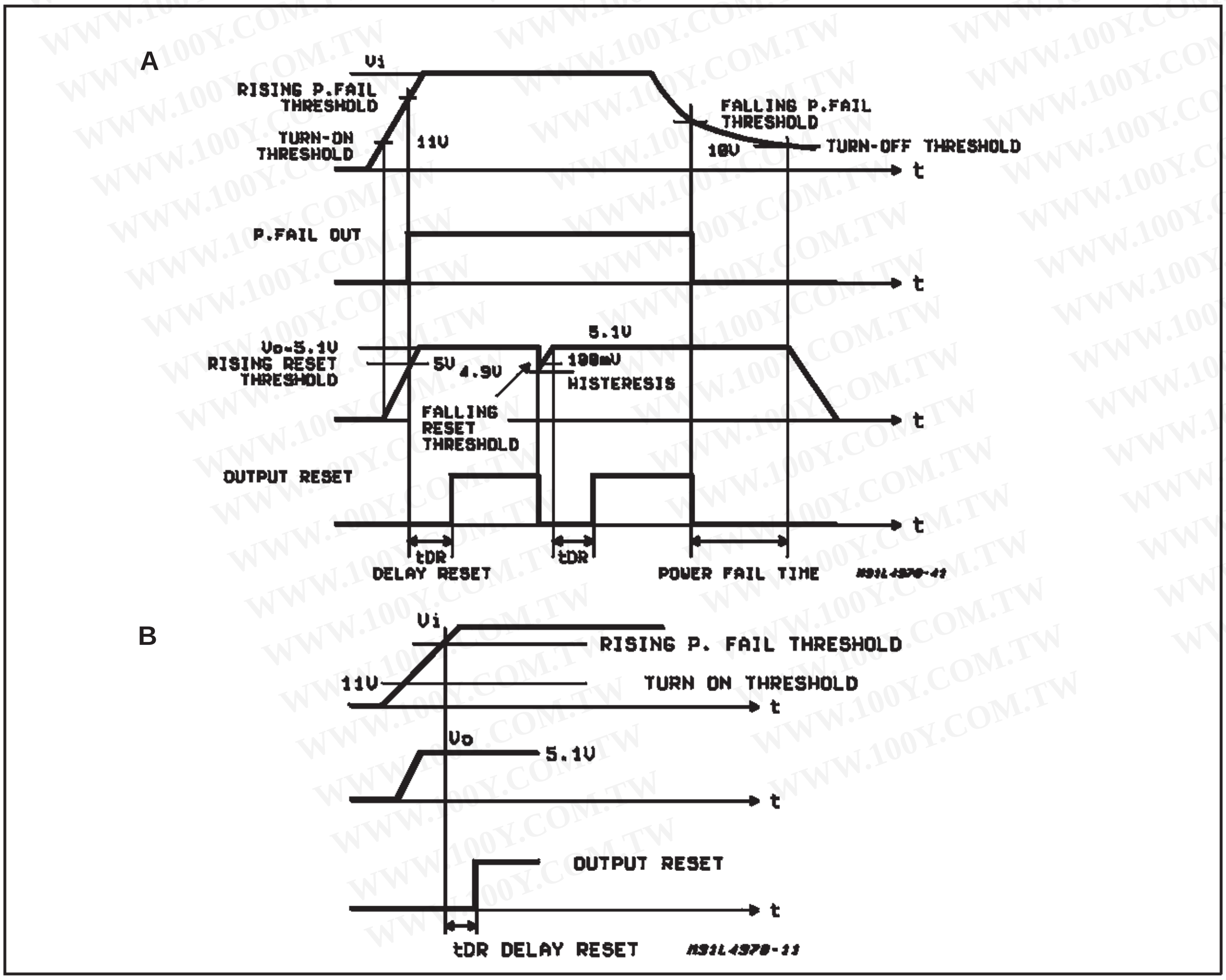
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	$V_o = V_{ref}$ to 40V I_o = 5A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 3A; $V_o = V_{ref}$	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A; $V_o = V_{ref}$		12	30	mV	5
ΔV_o	Load Regulation	$V_o = V_{ref}$ I_o = 2A to 4A I_o = 1A to 5A		 10 20	 30 50	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 3A I_o = 5A		0.4 0.55	0.6 0.8	V V	5
I_{7L}	Max. Limiting Current	V_i = 15 to 50V $V_o = V_{ref}$ to 40V	5.5	6.5	7.5	A	5
η	Efficiency	I_o = 3A $V_o = V_{ref}$ V_o = 12V	 70	 75 80		 % %	5
		I_o = 5A $V_o = V_{ref}$ V_o = 12V	 80	 85 92		 % %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 3A f = 100Hz; $V_o = V_{ref}$	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$; R_4 = 10KΩ I_o = 5A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	V_{12} = 0; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	V_i = 55V; S3 = A; V_{12} = 0			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V; V_{11} = 0V	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	I_{12} = 20mA; V_9 = 10V			1	V	7B
		I_{12} = 200µA; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	I_{10} = -100µA; S1 = C V_{11} = 4.7V	6			V	7C
V_{10L}	Low Level Out Voltage	I_{10} = +100µA; S1 = C V_{11} = 5.3V;			1.2	V	7C
I_{10H}	Source Output Current	V_{10} = 1V; S1 = E V_{11} = 4.7V	100	150		µA	7C
I_{10L}	Sink Output Current	V_{10} = 6V; S1 = D V_{11} = 5.3V	100	150		µA	7C
I_{11}	Input Bias Current	R_S = 10KΩ		0.4	3	µA	–
G_V	DC Open Loop Gain	V_{VCM} = 4V; R_S = 10Ω	60			dB	–
SVR	Supply Voltage Rejection	15 < V_i < 50V; R_S = 10Ω	60	80		dB	–
V_{OS}	Input Offset Voltage	R_S = 50Ω		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B	1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C, S2 = B; V_i = 15V		2.5		V	7A
		S1 = C, S2 = B; V_i = 45V		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; I_1 = 100µA		270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; I1 = 1mA	2.4	2.7		mA	7A

SYNC FUNCTION (pin 13)

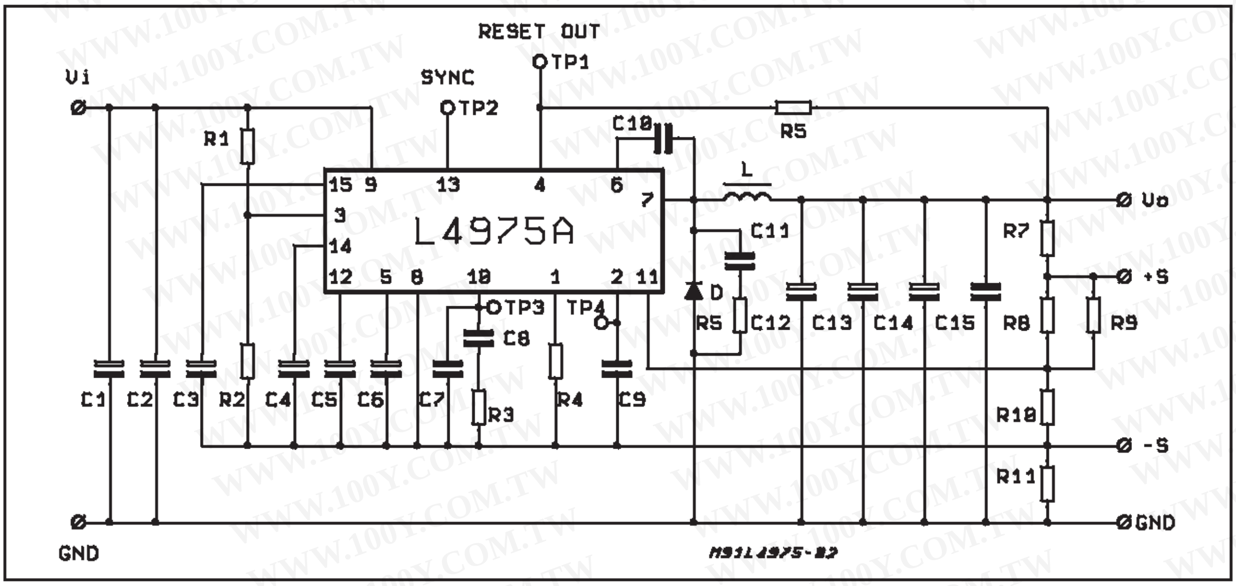
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	V_i = 15V to 50V; V_{12} = 0; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	V_{12} = 0; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	V_2 = V_{13} = 0.9V; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	V_{13} = 3.5V; S4 = A; S1 = C; S2 = B			2	mA	7A
V_{13}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} –120	V_{ref} –100	V_{ref} –80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	Vi = 15 to 50V V_3 = 5.3V	4.77	V_{ref} –200	V_{ref} –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	Vi = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresys		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 5A ; f_{SW} = 200KHz)

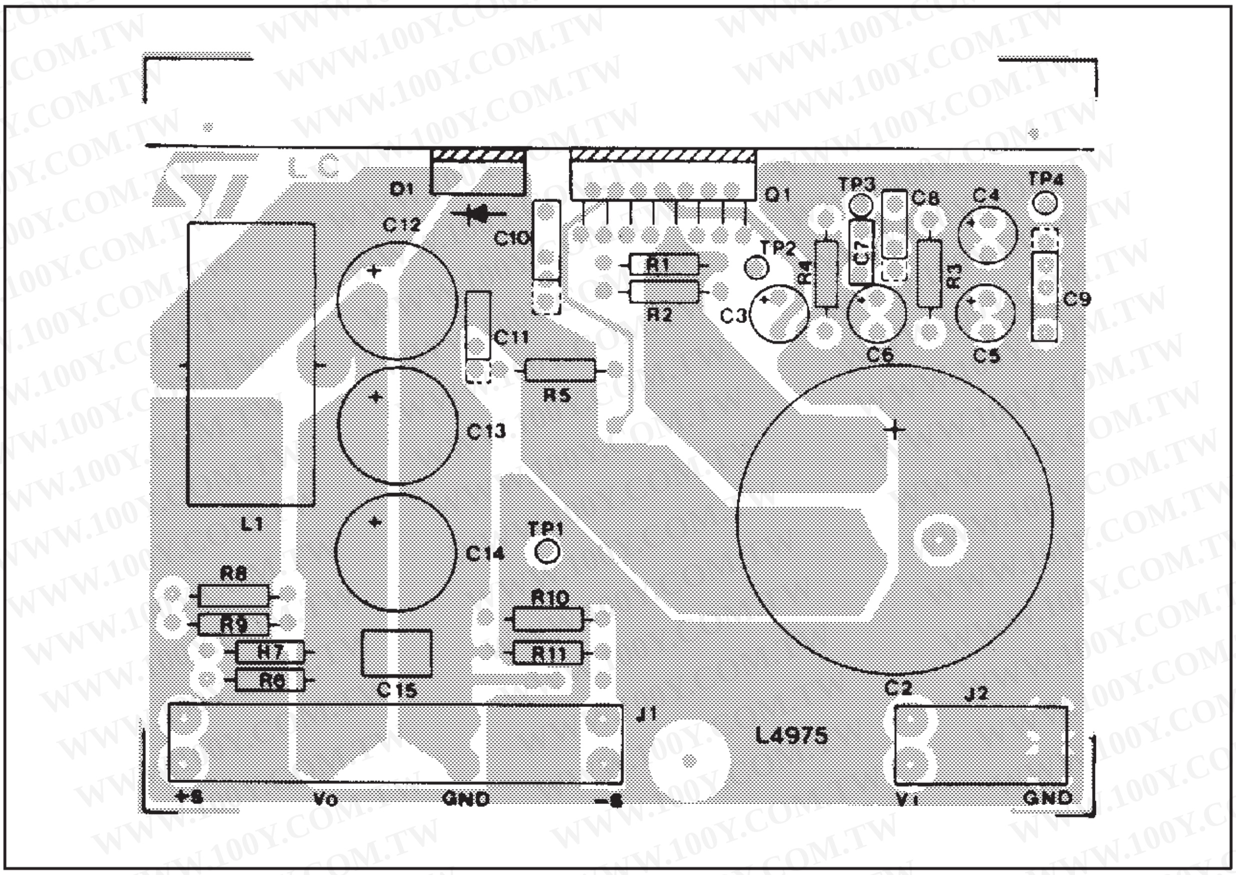
$V_{o\ RIPPLE}$ = 30mV (at 5A) with output filter capacitor ESR ≤ 60mΩ

Line regulation = 5mV (V_i = 15 to 50V)

Load regulation = 15mV (I_o = 2 to 5A)

For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 760CT (or 7.5A/60V or equivalent)	
L1 = 80µH	core 58930 MAGNETICS 24 TURNS Ø 1.1mm (AWG 17) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A

V_0	R_9	R_7
12V	4.7kΩ	6.2kW
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12kΩ
24V	4.7kΩ	18kΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

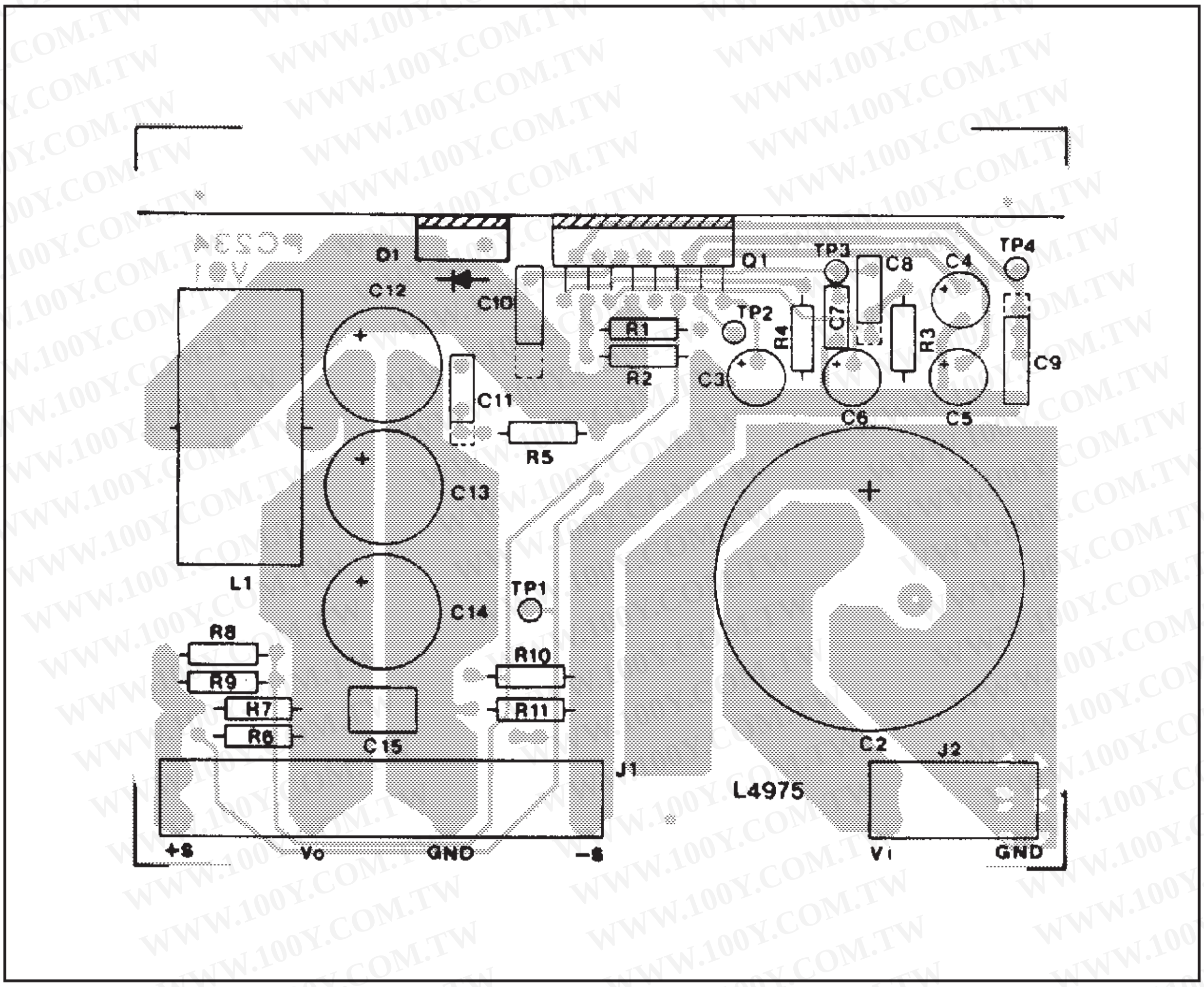


Figure 7: DC Test Circuits

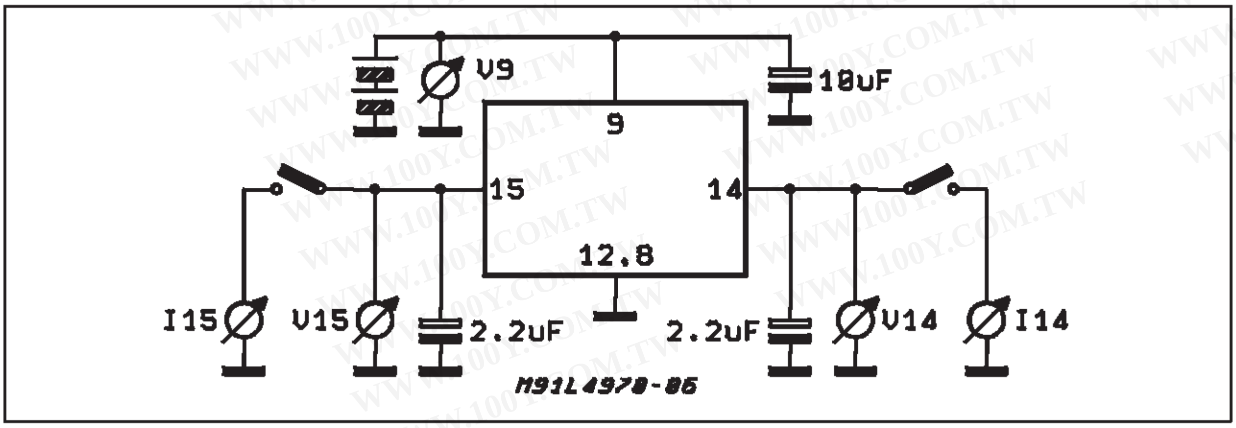


Figure 7A

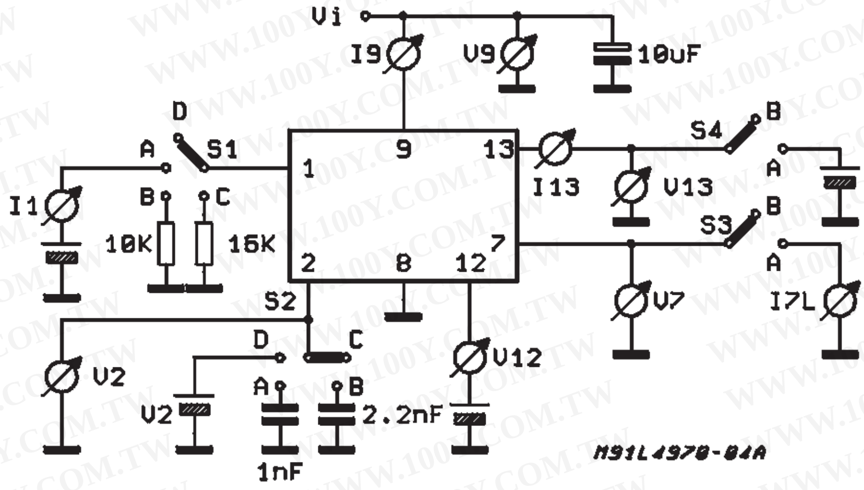


Figure 7B

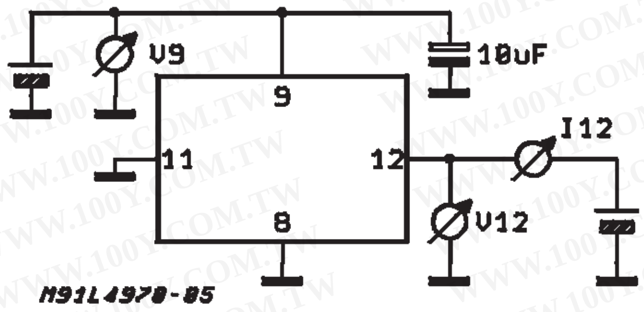


Figure 7D

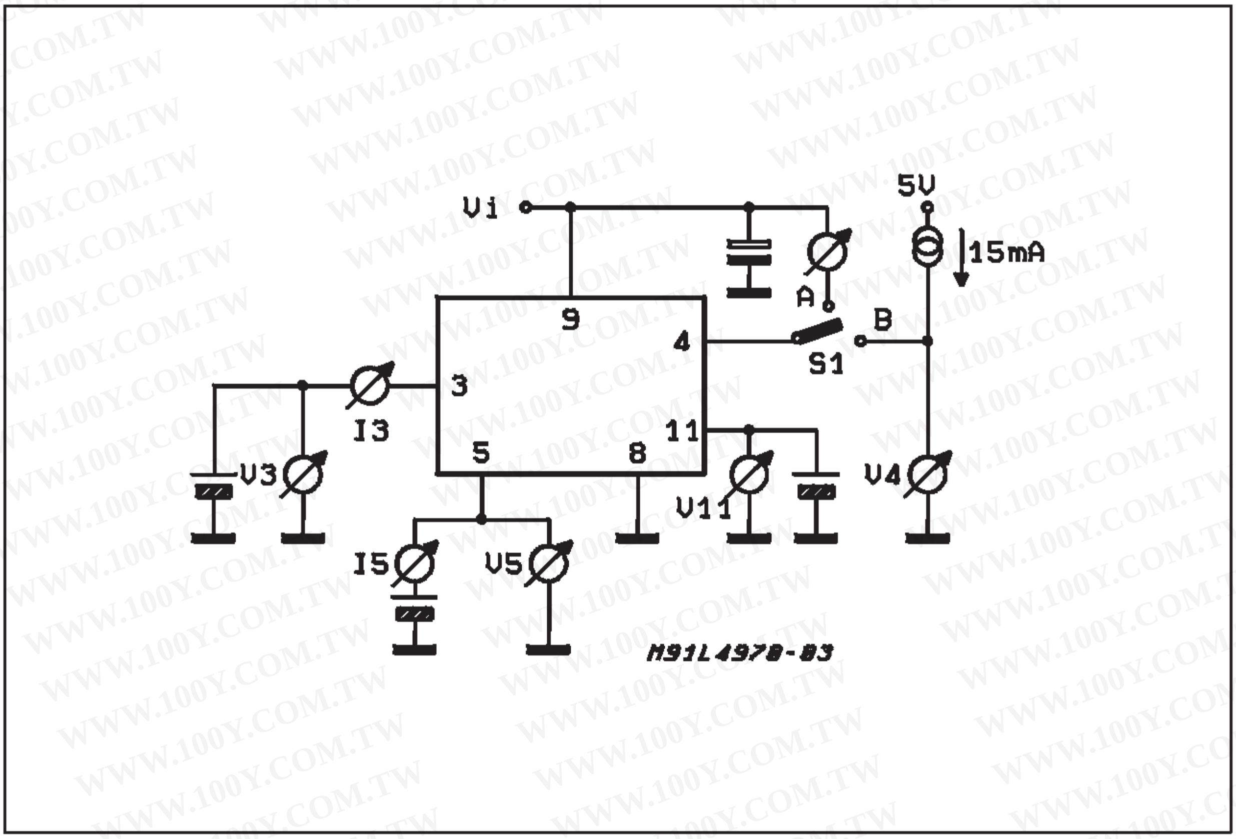
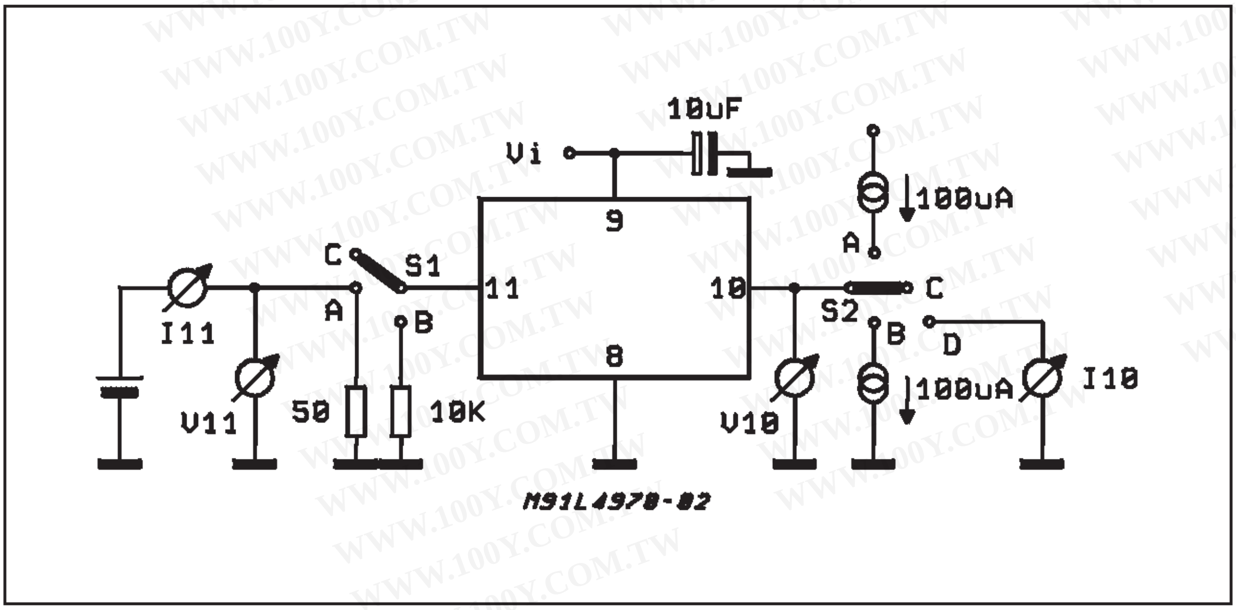


Figure 7C



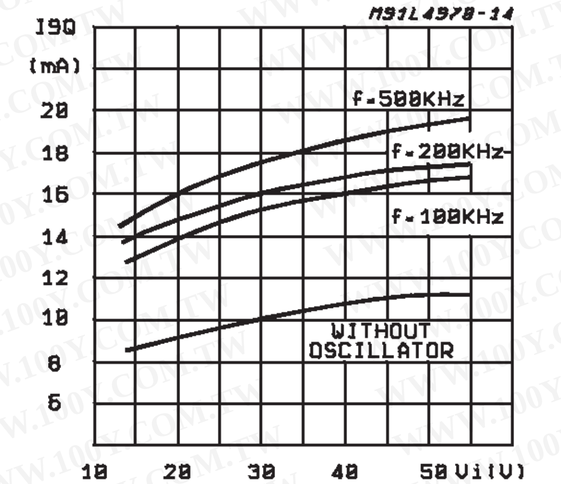


Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

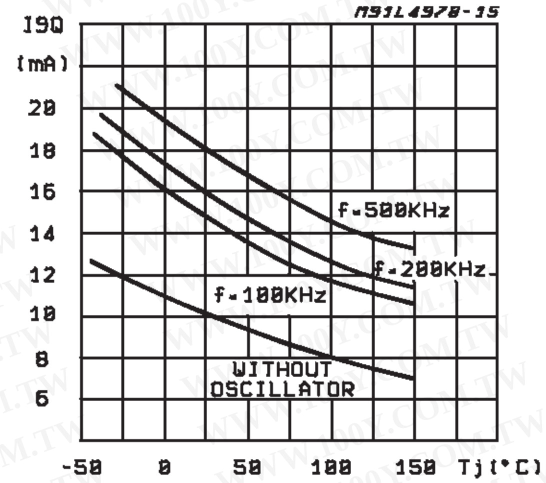


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

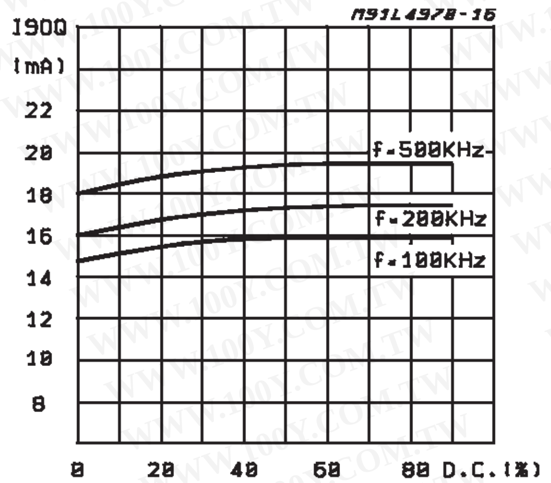


Figure 10: Quiescent Drain Current vs. Duty Cycle

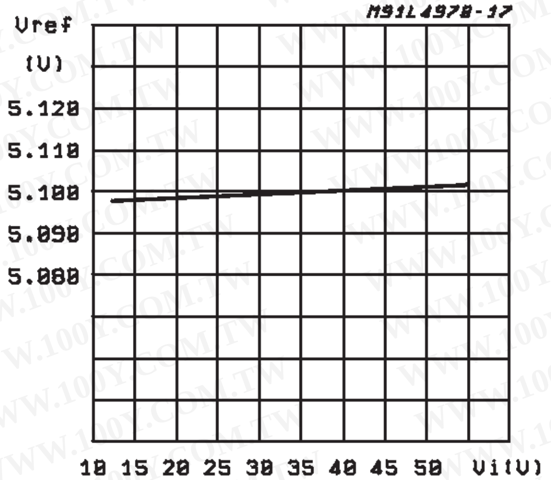


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

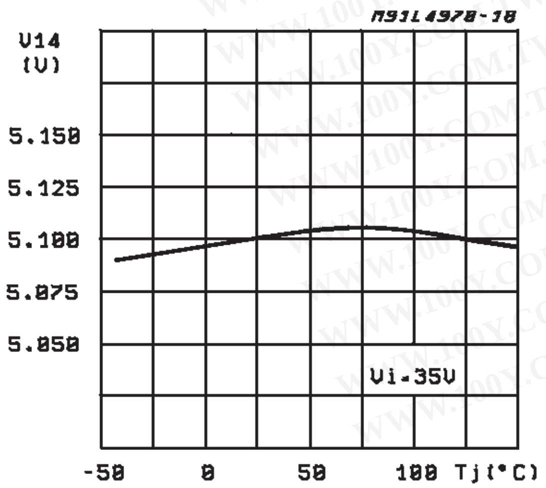


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

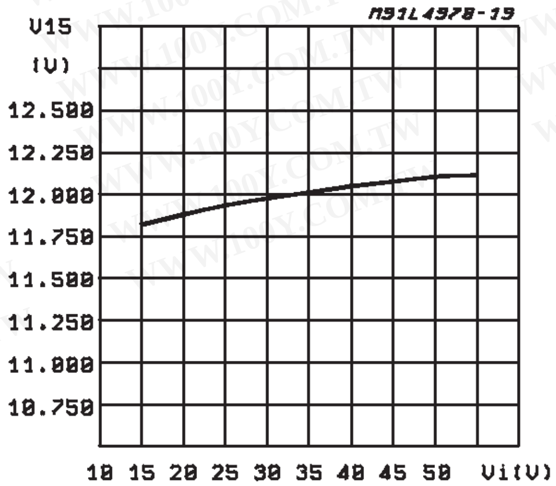


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

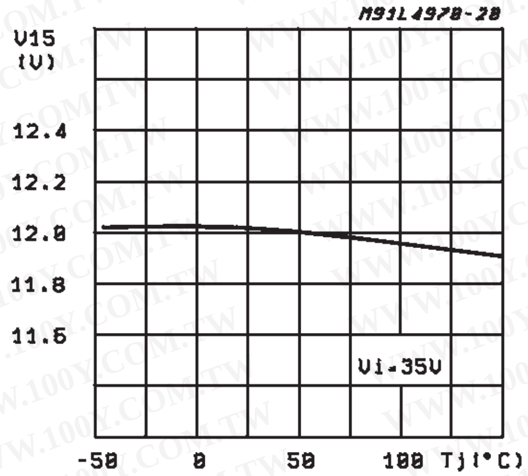


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

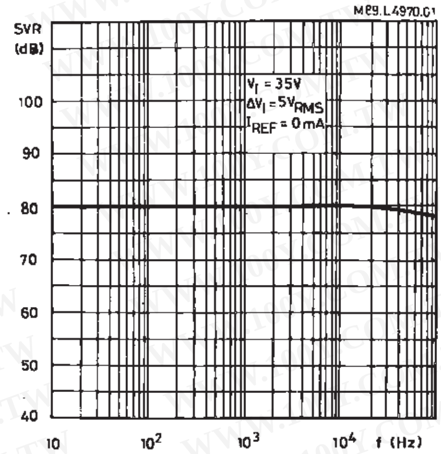


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

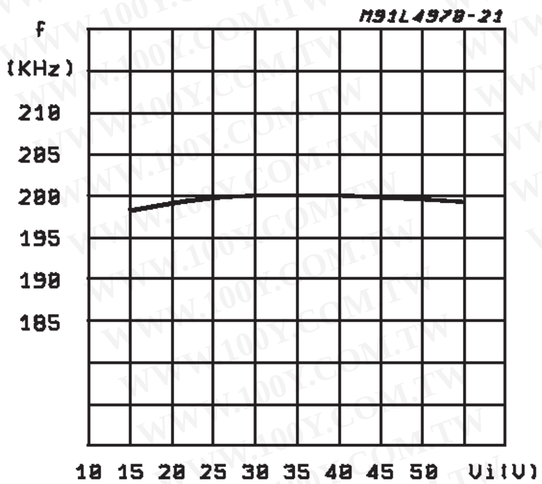


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

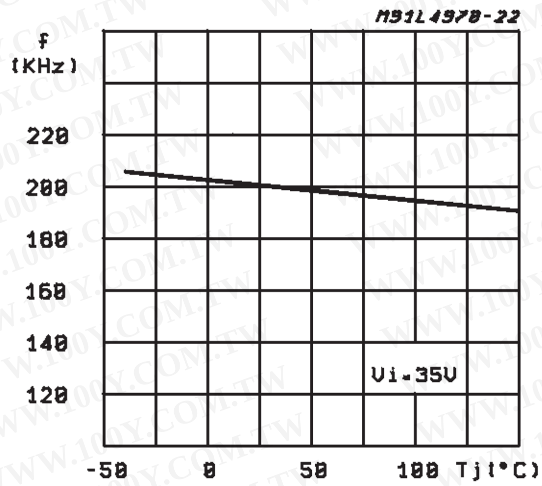


Figure 18: Switching Frequency vs. R4 (see fig. 5)

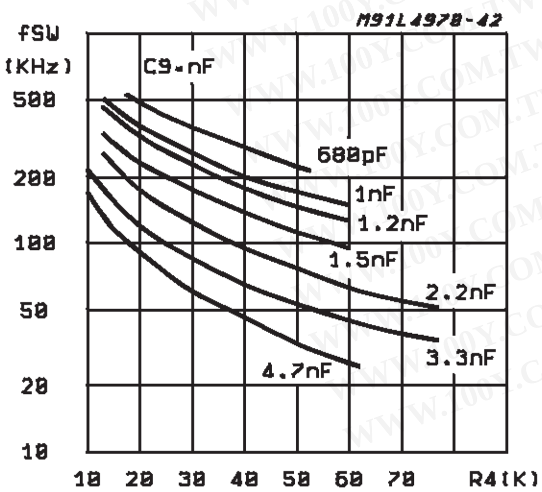


Figure 19: Max. Duty Cycle vs. Frequency

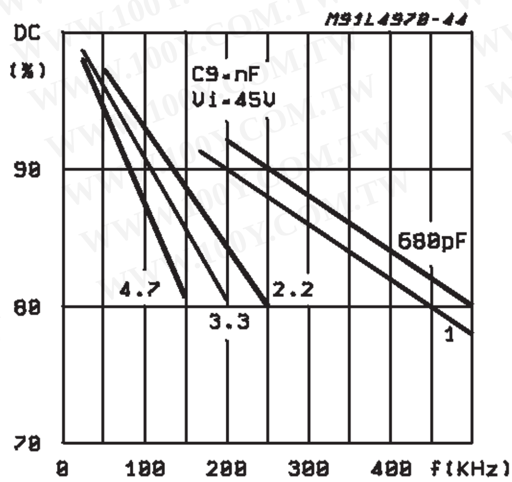


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

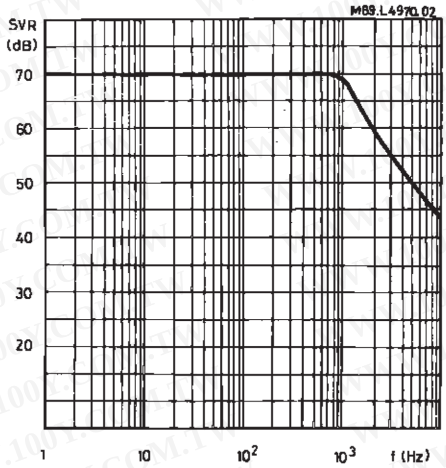


Figure 21: Line Transient Response (see fig. 5)

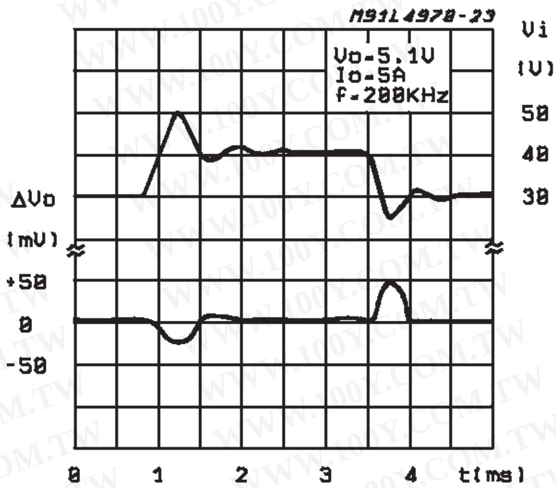


Figure 22: Load Transient Response (see fig. 5)

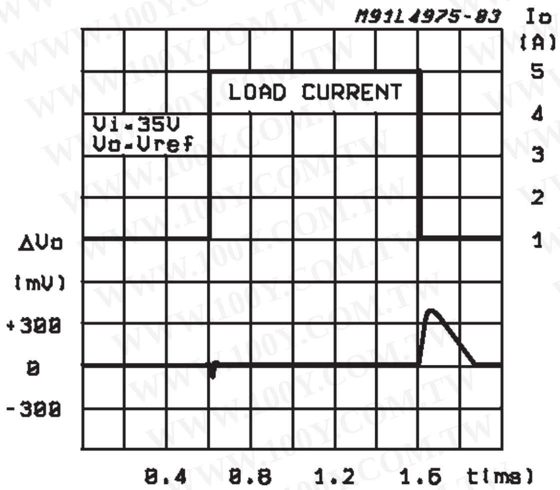


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

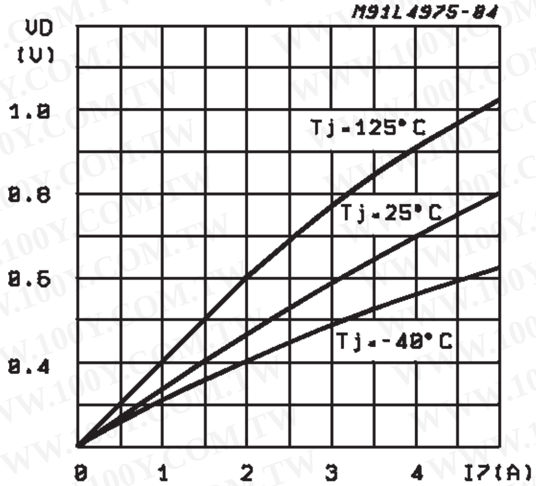


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

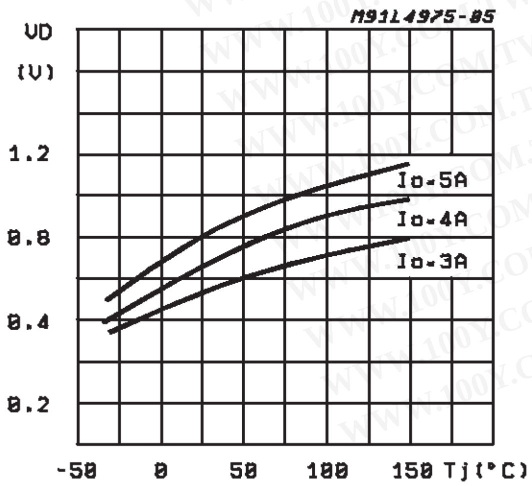


Figure 25: Power Dissipation (device only) vs. Input Voltage

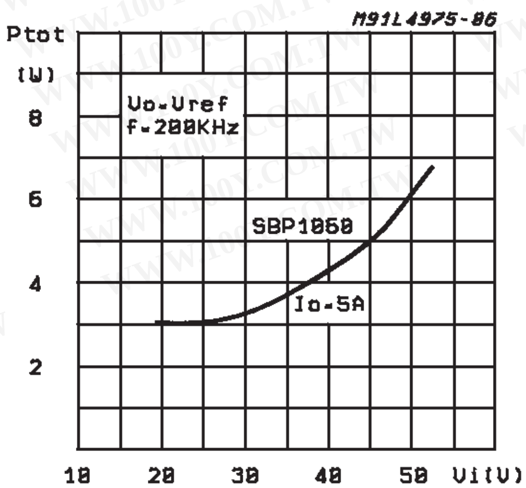


Figure 26: Power Dissipation (device only) vs. Output Voltage

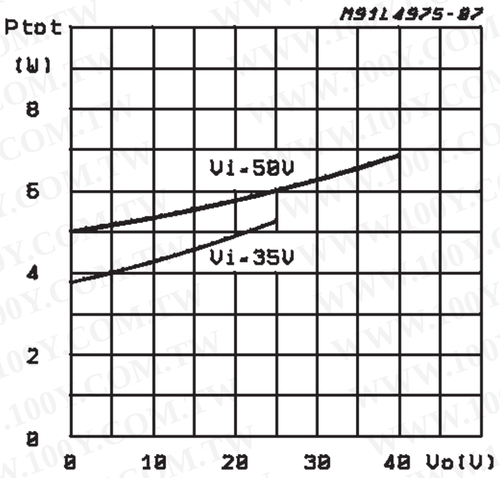


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th} - \text{Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

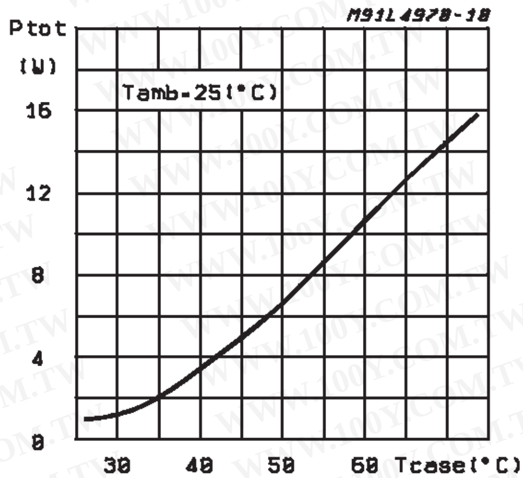


Figure 28: Efficiency vs. Output Current

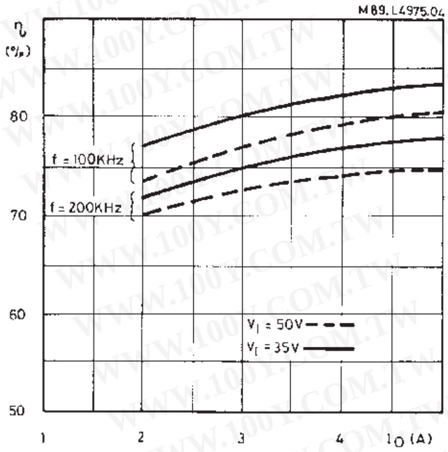


Figure 29: Efficiency vs. Output Voltage

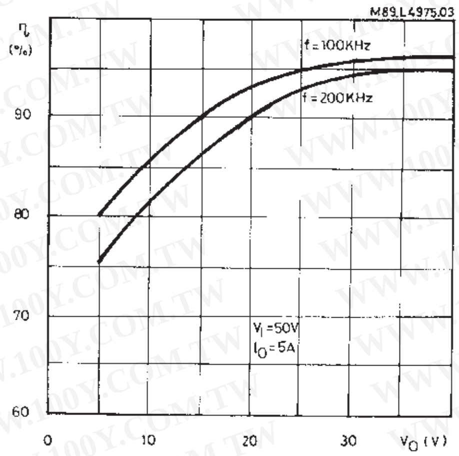


Figure 30: Efficiency vs. Output Voltage

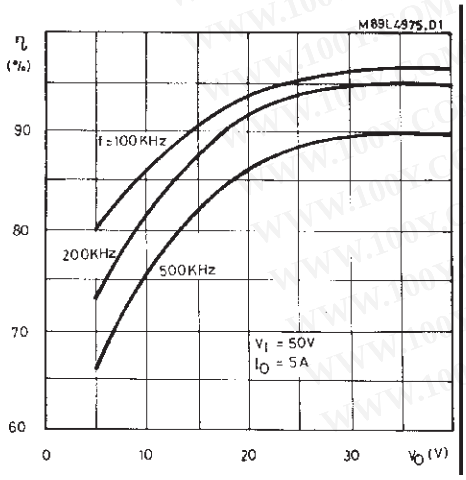


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

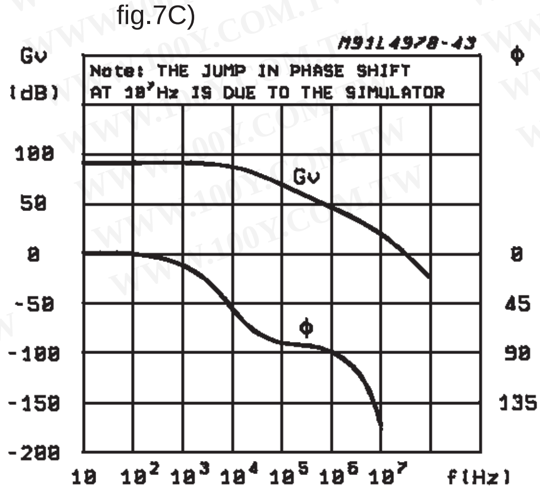


Figure 32: Power Dissipation Derating Curve

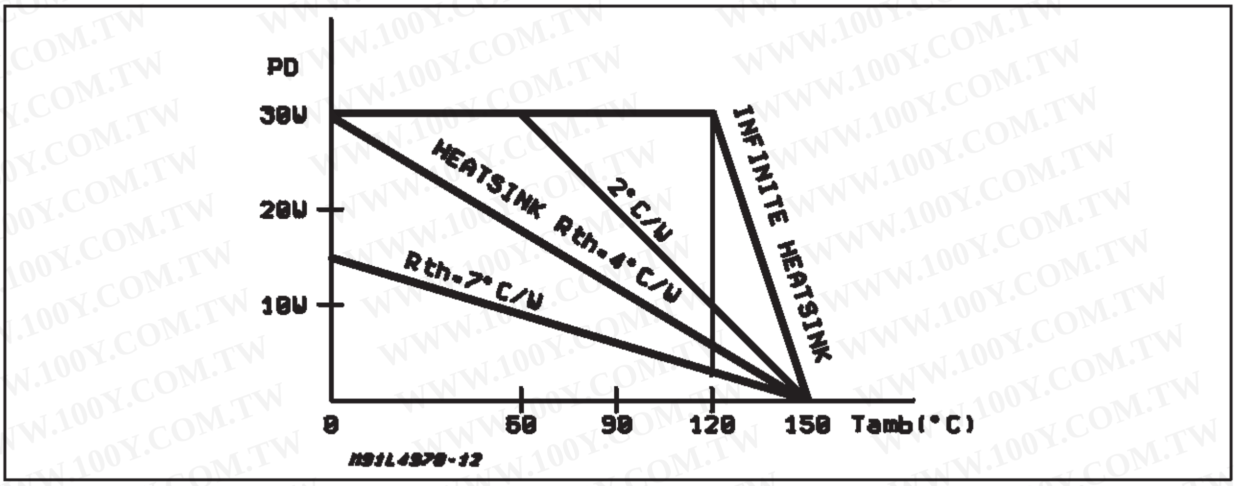


Figure 33: 5.1V/12V Multiple Supply. Note the Synchronization between the L4975A and the L4974A

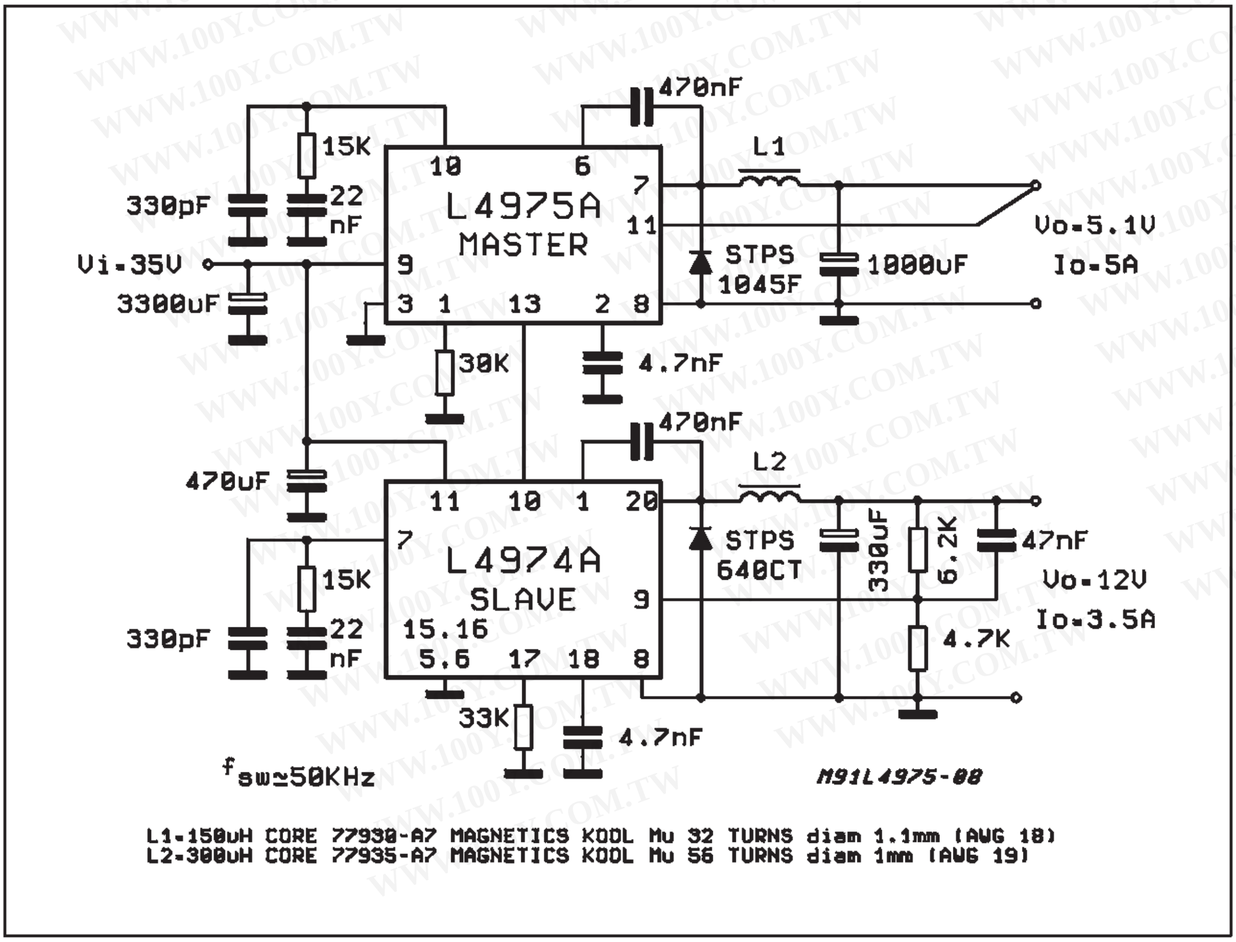


Figure 34: 5.1V / 5A Low Cost Application

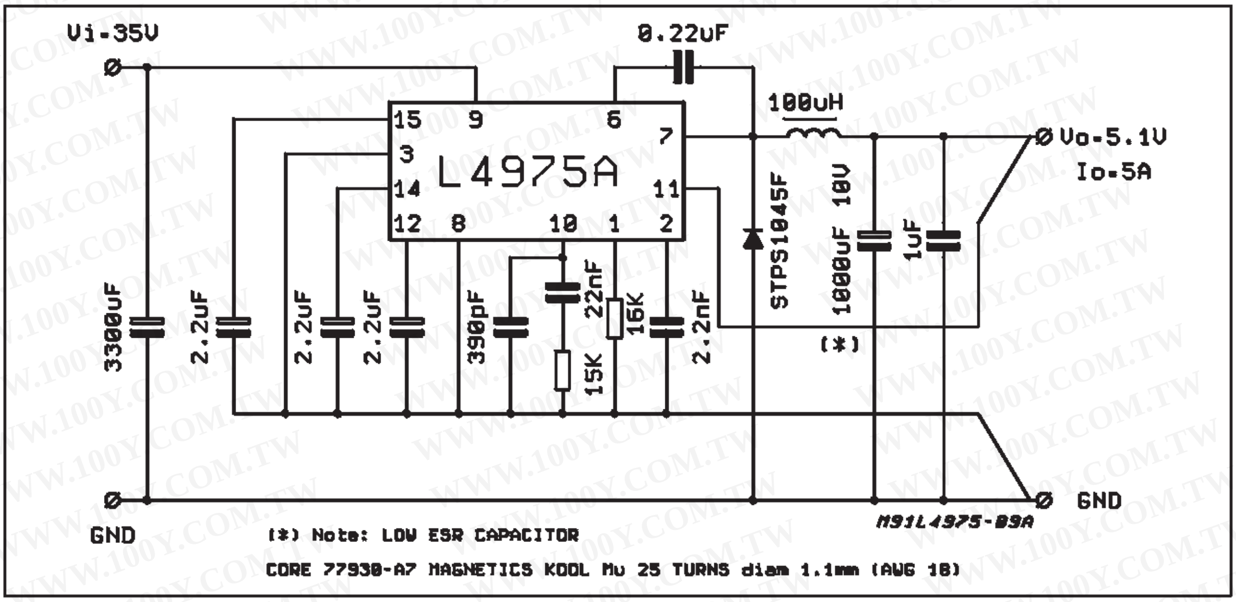


Figure 35: 5A Switching Regulator, Adjustable from 0V to 25V.

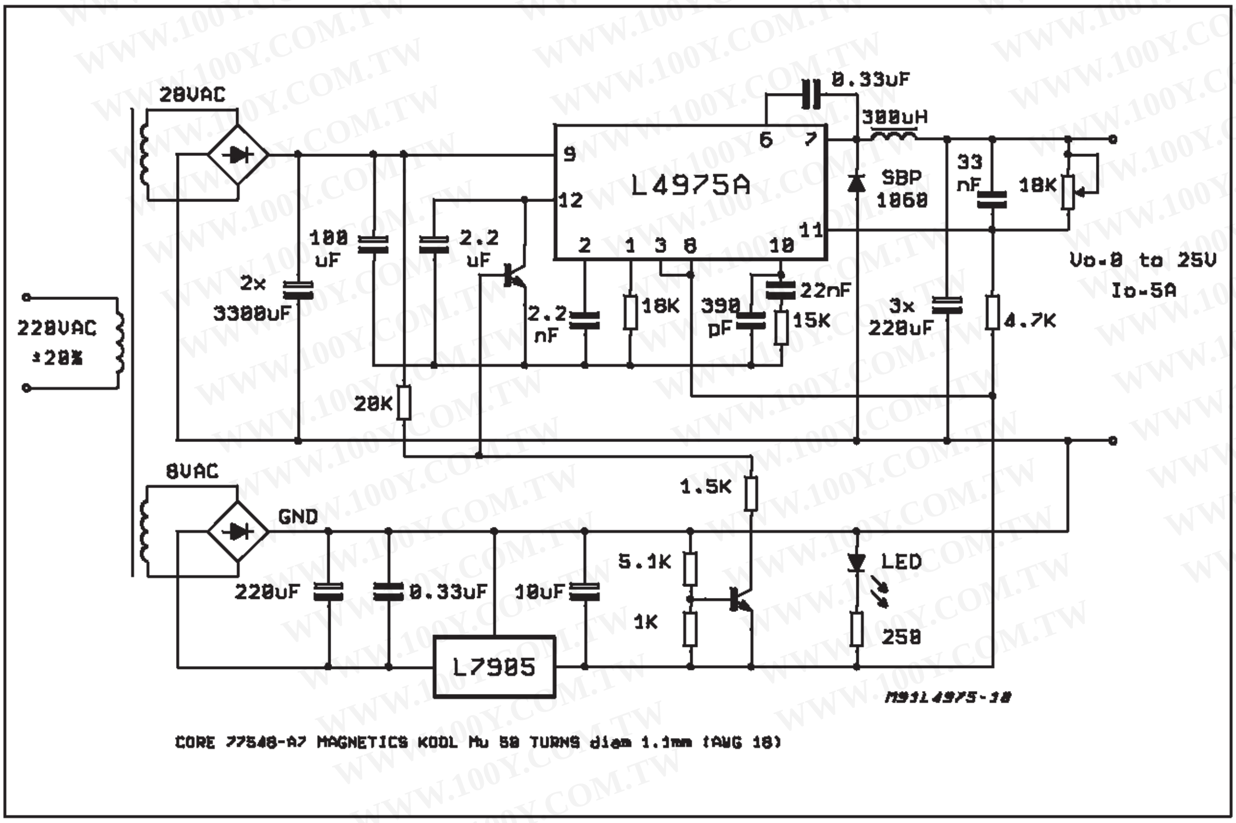
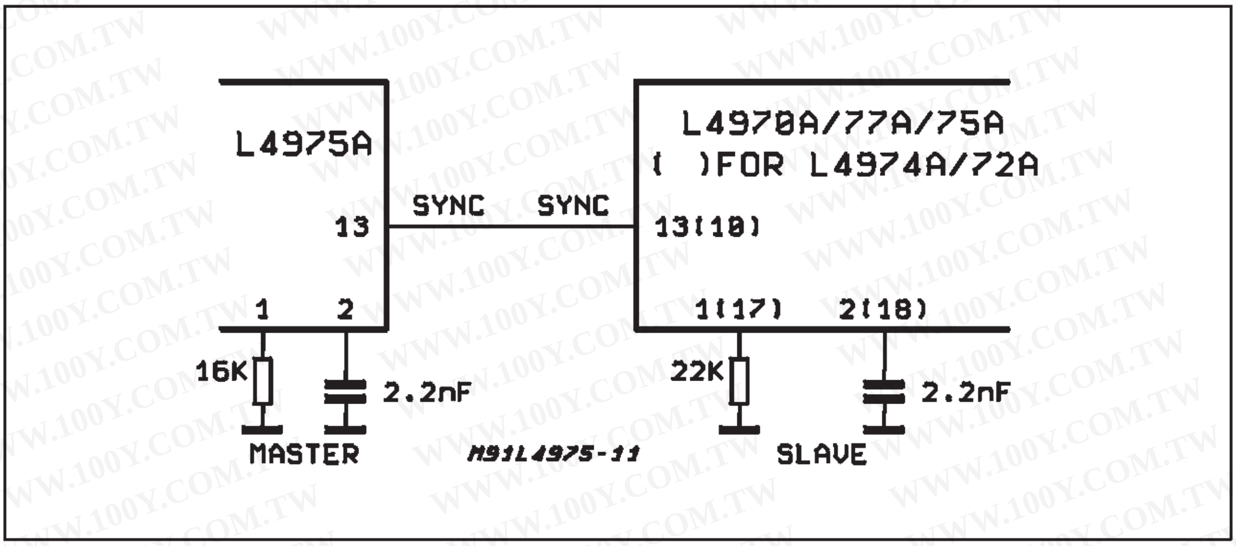
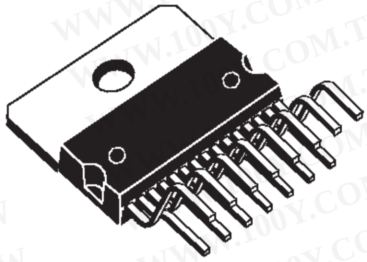


Figure 36: L4975A's Sync. Example



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Multiwatt15 V