

勝特力材料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

LP2950/LP2951 Series of Adjustable Micropower Voltage Regulators General Description (.05% typ.) and a very low output voltage tempera ficient making the part useful as a low-nower volt

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75µA typ.) and very low dropout voltage (typ. 40mV at light loads and 380mV at 100mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950-5.0 is available in the surface-mount D-Pak package, and in the popular 3-pin TO-92 package for pincompatibility with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V, 3V, or 3.3V output (depending on the version), or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation

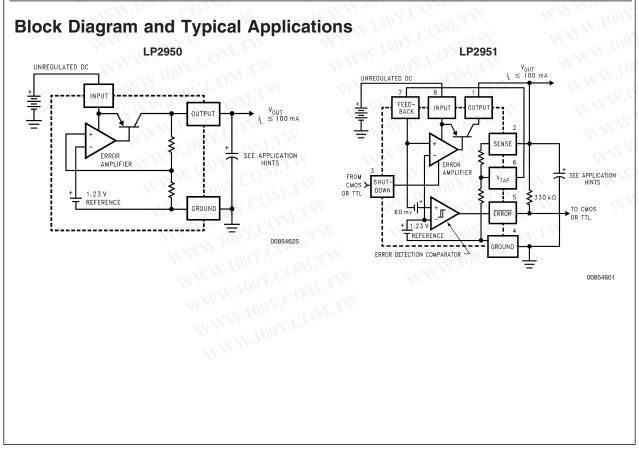
(.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

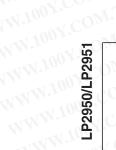
Features

- 5V, 3V, and 3.3V versions available
- High accuracy output voltage
- Guaranteed 100mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs minimum capacitance for stability
- Current and Thermal Limiting
- Stable with low-ESR output capacitors

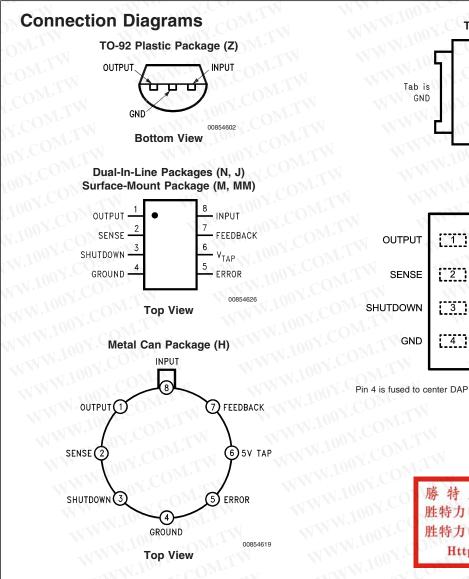
LP2951 versions only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

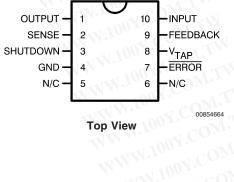




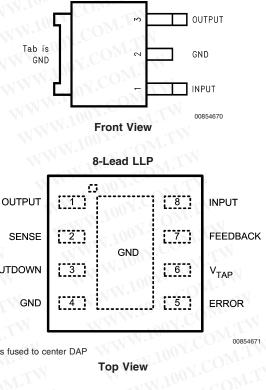
Connection Diagrams



10-Lead Ceramic Surface-Mount Package (WG)







TO-252 (D-Pak)

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Package		tion					
	Temperature Range	Part Number	Package Marking	Transport Media	NSC Drawing		
TO-92 (Z)	$-40 < T_{J} < 125$	LP2950ACZ-3.0	2950A CZ3.0	Bag	Z03A		
N.100	OM. C	LP2950CZ-3.0	2950 CZ3.0	Bag	W		
W.100Y.	COM.TW	LP2950ACZ-3.3	2950A CZ3.3	Bag			
1001	WT.M.	LP2950CZ-3.3	2950 CZ3.3	Bag	1.1.1		
WW.L	V.COM. TW	LP2950ACZ-5.0	2950A CZ5.0	Bag	WILL		
WW.10	COM.	LP2950CZ-5.0	2950 CZ5.0	Bag	WT		
TO-252	–40 < T _J < 125	LP2950CDT-3.0	LP2950CDT-3.0	75 Units/Rail	TD03B		
(D-Pak)	00Y.COM.T	LP2950CDTX-3.0	N.100Y.COM.TW	2.5k Units Tape and Reel	WT.NO		
WW	TOO T COM.	LP2950CDT-3.3	LP2950CDT-3.3	75 Units/Rail	COM		
WWW	1.100X.CON	LP2950CDTX-3.3	WW.1001.COM.IW	2.5k Units Tape and Reel	COM.I		
NT.	W.IV CO	LP2950CDT-5.0	LP2950CDT-5.0	75 Units/Rail	N.COM		
WW	VW.1001.CC	LP2950CDTX-5.0	WWW.1001.COM.T	2.5k Units Tape and Reel	OV.COM		
N (N-08E)	–40 < T _J < 125	LP2951ACN-3.0	LP2951ACN-3.0	40 Units/Rail	N08E		
	WW.IVe	LP2951CN-3.0	LP2951CN-3.0	40 Units/Rail	LONY.CUT		
	W.100 1	LP2951ACN-3.3	LP2951ACN-3.3	40 Units/Rail	.10° × CO		
	WW 1001	LP2951CN-3.3	LP2951CN-3.3	40 Units/Rail	N.100 1.		
	WWW	LP2951ACN	LP2951ACN	40 Units/Rail	1001.0		
	WWW.10	LP2951CN	LP2951CN	40 Units/Rail	V.V.		
M (M08A)	–40 < T _J < 125	LP2951ACM-3.0 LP2951ACMX-3.0	2951ACM30* (where * is die rev letter)	95 Units/Rail 2.5k Units Tape and	M08A		
	WWW.	N.COm	NY9001	Reel	100		
	WW	LP2951CM-3.0	2951CM30*	95 Units/Rail	WWW.		
	WW	LP2951CMX-3.0	(where * is die rev letter)	2.5k Units Tape and Reel	WWW.10		
	WW	LP2951ACM-3.3	2951ACM33*	95 Units/Rail	WWW.1		
	W	LP2951ACMX-3.3	(where * is die rev letter)	2.5k Units Tape and Reel	MMM.		
	1	LP2951CM-3.3	2951CM33*	95 Units/Rail	WW		
		LP2951CMX-3.3	(where * is die rev letter)	2.5k Units Tape and Reel	WW WW		
		LP2951ACM	2951ACM*	95 Units/Rail			
	-	LP2951ACMX	(where * is die rev letter)	2.5k Units Tape and Reel	W W		
		LP2951CM	2951CM*	95 Units/Rail	1		
		LP2951CMX	(where * is die rev letter)	2.5k Units Tape and Reel			

	ing Informa	tion (Continued)			
Package	Temperature Range	Part Number	Package Marking	Transport Media	NSC Drawir
MM	-40 < T _J < 125	LP2951ACMM-3.0	LOBA	1k Units Tape and Reel	MUA08A
(MUA08A)	W W	LP2951ACMMX-3.0		3.5k Units Tape and Reel	
Y.CO.	TN VI	LP2951CMM-3.0	L0BB	1k Units Tape and Reel	
OV.COM	WT.1	LP2951CMMX-3.0		3.5k Units Tape and Reel	
00Y.C	MT.IM	LP2951ACMM-3.3	LOCA	1k Units Tape and Reel	
.100¥.CU	M.TW	LP2951ACMMX-3.3		3.5k Units Tape and Reel	
v.1001.	OM.1	LP2951CMM-3.3	LOCB	1k Units Tape and Reel	
W.100Y.	COM.TW	LP2951CMMX-3.3		3.5k Units Tape and Reel	
VW.100	CONT	LP2951ACMM	LODA	1k Units Tape and Reel	
WW.100	N.COM.TW	LP2951ACMMX	100Y.COM.IV	3.5k Units Tape and Reel	
WWW.L	NV.COM	LP2951CMM	LODB	1k Units Tape and Reel	
WWW.I	100 ^{Y.COM.1}	LP2951CMMX	N.100Y.COM.TW	3.5k Units Tape and Reel	OM.TW
J (J08A)	$-55 < T_{\rm J} < 150$	LP2951J/883	See MIL/AERO Datasheet	40 Units/Rail	J08A
H (H08C)	–55 < T _J < 150	LP2951H/883	See MIL/AERO Datasheet	Tray	H08C
WG (WG10A)	–55 < T _J < 150	LP2951WG/883	See MIL/AERO Datasheet	Tray	WG10A
8-lead	–40 < T _J < 125	LP2951ACLD-3.0	L002A	1k Units Tape and Reel	LDA08A
LLP	WW.100Y.C	LP2951ACLDX-3.0	WWW.100Y.COM	4.5k Units Tape and Reel	
1	1001.	LP2951CLD-3.0	L002B	1k Units Tape and Reel	
	WWW.100Y	LP2951CLDX-3.0	WWWW.100Y.COM	4.5k Units Tape and Reel	
	W	LP2951ACLD-3.3	L003A	1k Units Tape and Reel	
	WWW.10	LP2951ACLDX-3.3	WWW.100X.CC	4.5k Units Tape and Reel	
	L.WW.	LP2951CLD-3.3	L003B	1k Units Tape and Reel	
	WWW	LP2951CLDX-3.3	WWW.1001.	4.5k Units Tape and Reel	
	WIT	LP2951ACLD-5.0	L027A	1k Units Tape and Reel	
	WW	LP2951ACLDX-5.0	LM MMM.100	4.5k Units Tape and Reel	
	W	LP2951CLD-5.0	L027B	1k Units Tape and Reel	
		LP2951CLDX-5.0		4.5k Units Tape and Reel	

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Supply Voltage	-0.3 to +30V
SHUTDOWN Input Voltage,	
Error Comparator Output	
Voltage, (Note 9)	
FEEDBACK Input Voltage	-1.5 to +30V
(Note 9) (Note 10)	
Power Dissipation	Internally Limited
Junction Temperature (T _J)	+150°C
Ambient Storage Temperature	−65° to +150°C
Soldering Dwell Time, Temperati	ure
Wave	4 seconds, 260°C
Infrared	10 seconds, 240°C
Vapor Phase	75 seconds, 219°C

Electrical Characteristics (Note 2)

ESD Rating Human Body Model(Note 18)

2500V

LP2950/LP2951

N.100X.C

Operating Ratings (Note 1)

Maximum Input Supply Voltage	30V
Junction Temperature Range	
(T _J) (Note 8)	
LP2951	-55° to +150°C
LP2950AC-XX, LP2950C-XX,	
LP2951AC-XX, LP2951C-XX	-40° to +125°C

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WWW.	NOX.COM.TW	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			COM
Parameter	Conditions (Note 2)	Тур	Tested Limit (Notes 3, 16)	Тур	Tested Limit (Note 3)	Design Limit (Note 4)	Тур	Tested Limit (Note 3)	Design Limit (Note 4)	Units
3V Versions (Note 17	W.L. COMP	N	WW	N	N.CU	VT.		W		NY.C
Output Voltage	$T_J = 25^{\circ}C$	3.0	3.015 2.985	3.0	3.015 2.985	ONL.	3.0	3.030 2.970	WW.	V max V min
	–25°C ≤ T _J ≤ 85°C	3.0	W	3.0	.100X.	3.030 2.970	3.0		3.045 2.955	V max V min
	Full Operating Temperature Range	3.0	3.036 2.964	3.0	N.100	3.036 2.964	3.0	N	3.060 2.940	V max V min
Output Voltage	$100\mu A \le I_L \le 100mA$ $T_J \le T_{JMAX}$	3.0	3.045 2.955	3.0	NN.10	3.042 2.958	3.0	N N	3.072 2.928	V max V min
3.3V Versions (Note		CON		- 14	W.	00	OM			Win
Output Voltage	$T_J = 25^{\circ}C$	3.3	3.317 3.284	3.3	3.317 3.284	1001.	3.3	3.333 3.267		V max V min
	$-25^{\circ}C \le T_{J} \le 85^{\circ}C$	3.3	MI.TW	3.3	WWV	3.333 3.267	3.3	M.TW	3.350 3.251	V max V min
	Full Operating Temperature Range	3.3	3.340 3.260	3.3	NN.	3.340 3.260	3.3	OM.T	3.366 3.234	V max V min
Output Voltage	$100\mu A \le I_L \le 100mA$ $T_J \le T_{JMAX}$	3.3	3.350 3.251	3.3	N	3.346 3.254	3.3	COM.	3.379 3.221	V max V min
5V Versions (Note 17		100	Y.CO.A.T	N	1	NN II	100	1.00	11	
Output Voltage	$T_J = 25^{\circ}C$	5.0	5.025 4.975	5.0	5.025 4.975	Maria	5.0	5.05 4.95		V max V min
	–25°C ≤ T _J ≤ 85°C	5.0	001.CON	5.0		5.05 4.95	5.0		5.075 4.925	V max V min
	Full Operating Temperature Range	5.0	5.06 4.94	5.0		5.06 4.94	5.0		5.1 4.9	V max V min
Output Voltage	$100\mu A \le I_L \le 100mA$ $T_J \le T_{JMAX}$	5.0	5.075 4.925	5.0		5.075 4.925	5.0		5.12 4.88	V max V min

Electrical Ch	naracteristics (No	ote 2)	(Continued)	NWV	1.100X.	COM	LM			
	WWW.100 L.CO		LP2951		LP2950A			LP2950C		
Parameter	Conditions (Note 2)	Тур	Tested Limit (Notes 3, 16)	Тур	Tested Limit	Design Limit (Note 4)	Тур	Tested Limit	Design Limit (Note 4)	Unit
All Voltage Options	WW 100Y		WT.L		A A A A A A A A A A A A A A A A A A A	100%.	-01	V.T.M		
Output Voltage Temperature Coefficient	(Note 12)	20	120	20	MM	100	50	M.TW	150	ppm/
Line Regulation (Note 14)	$(V_ONOM + 1)V \le V_{in} \le$ 30V (Note 15)	0.03	0.1 0.5	0.03	0.1	0.2	0.04	0.2	0.4	% ma
Load Regulation (Note 14)	$100\mu A \le I_L \le 100m A$	0.04	0.1 0.3	0.04	0.1	0.2	0.1	0.2	0.3	% ma % ma
Dropout Voltage (Note 5)	I _L = 100μA	50	80 150	50	80 <	150	50	80	150	mV m mV m
	I _L = 100mA	380	450 600	380	450	600	380	450	600	mV m mV m
Ground Current	I _L = 100μA	75	120 140	75	120	140	75	120	140	μA ma μA ma
	I _L = 100mA	8	12 14	8	12	14	8	12	14	mA m mA m
Dropout Ground Current	$V_{in} = (V_O NOM - 0.5)V$ $I_L = 100 \mu A$	110	170 200	110	170	200	110	170	200	μA m μA m
Current Limit	V _{out} = 0	160	200 220	160	200	220	160	200	220	mA m mA m
Thermal Regulation	(Note 13)	0.05	0.2	0.05	0.2	N	0.05	0.2	. MAY.	%/W m
Output Noise,	$C_{L} = 1\mu F$ (5V Only)	430	. WW.10	430	-O _N ,		430	WW	, Los	µV m
10 Hz to 100 kHz	$C_{L} = 200 \mu F$ $C_{L} = 3.3 \mu F$	160	MMM'I	160	.coM	NT	160	NW	1.100	µV m
	(Bypass = 0.01µF Pins 7 to 1 (LP2951)	100	WWW.	100	V.COM	M.TW	100	WW	VW.10	µV m
8-pin Versions Only	NI 100Y. COM.T	NN NN	LP2951	N 10	LP2951A	C-XX		LP2951C	-XX	10
Reference Voltage	WW.100Y.COM.T	1.235	1.25 1.26 1.22	1.235	1.25 1.22	1.26	1.235	1.26 1.21	1.27	V ma V ma V mi
Reference	(Note 7)	TT.	1.2 1.27	NV.	1.100	1.2 1.27	11		1.2 1.285	V mi V ma
Voltage Feedback Pin	WWW.100Y.CO	20	1.19 40	20	40	1.19	20	40	1.185	V mi nA m
Bias Current Reference Voltage	(Note 12)	20	60	20	WW.1	60	50		60	nA ma
Temperature Coefficient	WWW.100Y	.co	M.T.W		NMM.					
Feedback Pin Bias Current Temperature Coefficient	WWW.100	0.1	DM.TW	0.1			0.1			nA/°(
Error Comparator	dis.									
Output Leakage Current	V _{OH} = 30V	0.01	1 2	0.01	1	2	0.01	1	2	μA ma μA ma
Output Low Voltage	$V_{in} = (V_O NOM - 0.5)V$ $I_{OL} = 400 \mu A$	150	250 400	150	250	<u>40</u> 0	150	250	400	mV m mV m

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CONTRACT	naracteristics (No	ote 2)	(Continued)	1	WW	1.10	J.CC	Disr.	N	
Parameter	WWW.10	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			
	Conditions (Note 2)	Тур	Tested Limit (Notes 3, 16)	Тур	Tested Limit (Note 3)	Design Limit (Note 4)	Тур	Tested Limit (Note 3)	Design Limit (Note 4)	Units
Error Comparator	WW WY	-10	DY.C.	L.M.	-	W.	1100	1.0	N.T.V	
Upper Threshold Voltage	(Note 6)	60	40 25	60	40	25	60	40	25	mV mir mV mir
Lower Threshold Voltage	(Note 6)	75	95 140	75	95	140	75	95	140	mV max mV max
Hysteresis	(Note 6)	15	00.VCC	15	W	N	15	You	COm	mV
Shutdown Input	COM.1		W.100	ON			IN	N.100	1 COM	- N
Input Logic Voltage	Low (Regulator ON) High (Regulator OFF)	1.3	0.6 2.0	1.3	N.TW	0.7 2.0	1.3	W.100	0.7 2.0	V V max V min
Shutdown Pin Input Current	V _{shutdown} = 2.4V	30	50 100	30	50	N 100	30	50	100	μΑ max μΑ max
	V _{shutdown} = 30V	450	600 750	450	600	750	450	600	750	μA max μA max
Regulator Output Current in Shutdown	(Note 11)	3	10 20	3	10	20	3	10	20	μA max μA max

LP2950/LP295

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: Unless otherwise specified all limits guaranteed for V_{IN} = (V_{ONOM} + 1)V, I_L = 100µA and C_L = 1µF for 5V versions and 2.2µF for 3V and 3.3V versions. Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for T_A = T_J = 25°C. Additional conditions for the 8-pin versions are FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE, and V_{SHUTDOWN} \leq 0.8V.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at V_{in} = (V₀NOM + 1)V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{out}/V_{ref} = (R1 + R2)/R2.For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95mV x 5V/1.235V = 384 mV. Thresholds remain constant as a percent of Vout as Vout is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: $V_{ref} \leq V_{out} \leq (V_{in} - 1V), 2.3V \leq V_{in} \leq 30V, 100\mu A \leq I_L \leq 100mA, T_J \leq T_{JMAX}.$

Note 8: The junction-to-ambient thermal resistances are as follows: 180°C/W and 160°C/W for the TO-92 package with 0.40 inch and 0.25 inch leads to the printed circuit board (PCB) respectively, 105°C/W for the molded plastic DIP (N), 130°C/W for the ceramic DIP (J), 160°C/W for the molded plastic SOP (M), 200°C/W for the molded plastic MSOP (MM), and 160°C/W for the metal can package (H). The above thermal resistances for the N, J, M, and MM packages apply when the package is soldered directly to the PCB. Junction-to-case thermal resistance for the H package is 20°C/W. Junction-to-case thermal resistance for the TO-252 package is 5.4°C/W. The value of θ_{JA} for the LLP package is typically 51°C/W but is dependent on the PCB trace area, trace material, and the number of layers and thermal vias. For details of thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187.

Note 9: May exceed input supply voltage.

Note 10: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 11: $V_{shutdown} \ge 2V$, $V_{in} \le 30V$, $V_{out} = 0$, Feedback pin tied to V_{TAP} .

Note 12: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 13: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10ms.

Note 14: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

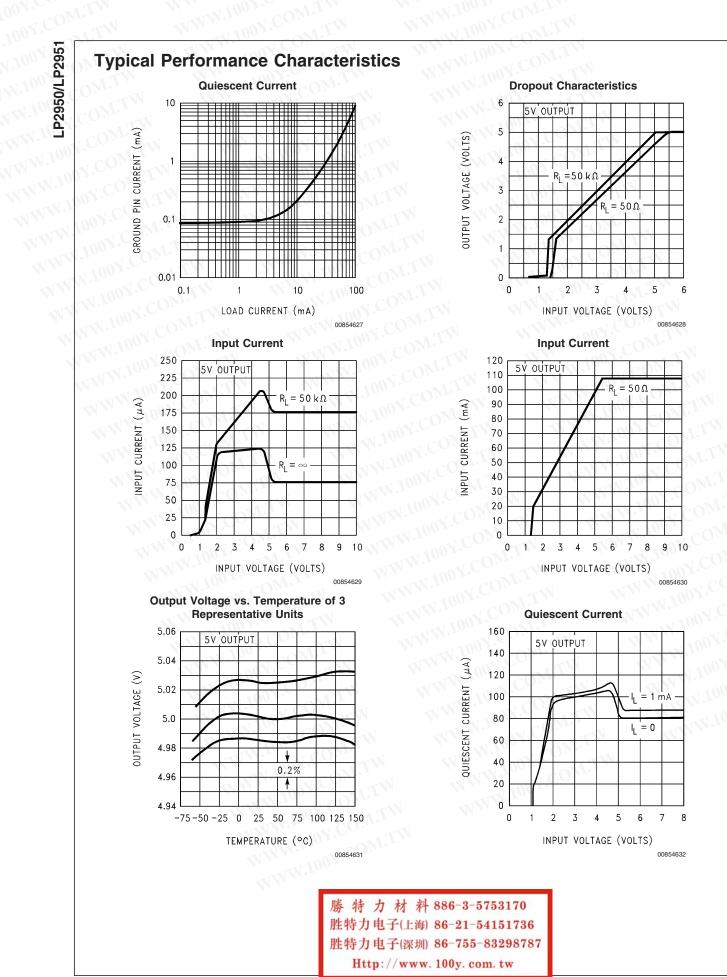
Note 15: Line regulation for the LP2951 is tested at 150°C for I_L = 1mA. For I_L = 100µA and T_J = 125°C, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

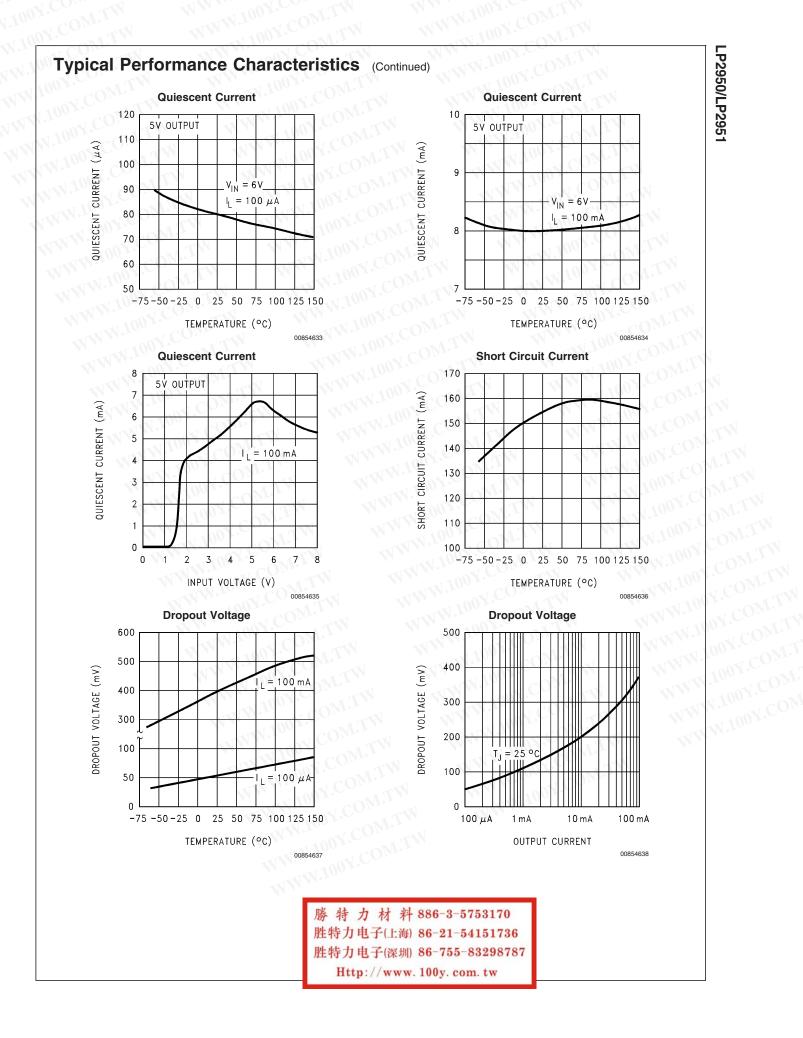
Note 16: A Military RETS specification is available on request. At time of printing, the LP2951 RETS specification complied with the boldface limits in this column. The LP2951H, WG, or J may also be procured as Standard Military Drawing Spec #5962-3870501MGA, MXA, or MPA.

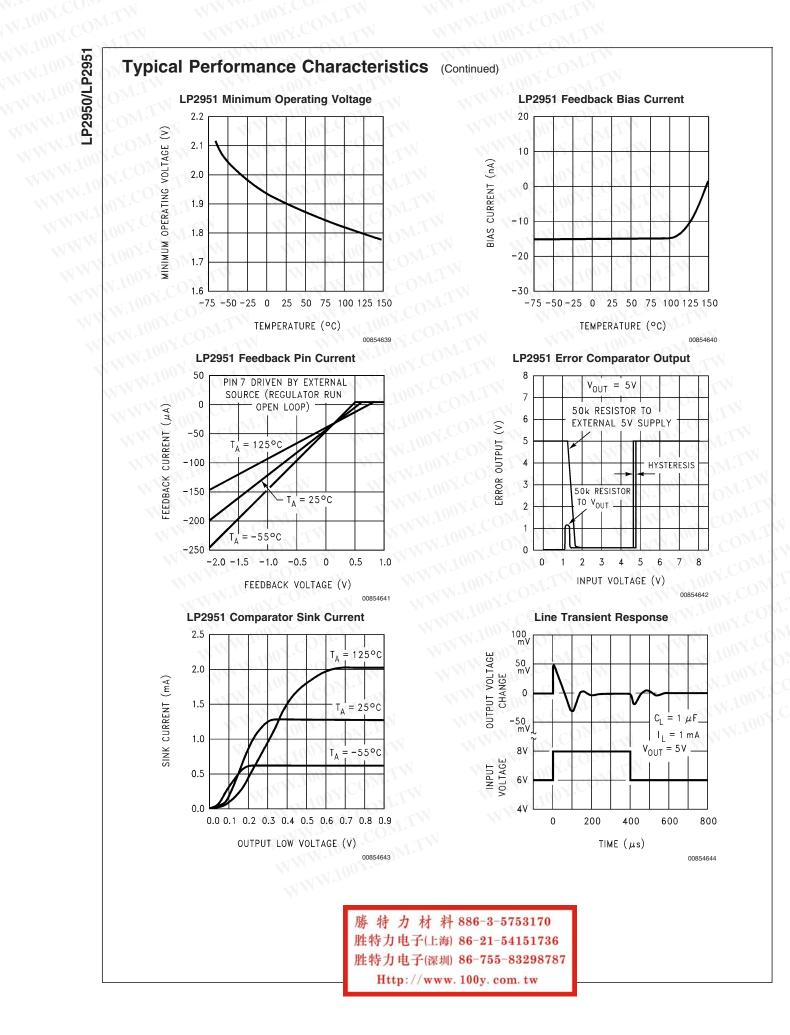
Note 17: All LP2950 devices have the nominal output voltage coded as the last two digits of the part number. In the LP2951 products, the 3.0V and 3.3V versions are designated by the last two digits, but the 5V version is denoted with no code at this location of the part number (refer to ordering information table). Note 18: Human Body Model 1.5kΩ in series with 100pF.

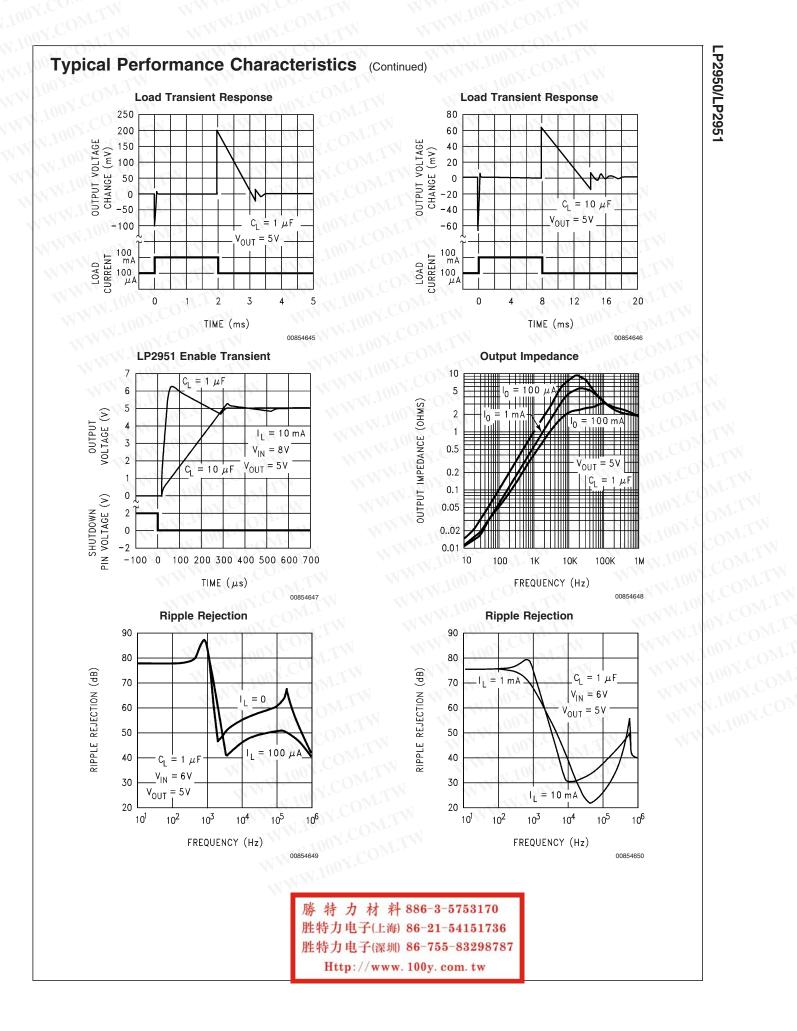


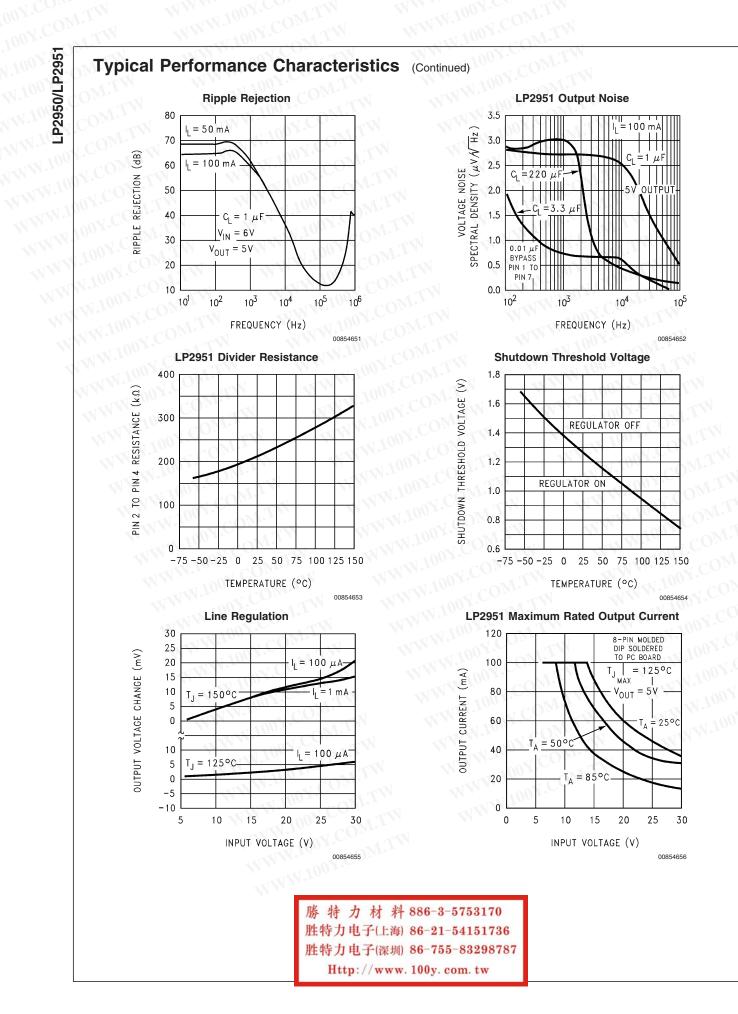


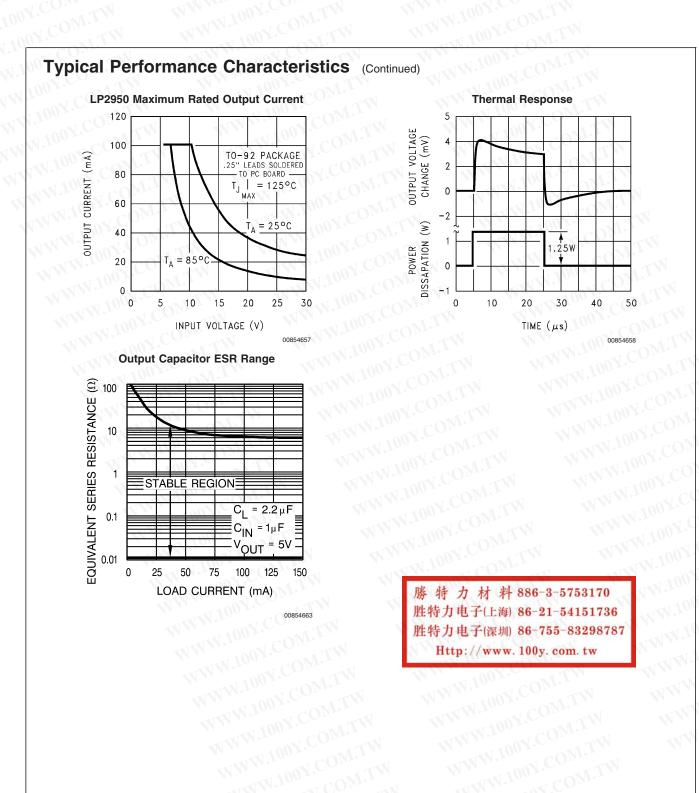












LP2950/LP295

V.TW

OY.COM.TW

LOOX.COM.TV

W.100Y.COM

WWW.100Y.COM.T

WWW.100Y.COM.

50

WWW.100Y.C

WW.109

VWW.1

WW

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Application Hints

EXTERNAL CAPACITORS

A 1.0 μ F (or greater) capacitor is required between the output and ground for stability at output voltages of 5V or more. At lower output voltages, more capacitance is required (2.2 μ F or more is recommended for 3V and 3.3V versions). Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about -30°C, so solid tantalums are recommended for operation below -25°C. The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

Ceramic capacitors whose value is greater than 1000pF should not be connected directly from the LP2951 output to ground. Ceramic capacitors typically have ESR values in the range of 5 to $10m\Omega$, a value below the lower limit for stable operation (see curve Output Capacitor ESR Range).

The reason for the lower ESR limit is that the loop compensation of the part relies on the ESR of the output capacitor to provide the zero that gives added phase lead. The ESR of ceramic capacitors is so low that this phase lead does not occur, significantly reducing phase margin. A ceramic output capacitor can be used if a series resistance is added (recommended value of resistance about 0.1Ω to 2Ω).

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33μ F for currents below 10mA or 0.1μ F for currents below 1mA. Using the adjustable versions at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100mA load at 1.23V output (Output shorted to Feedback) a 3.3μ F (or greater) capacitor should be used.

Unlike many other regulators, the LP2950 will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951 versions with external resistors, a minimum load of 1 μ A is recommended.

A 1 μ F tantalum, ceramic or aluminum electrolytic capacitor should be placed from the LP2950/LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the LP2951 Feedback terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3μ F will fix this problem.

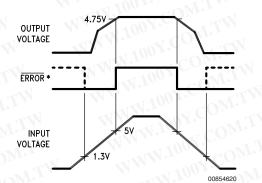
ERROR DETECTION COMPARATOR OUTPUT

The comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60mV divided by the 1.235 reference voltage. (Refer to the block diagram in the front of the datasheet.) This trip level remains "5% below normal" regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

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Figure 1 below gives a timing diagram depicting the ERROR signal and the regulated output voltage as the LP2951 input is ramped up and down. For 5V versions, the ERROR signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which $V_{OUT} = 4.75V$). Since the LP2951's dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 μ A, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 M Ω . The resistor is not required if this output is unused.



*When V_{IN} \leq 1.3V, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see *Figure 2*), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10k Ω suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

FIGURE 1. ERROR Output Timing

PROGRAMMING THE OUTPUT VOLTAGE (LP2951)

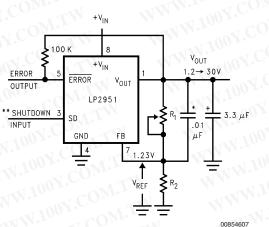
The LP2951 may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying the output and sense pins together, and also tying the feedback and V_{TAP} pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in *Figure 2*, an external pair of resistors is required.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally –20nA. The minimum recommended load current of 1µA forces an upper limit of 1.2 MΩ on the value of R₂, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R₁. For better accuracy, choosing R₂ = 100k reduces this error to 0.17% while increasing the resistor program current to 12µA. Since the LP2951 typically draws 60µA at no load with Pin 2 opencircuited, this is a small price to pay.

Application Hints (Continued)



*See Application Hints

$$V_{out} = V_{Ref} \left(1 + \frac{R_1}{R_2} \right)$$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

FIGURE 2. Adjustable Regulator

Typical Applications

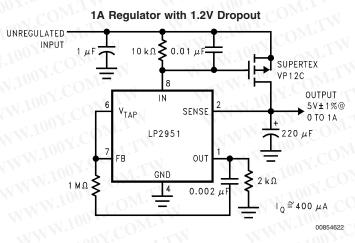


In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP2950 but is relatively inefficient, as increasing the capacitor from 1µF to 220µF only decreases the noise from 430µV to 160µV rms for a 100kHz bandwidth at 5V output. Noise can be reduced fourfold by a bypass capacitor across R₁, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200 \text{ Hz}}$$

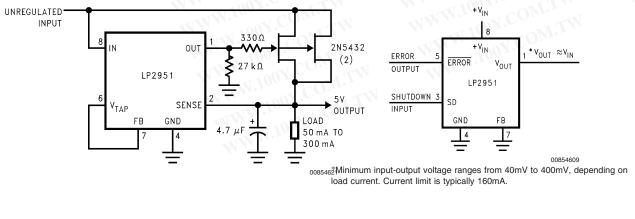
or about 0.01 μ F. When doing this, the output capacitor must be increased to 3.3 μ F to maintain stability. These changes reduce the output noise from 430 μ V to 100 μ V rms for a 100kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

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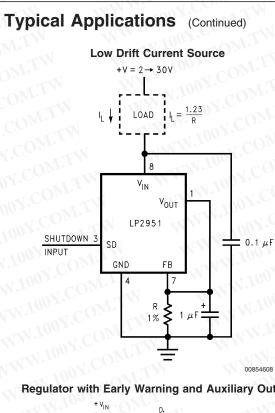


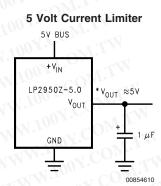
300mA Regulator with 0.75V Dropout





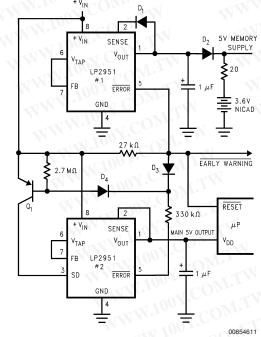






*Minimum input-output voltage ranges from 40mV to 400mV, depending on load current. Current limit is typically 160mA.

Regulator with Early Warning and Auxiliary Output

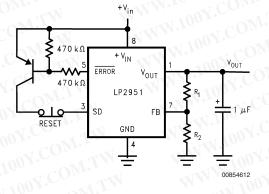


Early warning flag on low input voltage

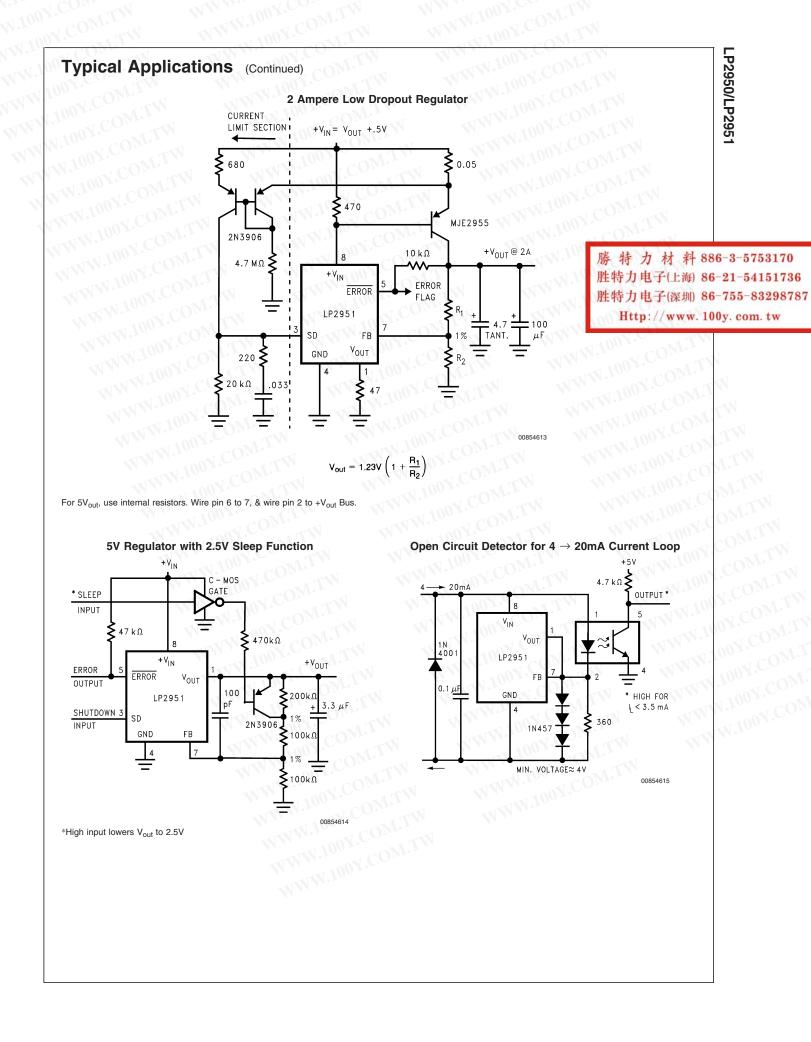
- Main output latches off at lower input voltages
- Battery backup on auxiliary output

Operation: Reg. #1's V_{out} is programmed one diode drop above 5V. Its error flag becomes active when $V_{in} \leq 5.7V$. When V_{in} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When Vin again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

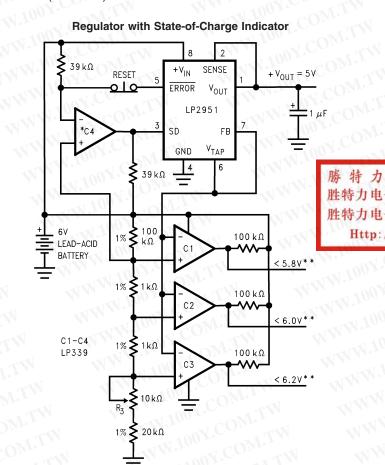
Latch Off When Error Flag Occurs



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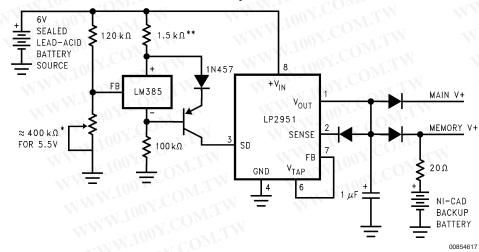


Typical Applications (Continued)



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*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V. **Outputs go low when V_{in} drops below designated thresholds.



Low Battery Disconnect

00854616

For values shown, Regulator shuts down when $V_{in} < 5.5V$ and turns on again at 6.0V. Current drain in disconnected mode is $\approx 150\mu$ A. *Sets disconnect Voltage

**Sets disconnect Hysteresis

WW.19<u>07</u>.COM.TW Typical Applications (Continued)

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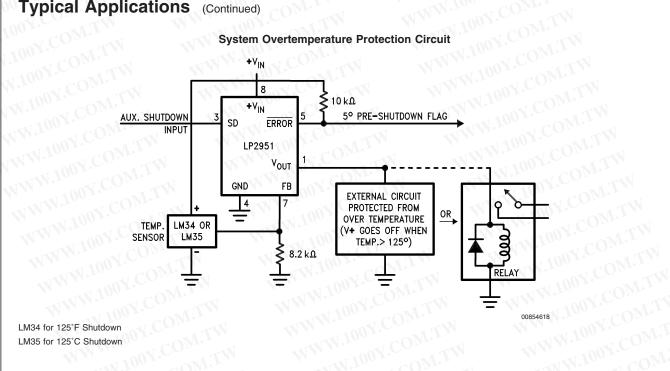
System Overtemperature Protection Circuit

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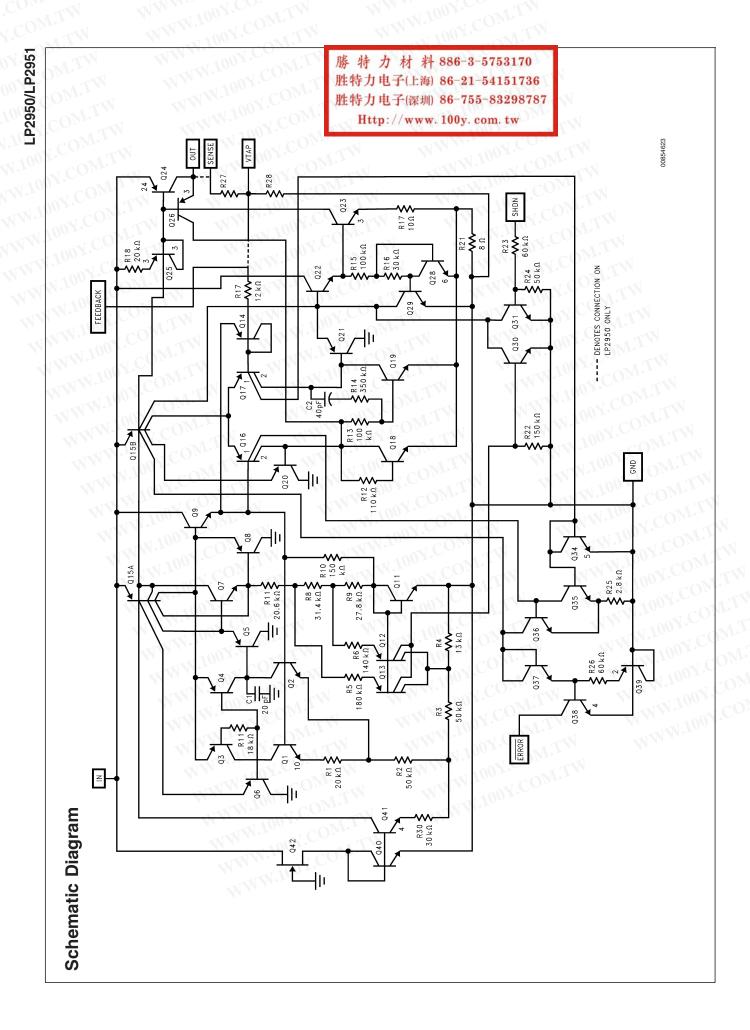
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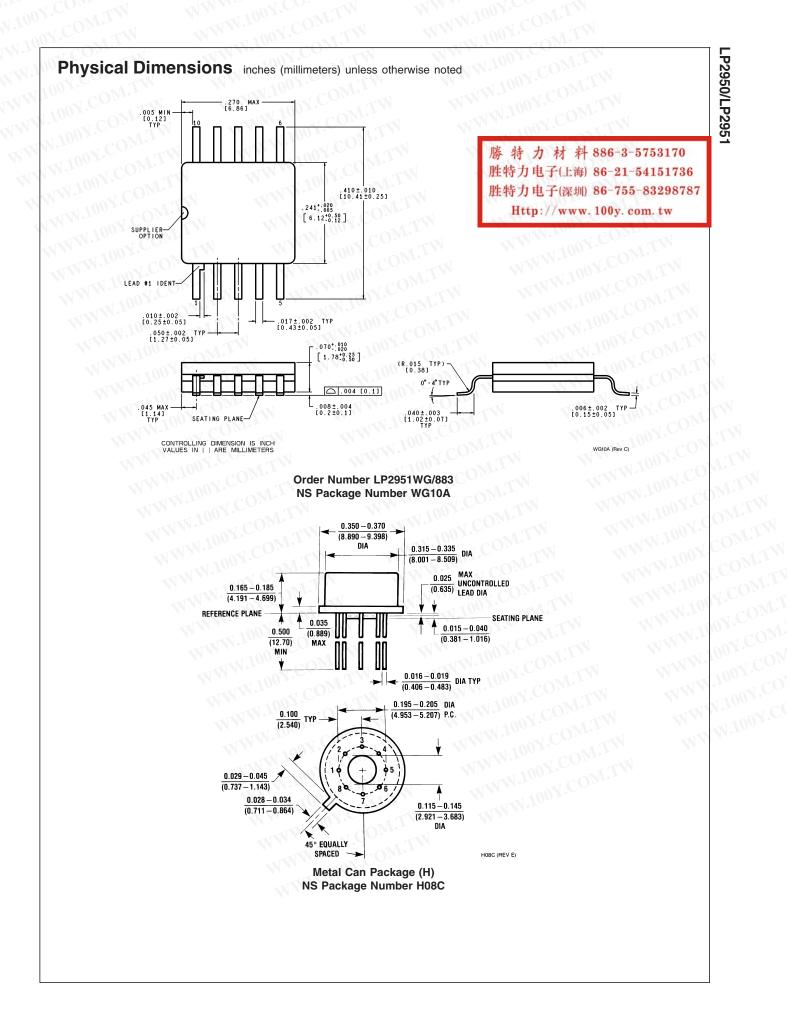
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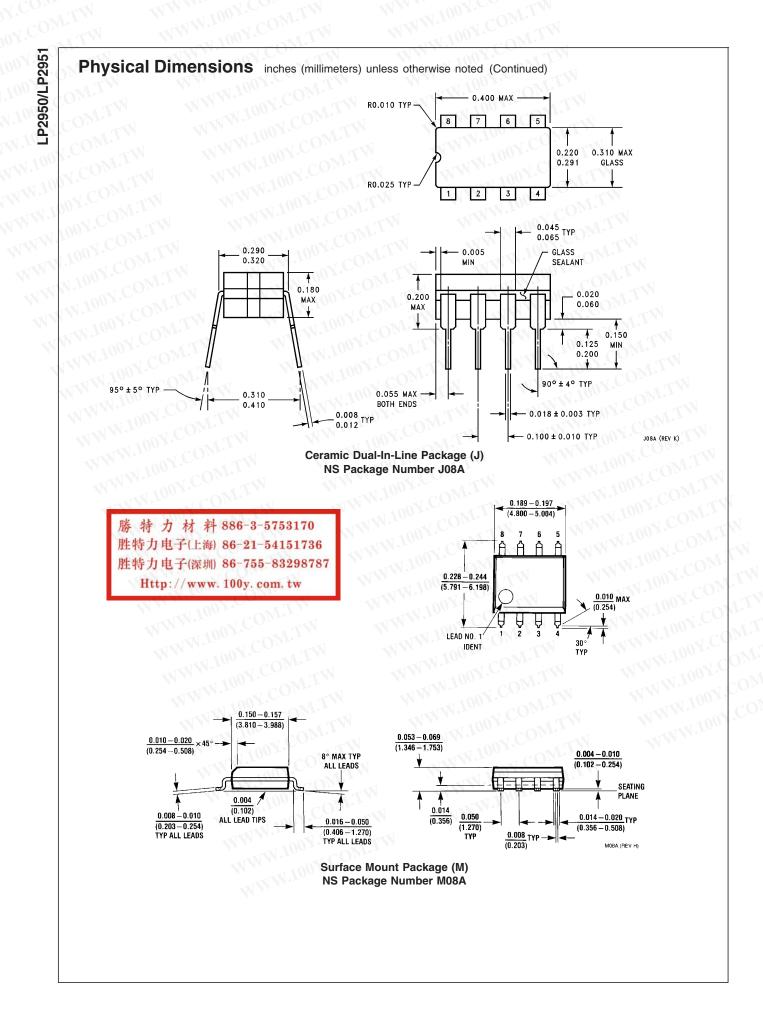
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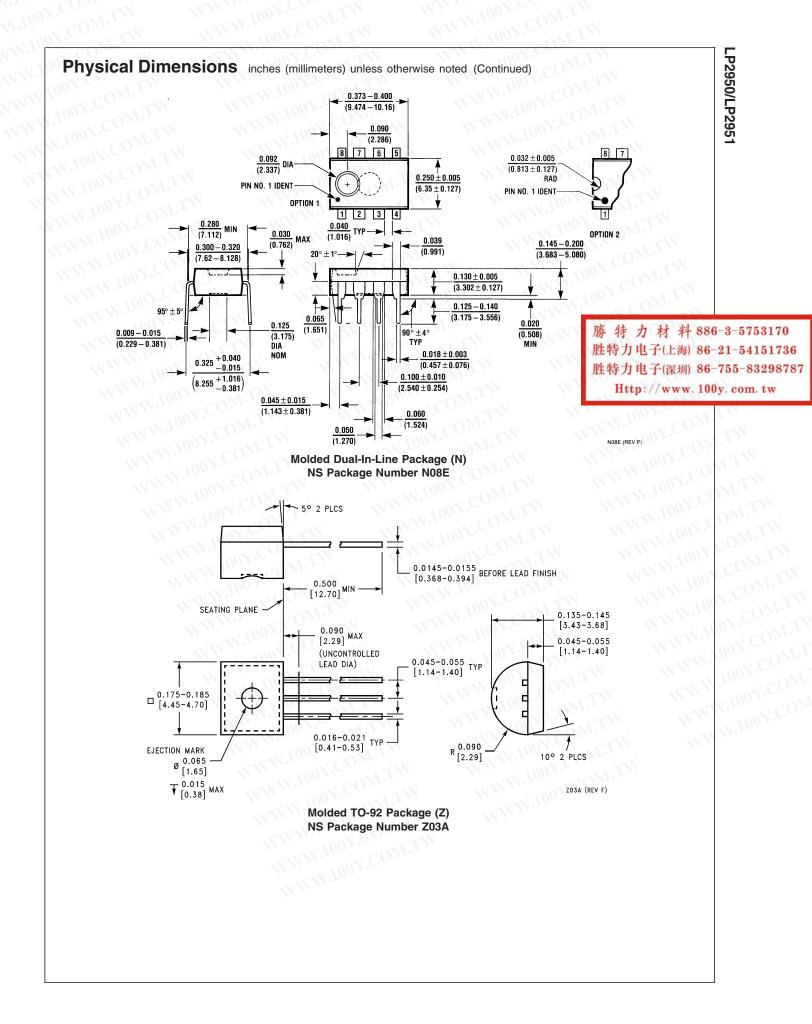
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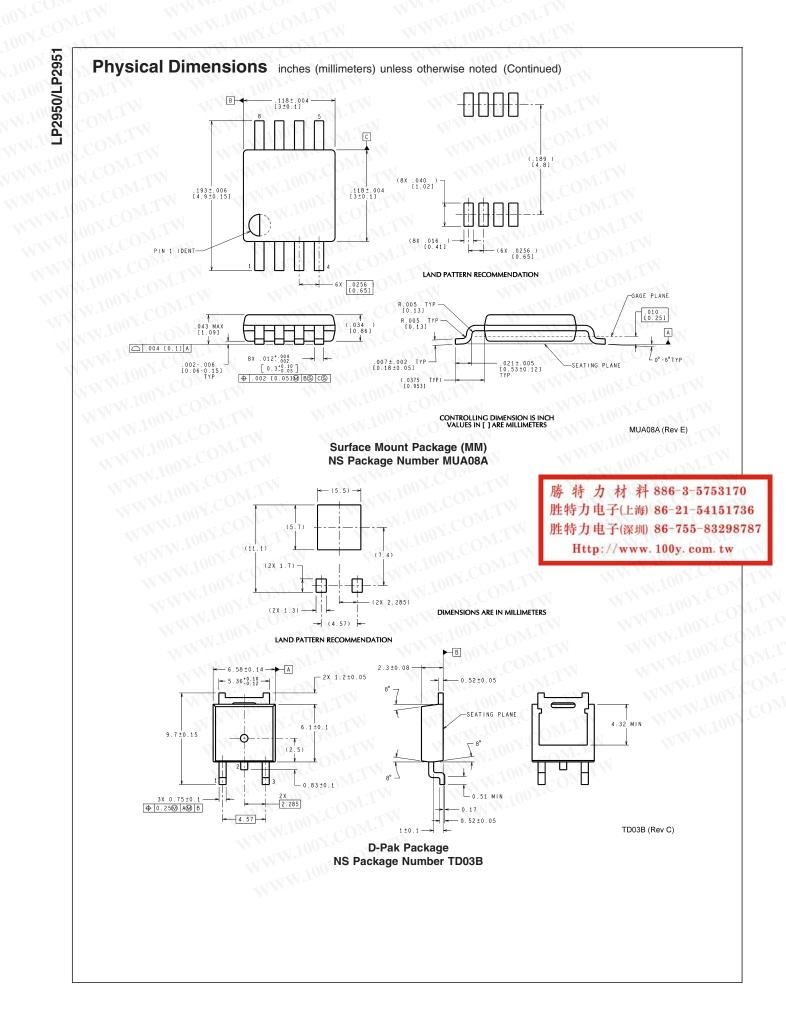
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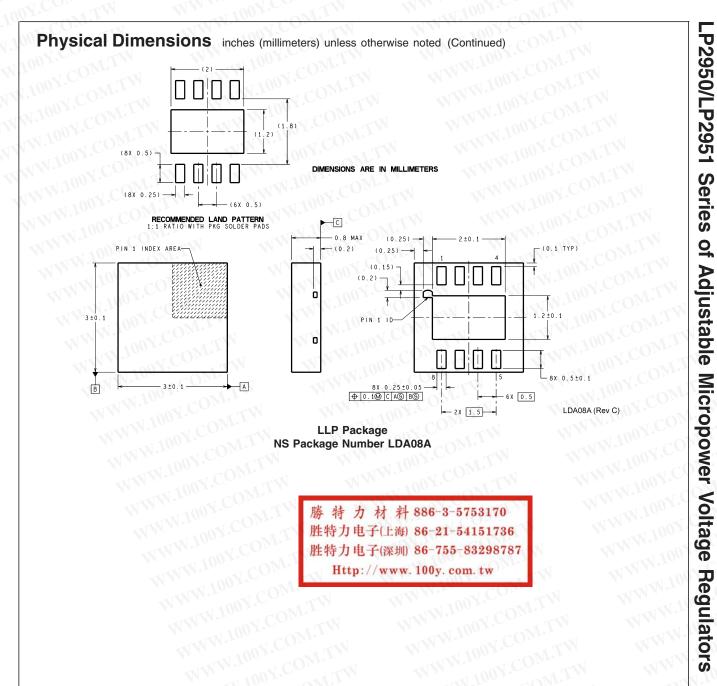












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