INTEGRATED CIRCUITS

DATA SHEET

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

LM139/239/239A/339/339A/LM2901/MC 3302

Quad voltage comparator

Product specification

1995 Nov 27

IC11 Data Handbook





Quad voltage comparator

LM139/239/239A/339/339A /LM2901/MC3302

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though they are operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

- Wide single supply voltage range 2.0V_{DC} to 36V_{DC} or dual supplies $\pm 1.0 V_{DC}$ to $\pm 18 V_{DC}$
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0V_{DC})
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage
- Input common–mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

PIN CONFIGURATION

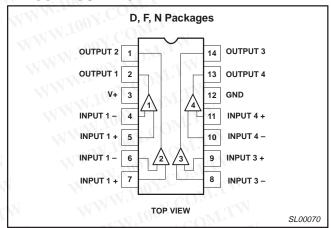


Figure 1. Pin Configuration

EQUIVALENT CIRCUIT

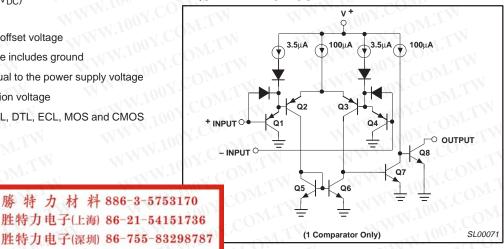


Figure 2. Equivalent Circuit

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG#
14-Pin Ceramic Dual In-Line Package (Cerdip)	−55 to +125°C	LM139F	0581B
14–Pin Plastic Dual In-Line Package (DIP)	−25°C to +85°C	LM239AN	SOT27-1
14–Pin Plastic Dual In-Line Package (DIP)	−25°C to +85°C	LM239N	SOT27-1
14–Pin Plastic Small Outline (SO) Package	−25°C to +85°C	LM239D	SOT108-1
14–Pin Plastic Dual In-Line Package (DIP)	-40°C to +125°C	LM2901N	SOT27-1
14-Pin Plastic Small Outline (SO) Package	-40°C to +125°C	LM2901D	SOT108-1
14–Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM339AN	SOT27-1
14–Pin Plastic Small Outline (SO) Package	0 to +70°C	LM339D	SOT108-1
14–Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM339N	SOT27-1
14–Pin Plastic Small Outline (SO) Package	-40°C to +85°C	MC3302D	SOT108-1
14-Pin Ceramic Dual In-Line Package (Cerdip)	-40°C to +85°C	MC3302F	0581B
14–Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	MC3302N	SOT27-1
14–Pin Plastic Dual In-Line Package (DIP)	−55 to +125°C	LM139N	SOT27-1

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	V _{CC} supply voltage	36 or ±18	V _{DC}
V_{DIFF}	Differential input voltage	36	V _{DC}
V _{IN}	Input voltage	-0.3 to +36	V _{DC}
P _D COV	Maximum power dissipation, T _A =25°C (still–air) ¹	OX.COM.TW	
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
100 F. COM	Output short–circuit to ground ²	Continuous	- KN
I _{IN}	Input current (V _{IN} <-0.3V _{DC}) ³	50	mA
T _A	Operating temperature range	T 100Y.	T. M.
	LM139	-55 to +125	°C W
	LM239/239A	-25 to +85	°C
	LM339/339A	0 to +70	°C
	LM2901	-40 to +125	°C
	MC3302	-40 to +85	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10sec max)	300	°C ·

NOTES:

- 1. Derate above 25°C, at the following rates:
 - F Package at 9.5mW/°C
 - N Package at 11.4mW/°C
 - D Package at 8.3mW/°C
- 2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
- 3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than -0.3V_{DC}.

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LM139/239/239A/339/339A/ LM2901/MC3302

DC AND AC ELECTRICAL CHARACTERISTICS

 $V+=5V_{DC}, LM139: -55^{\circ}C \leq T_{A} \leq 125^{\circ}C; LM239/239A: -25^{\circ}C \leq T_{A} \leq 85^{\circ}C; LM339/339A: 0^{\circ}C \leq T_{A} \leq 70^{\circ}C;; LM2901: -40^{\circ}C \leq T_{A} \leq 125^{\circ}C, MC3302: -40^{\circ}C \leq T_{A} \leq 85^{\circ}C, unless otherwise specified.$

SYMBOL	PARAMETER	TEST CONDITIONS		M239A/3	39A	UNIT
STWBUL	PARAMETER	TEST CONDITIONS	Min	Тур	Max	UNII
Vos	Input offset voltage ²	T _A =25°C Over temp.	OM.	±1.0	±2.0 ±4.0	mV mV
V _{CM}	Input common–mode voltage range ³	T _A =25°C Over temp.	0	WT	V+-1.5 V+-2.0	V
V _{IDR}	Differential input voltage ¹	Keep all V _{IN} ^s ≥0V _{DC} (or V– if need)	V.CO	M.TV	V+	٧
I _{BIAS}	Input bias current ⁴	I _{IN(+)} or I _{IN(-)} with output in linear range T _A =25°C Over temp.	100X.C	25	250 400	nA nA
los	Input offset current	I _{IN(+)} -I _{IN(-)} T _A =25°C Over temp.	N.1007	±5.0	±50 ±150	nA nA
l _{OL}	Output sink current	$V_{IN(-)} \ge 1V_{DC}, V_{IN}(+) = 0,$ $V_{O} \le 1.5V_{DC},$ $T_{A} = 25^{\circ}C$	6.0	16	OM.TV	mA
MMA	Output leakage current	$V_{IN(+)} \ge 1V_{DC}$, $V_{IN}(-) = 0$ $V_{O} = 5V_{DC}$, $T_{A} = 25$ °C $V_{O} = 30V_{DC}$, over temp.	MAM	0.1	1.0	nA μA
l _{cc}	Supply current	R _L =∞ on comparators, T _A =25°C V+=30V	WW	0.8	2.0	mA
A _V	Voltage gain	R _L ≥15kΩ, V+=15V _{DC}	50	200	100X.C	V/mV
V _{OL}	Saturation voltage	$V_{\text{IN}(-)} \ge 1 V_{\text{DC}}, \ V_{\text{IN}(+)} = 0, \ I_{\text{SINK}} \le 4 \text{mA} \ T_{\text{A}} = 25^{\circ}\text{C} \ \text{Over temp.}$		250	400 700	mV mV
t _{LSR}	Large-signal response time	V_{IN} =TTL logic swing, V_{REF} =1.4 V_{DC} , V_{RL} =5 V_{DC} , R_L =5.1 $k\Omega$, T_A =25°C	N	300	N. You	ns
t _R	Response time ⁵	V_{RL} =5 V_{DC} , R_L =5.1k Ω , T_A =25°C	W	1.3	MAN.	μs

See notes at the end of the Electrical Characteristics.

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1995 Nov 27 4

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SYMBOL	PARAMETER	TEST CONDITIONS		LM13	9		LM239/	339	UNIT
STWBUL	PARAMETER	TEST CONDITIONS	Min	Тур	Max	Min	Тур	Max	UNII
Vos	Input offset voltage ²	T _A =25°C Over temp.	WW	±2.0	±5.0 ±9.0	TV	±2.0	±5.0 ±9.0	mV mV
V _{CM}	Input common–mode voltage range ³	T _A =25°C Over temp.	0	W.10	V+-1.5 V+-2.0	0	N	V+-1.5 V+-2.0	٧
V _{IDR}	Differential input voltage ¹	Keep all V _{IN} s≥0V _{DC} (or V– if need)	W	WW.1	V+ C	OM:	IN	V+	V
I _{BIAS}	Input bias current ⁴	I _{IN(+)} or I _{IN(-)} with output in linear range T _A =25°C Over temp.	1	25	100 300	V.CO	25	250 400	nA nA
los	Input offset current	I _{IN(+)} −I _{IN(−)} T _A =25°C		±3.0	±25	oy.C	±5.0	±50	nA
	ONY.CO TY	Over temp.		1/1	±100	00x.		±150	nA
I _{OL}	Output sink current	V _{IN(−)} ≥1V _{DC} , V _{IN} (+)=0, V _O ≤1.5V _{DC} , T _A =25°C	6.0	16	MAM	6.0	16	MITY	mA
WW	W.100Y.COM.TW	V _{IN(+)} ≥1V _{DC} , V _{IN} (-)=0 V _O =5V _{DC} ,	TW		WW	W.10	ov.C	OM.T	N
	Output leakage current	T _A =25°C V _O =30V _{DC} ,	M.T	0.1	1.0	WW.	0.1	COM. 1-9.0	nA μA
I _{CC}	Supply current	over temp. $R_L=\infty$ on comparators, $T_A=25^{\circ}C$ $V+=30V$	COM	0.8	2.0	NN	0.8	2.0	mΑ
A _V	Voltage gain	R _L ≥15kΩ, V+=15V _{DC}	50	200		50	200	1001	V/mV
V _{OL}	Saturation voltage	$V_{IN(-)} \ge 1 V_{DC}, V_{IN(+)} = 0,$ $I_{SINK} \le 4 mA$ $T_A = 25 °C$ Over temp.	07.C	250	400 700		250	400 700	mV mV
t _{LSR}	Large-signal response time	V_{IN} =TTL logic swing, V_{REF} =1.4 V_{DC} , V_{RL} =5 V_{DC} , R_L =5.1 $k\Omega$, T_A =25°C	700X	300	M.TW		300	MN.10	ns
t _R	Response time ⁵	V_{RL} =5 V_{DC} , R_{L} =5.1 $k\Omega$, T_{A} =25° C	1.100	1.3	MI	V	1.3	WW.	μs

See notes on following page.

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 $V + = 5V_{DC}, LM139: -55^{\circ}C \leq T_{A} \leq 125^{\circ}C; LM239/239A: -25^{\circ}C \leq T_{A} \leq 85^{\circ}C; LM339/339A: 0^{\circ}C \leq T_{A} \leq 70^{\circ}C; LM2901: -40^{\circ}C \leq T_{A} \leq 125^{\circ}C, MC3302: -40^{\circ}C \leq T_{A} \leq 85^{\circ}C, unless otherwise specified.$

SYMBOL	DADAMETER	TEST COMPITIONS	1,1,1	LM290)1		MC330)2	UNIT
SYMBOL	PARAMETER	TEST CONDITIONS	Min	Тур	Max	Min	Тур	Max	UNII
Vos	Input offset voltage ²	T _A =25°C Over temp.	WW	±2.0 ±9	±7.0 ±15	TV	±3.0	±20 ±40	mV mV
V _{CM}	Input common–mode voltage range ³	T _A =25°C Over temp.	0	N.10	V+-1.5 V+-2.0	0 0	N	V+-1.5 V+-2.0	V
V _{IDR}	Differential input voltage ¹	Keep all V _{IN} s≥0V _{DC} (or V– if need)	W	WW.	V+	OM.	TW	V+	V
I _{BIAS}	Input bias current ⁴	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A =25°C Over temp.	V	25 200	250 500		25	500 1000	nA nA
los	Input offset current	I _{IN(+)} -I _{IN(-)} T _A =25°C Over temp.		±5 ±50	±50 ±200	07.C	±5	±100 ±300	nA nA
l _{OL}	Output sink current	V _{IN(-)} ≥1V _{DC} , V _{IN} (+)=0, V _O ≤1.5V _{DC} , T _A =25°C	6.0	16	WW.	100X	16	M.I.M	mA
WW	Output leakage current	$V_{IN(+)} \ge 1V_{DC}$, $V_{IN}(-) = 0$ $V_{O} = 5V_{DC}$, $T_{A} = 25^{\circ}C$ $V_{O} = 30V_{DC}$, over temp.	TW	0.1	1.0	N.100 N.10	0.1	OM. TO 1.0	nA μA
- 14	100 - COM.	R _L =∞ on all comparators,	Mr.	-1		Wir	.8	1.8	mA
Icc 1	Supply current	T _A =25°C	-21.7	0.8	2.0		100		1.1,
	MAN. TO ON COM.	R _L =∞ on all comparators, V+=30V	322	1.0	2.5	MAA	100	N.C.	mA
A _V	Voltage gain	R _L ≥15kΩ, V+=15V _{DC}	25	100		2	100	OOY.CC	V/mV
V _{OL}	Saturation voltage	$V_{IN(-)} \ge 1V_{DC}, V_{IN(+)} = 0,$ $I_{SINK} \le 4mA$ $T_A = 25^{\circ}C$ Over temp.	(CO)	400	400 700	N	150	400 700	mV mV
t _{LSR}	Large-signal response time	V_{IN} =TTL logic swing, V_{REF} =1.4 V_{DC} , V_{RL} =5 V_{DC} , R_L =5.1 $k\Omega$, T_A =25°C	WY.	300	TW		300	N.700	ns
t _R	Response time ⁵	V_{RL} =5 V_{DC} , R_L =5.1 $k\Omega$, T_A =25° C	1001	1.3	WIN		1.3	W. 10	μѕ

NOTES:

- Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V_{DC} (or 0.3V_{DC} below the magnitude of the negative power supply, if used).
- 2. At output switch point, $V_O \approx 1.4 V_{DC}$, $R_S = 0 \Omega$ with V+ from 5V_{DC} to 30V_{DC}; and over the full input common—mode range (0V_{DC} to V+ $-1.5 V_{DC}$). Inputs of unused comparators should be grounded.
- The input common—mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of
 the common—mode voltage range is V+ 1.5V, but either or both inputs can go to 30V_{DC} without damage.
- 4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- 5. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained (see typical performance characteristics section).

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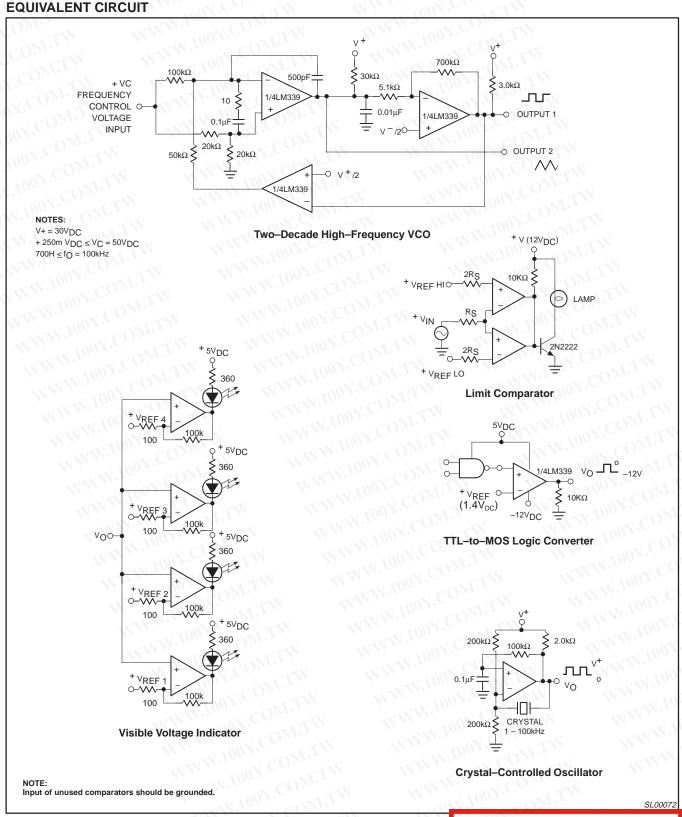


Figure 3. Equivalent Circuit

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TYPICAL PERFORMANCE CHARACTERISTICS

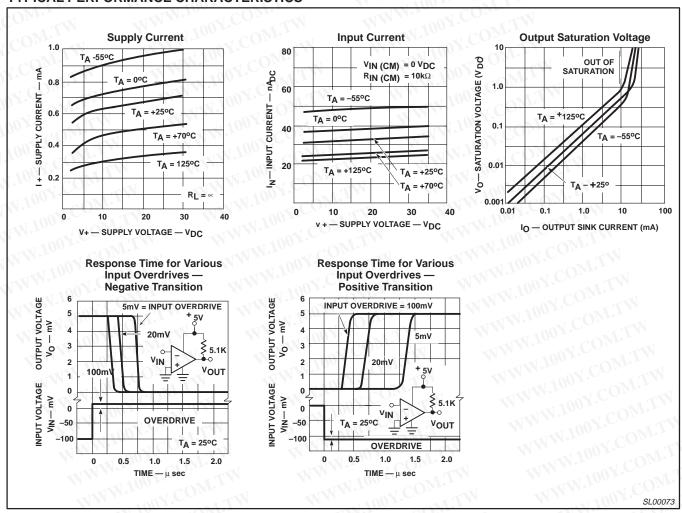


Figure 4. Typical Performance Characteristics

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Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philip Semiconductors reserves the right to make changes at any time without notice in order to improve desig and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make change at any time without notice, in order to improve design and supply the best possible product.

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