May 1999

National Semiconductor

LM7171
Very High Speed, High Output Current, Voltage Feedback Amplifier

General Description

The LM7171 is a high speed voltage feedback amplifier that has the slewing characteristic of a current feedback amplifier; yet it can be used in all traditional voltage feedback amplifier configurations. The LM7171 is stable for gains as low as +2 or −1. It provides a very high slew rate at 4100V/μs and a wide unity-gain bandwidth of 200 MHz while consuming only 6.5 mA of supply current. It is ideal for video and high speed signal processing applications such as HDSL and pulse amplifiers. With 100 mA output current, the LM7171 can be used for video distribution, as a transformer driver or as a laser diode driver.

Operation on ±15V power supplies allows for large signal swings and provides greater dynamic range and signal-to-noise ratio. The LM7171 offers low SFDR and THD, ideal for ADC/DAC systems. In addition, the LM7171 is specified for ±5V operation for portable applications.

The LM7171 is built on National's advanced VIP™ III (Vertically integrated PNP) complementary bipolar process.

Features

(Typical Unless Otherwise Noted)

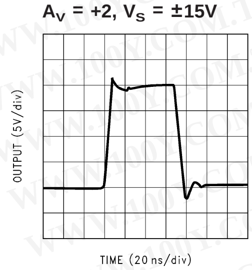
- Easy-To-Use Voltage Feedback Topology
- Very High Slew Rate: 4100V/μs
- Wide Unity-Gain Bandwidth: 200 MHz
- −3 dB Frequency @ A_V = +2: 220 MHz
- Low Supply Current: 6.5 mA
- High Open Loop Gain: 85 dB
- High Output Current: 100 mA
- Differential Gain and Phase: 0.01%, 0.02˚
- Specified for ±15V and ±5V Operation

Applications

- HDSL and ADSL Drivers
- Multimedia Broadcast Systems
- Professional Video Cameras
- Video Amplifiers
- Copiers/Scanners/Fax
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- CATV/Fiber Optics Signal Processing

Typical Performance

Large Signal Pulse Response
A_V = +2, V_S = ±15V



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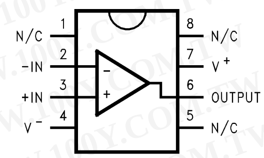
Connection Diagrams

8-Pin DIP/SO



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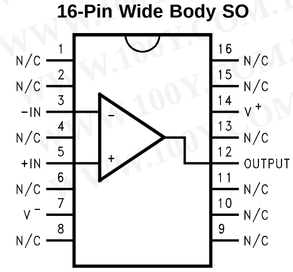
Top View

16-Pin Wide Body SO



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Top View

VIP™ is a trademark of National Semiconductor Corporation.

Ordering Information

Package	Temperature Range		Transport Media	NSC Drawing
	Industrial −40˚C to +85˚C	Military −55˚C to +125˚C		
8-Pin DIP	LM7171AIN, LM7171BIN		Rails	N08E
8-Pin CDIP	LM7171AMJ-QML LM7171AMJ-QMLV	5962-95536	Rails	J08A
10-Pin Ceramic SOIC	LM7171AMWG-QML LM7171AMWG-QMLV	5962-95536	Trays	WG10A
8-Pin Small Outline	LM7171AIM, LM7171BIM		Rails	M08A
	LM7171AIMX, LM7171BIMX		Tape and Reel	
16-Pin Small Outline	LM7171AIWM, LM7171BIWM		Rails	M16B
	LM7171AWMX, LM7171BWMX		Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2.5 kV
Supply Voltage ($V^+ – V^-$)	36V
Differential Input Voltage (Note 11)	±10V
Output Short Circuit to Ground (Note 3)	Continuous
Storage Temperature Range	−65˚C to +150˚C
Maximum Junction Temperature (Note 4)	150˚C

Operating Ratings (Note 1)

Supply Voltage	$5.5V \le V_S \le 36V$
Junction Temperature Range	
LM7171AI, LM7171BI	$−40˚C \le T_J \le +85˚C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	108˚C/W
M Package, 8-Pin Surface Mount	172˚C/W
M Package, 16-Pin Surface Mount	95˚C/W

±15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7171AI Limit (Note 6)	LM7171BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.2	1 **4**	3 **7**	mV max
TC V_{OS}	Input Offset Voltage Average Drift		35			μV/˚C
I_B	Input Bias Current		2.7	10 **12**	10 **12**	μA max
I_{OS}	Input Offset Current		0.1	4 **6**	4 **6**	μA max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	3.3			
R_O	Open Loop Output Resistance		15			Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	105	85 **80**	75 **70**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	90	85 **80**	75 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR > 60 dB	±13.35			V
A_V	Large Signal Voltage Gain (Note 7)	R_L = 1 kΩ	85	80 **75**	75 **70**	dB min
		R_L = 100Ω	81	75 **70**	70 **66**	dB min
V_O	Output Swing	R_L = 1 kΩ	13.3	13 **12.7**	13 **12.7**	V min
			−13.2	−13 **−12.7**	−13 **−12.7**	V max
		R_L = 100Ω	11.8	10.5 **9.5**	10.5 **9.5**	V min
			−10.5	−9.5 **−9**	−9.5 **−9**	V max
	Output Current (Open Loop) (Note 8)	Sourcing, R_L = 100Ω	118	105 **95**	105 **95**	mA min
		Sinking, R_L = 100Ω	105	95 **90**	95 **90**	mA max

±15V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7171AI Limit (Note 6)	LM7171BI Limit (Note 6)	Units
	Output Current (in Linear Region)	Sourcing, R_L = 100Ω	100			mA
		Sinking, R_L = 100Ω	100			
I_{SC}	Output Short Circuit Current	Sourcing	140			mA
		Sinking	135			
I_S	Supply Current		6.5	8.5 **9.5**	8.5 **9.5**	mA max

±15V AC Electrical Characteristics

Unless otherwise specified, T_J = 25˚C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7171AI Limit (Note 6)	LM7171BI Limit (Note 6)	Units
SR	Slew Rate (Note 9)	A_V = +2, V_{IN} = 13 V_{PP}	4100			V/µs
		A_V = +2, V_{IN} = 10 V_{PP}	3100			
	Unity-Gain Bandwidth		200			MHz
	−3 dB Frequency	A_V = +2	220			MHz
ϕ_m	Phase Margin		50			Deg
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 500Ω	42			ns
t_p	Propagation Delay	A_V = −2, V_{IN} = ±5V, R_L = 500Ω	5			ns
A_D	Differential Gain (Note 10)		0.01			%
ϕ_D	Differential Phase (Note 10)		0.02			Deg
	Second Harmonic (Note 12)	f_{IN} = 10 kHz	−110			dBc
		f_{IN} = 5 MHz	−75			dBc
	Third Harmonic (Note 12)	f_{IN} = 10 kHz	−115			dBc
		f_{IN} = 5 MHz	−55			dBc
e_n	Input-Referred Voltage Noise	f = 10 kHz	14			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 10 kHz	1.5			$\frac{pA}{\sqrt{Hz}}$

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7171AI Limit (Note 6)	LM7171BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.3	1.5 **4**	3.5 **7**	mV max
TC V_{OS}	Input Offset Voltage Average Drift		35			µV/˚C
I_B	Input Bias Current		3.3	10 **12**	10 **12**	µA max
I_{OS}	Input Offset Current		0.1	4	4	µA

±5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7171AI Limit (Note 6)	LM7171BI Limit (Note 6)	Units
				6	**6**	max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	3.3			
R_O	Output Resistance		15			Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V	104	80 **75**	70 **65**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	90	85 **80**	75 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR > 60 dB	±3.2			V
A_V	Large Signal Voltage Gain (Note 7)	R_L = 1 kΩ	78	75 **70**	70 **65**	dB min
		R_L = 100Ω	76	72 **67**	68 **63**	dB min
V_O	Output Swing	R_L = 1 kΩ	3.4	3.2 **3**	3.2 **3**	V min
			−3.4	−3.2 **−3**	−3.2 **−3**	V max
		R_L = 100Ω	3.1	2.9 **2.8**	2.9 **2.8**	V min
			−3.0	−2.9 **−2.8**	−2.9 **−2.8**	V max
	Output Current (Open Loop) (Note 8)	Sourcing, R_L = 100Ω	31	29 **28**	29 **28**	mA min
		Sinking, R_L = 100Ω	30	29 **28**	29 **28**	mA max
I_{SC}	Output Short Circuit Current	Sourcing	135			mA
		Sinking	100			
I_S	Supply Current		6.2	8 **9**	8 **9**	mA max

±5V AC Electrical Characteristics

Unless otherwise specified, T_J = 25˚C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7171AI Limit (Note 6)	LM7171BI Limit (Note 6)	Units
SR	Slew Rate (Note 9)	A_V = +2, V_{IN} = 3.5 V_{PP}	950			V/µs
	Unity-Gain Bandwidth		125			MHz
	−3 dB Frequency	A_V = +2	140			MHz
ϕ_m	Phase Margin		57			Deg
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±1V, R_L = 500Ω	56			ns
t_p	Propagation Delay	A_V = −2, V_{IN} = ±1V, R_L = 500Ω	6			ns
A_D	Differential Gain (Note 1)		0.02			%

±5V AC Electrical Characteristics (Continued)

Unless otherwise specified, T_J = 25˚C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7171AI Limit (Note 6)	LM7171BI Limit (Note 6)	Units
ϕ_D	Differential Phase (Note 10)		0.03			Deg
	Second Harmonic (Note 12)	f_{IN} = 10 kHz	−102			dBc
		f_{IN} = 5 MHz	−70			dBc
	Third Harmonic (Note 12)	f_{IN} = 10 kHz	−110			dBc
		f_{IN} = 5 MHz	−51			dBc
e_n	Input-Referred Voltage Noise	f = 10 kHz	14			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 10 kHz	1.8			$\frac{pA}{\sqrt{Hz}}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = $(T_{J(max)}–T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typifcal values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = ±5V, V_{OUT} = ±1V.

Note 8: The open loop output current is guaranteed, by the measurement of the open loop output voltage swing, using 100Ω output load.

Note 9: Slew Rate is the average of the raising and falling slew rates.

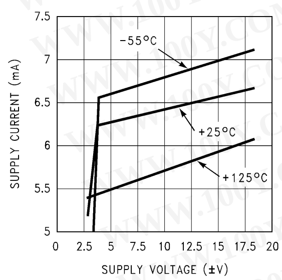
Note 10: Differential gain and phase are measured with A_V = +2, V_{IN} = 1 V_{PP} at 3.58 MHz and both input and output 75Ω terminated.

Note 11: Input differential voltage is applied at V_S = ±15V.

Note 12: Harmonics are measured with V_{IN} = 1 V_{PP}, A_V = +2 and R_L = 100Ω.

Typical Performance Characteristics unless otherwise noted, T_A= 25˚C

Supply Current vs Supply Voltage



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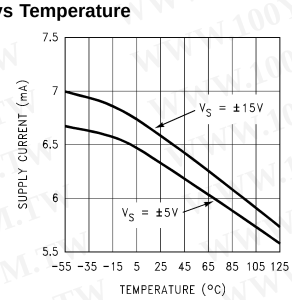
Supply Current vs Temperature



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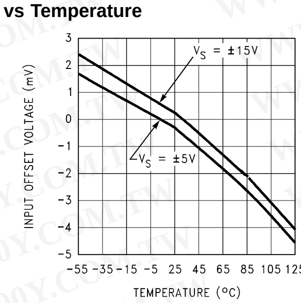
Input Offset Voltage vs Temperature



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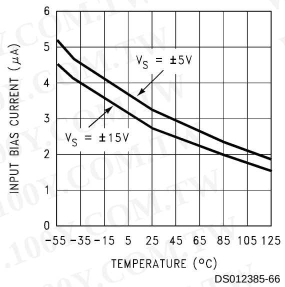
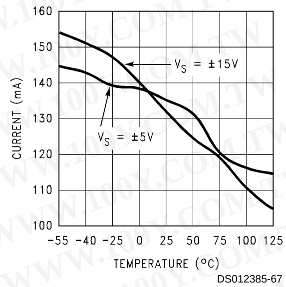
Typical Performance Characteristics unless otherwise noted, T_A= 25˚C (Continued)

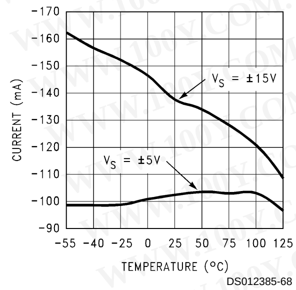
Input Bias Current vs Temperature



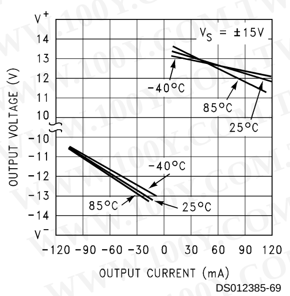
Short Circuit Current vs Temperature (Sourcing)



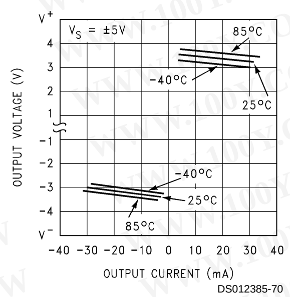
Short Circuit Current vs Temperature (Sinking)



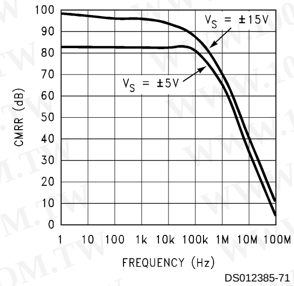
Output Voltage vs Output Current



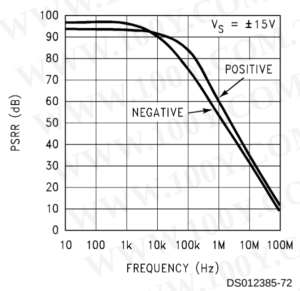
Output Voltage vs Output Current



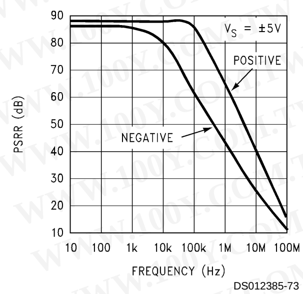
CMRR vs Frequency



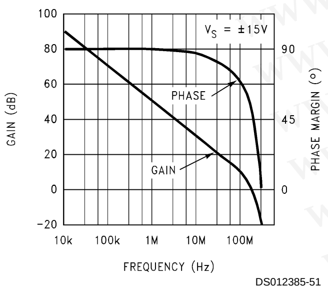
PSRR vs Frequency



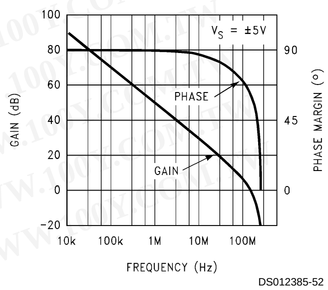
PSRR vs Frequency



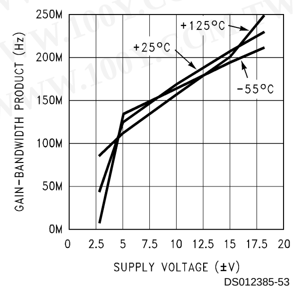
Open Loop Frequency Response



Open Loop Frequency Response

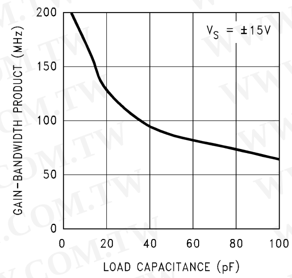


Gain-Bandwidth Product vs Supply Voltage



Typical Performance Characteristics unless otherwise noted, T_A= 25˚C (Continued)

Gain-Bandwidth Product vs Load Capacitance



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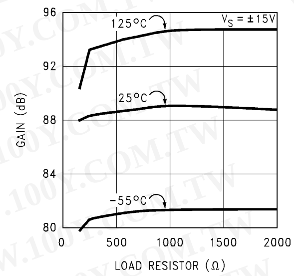
Large Signal Voltage Gain vs Load



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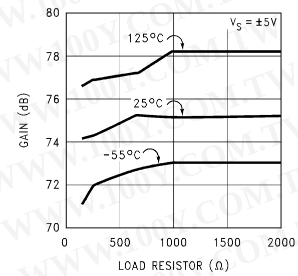
Large Signal Voltage Gain vs Load



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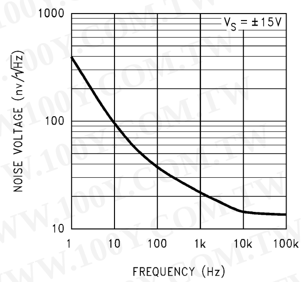
Input Voltage Noise vs Frequency



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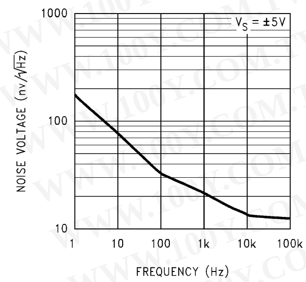
Input Voltage Noise vs Frequency



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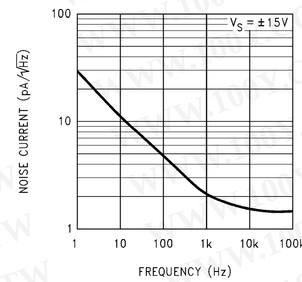
Input Current Noise vs Frequency



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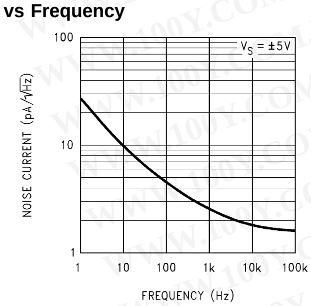
Input Current Noise vs Frequency



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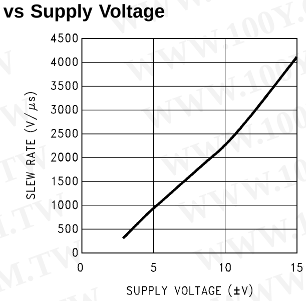
Slew Rate vs Supply Voltage



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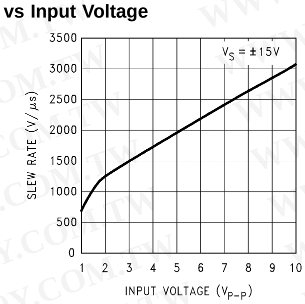
Slew Rate vs Input Voltage



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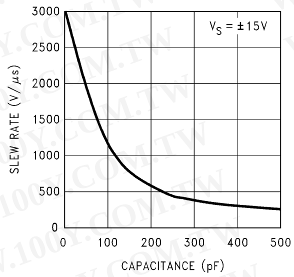
Typical Performance Characteristics unless otherwise noted, T_A= 25˚C (Continued)

Slew Rate vs Load Capacitance



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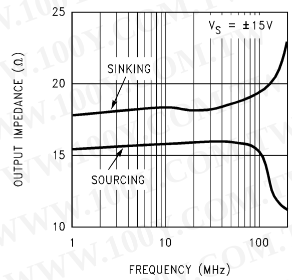
Open Loop Output Impedance vs Frequency



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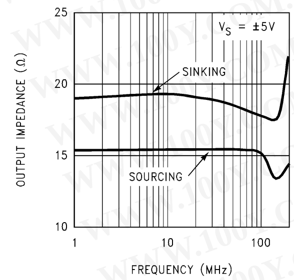
Open Loop Output Impedance vs Frequency



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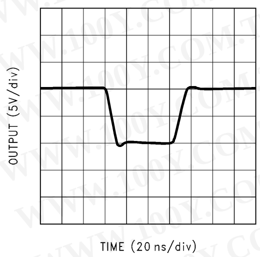
Large Signal Pulse Response A_V = −1, V_S = ±15V



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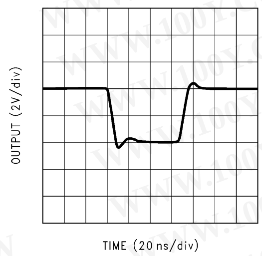
Large Signal Pulse Response A_V = −1, V_S = ±5V



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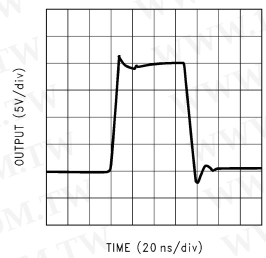
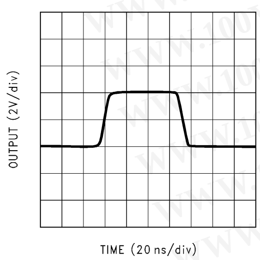
Large Signal Pulse Response A_V = +2, V_S = ±15V



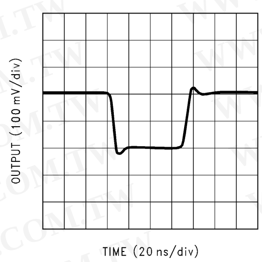
DS012385-29

Large Signal Pulse Response A_V = +2, V_S = ±5V



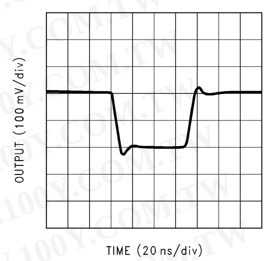
DS012385-30

Small Signal Pulse Response A_V = −1, V_S = ±15V



DS012385-31

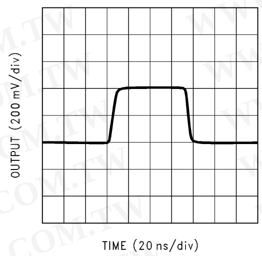
Small Signal Pulse Response A_V = −1, V_S = ±5V



DS012385-32

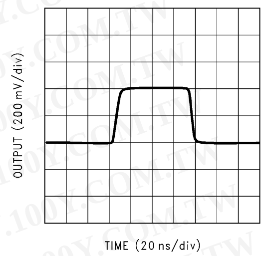
Typical Performance Characteristics unless otherwise noted, T_A= 25˚C (Continued)

Small Signal Pulse Response A_V = +2, V_S = ±15V



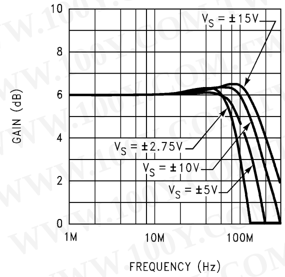
DS012385-33

Small Signal Pulse Response A_V = +2, V_S = ±5V



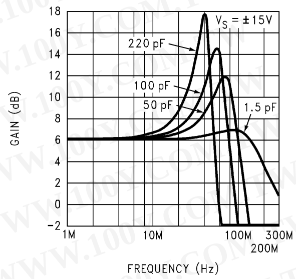
DS012385-34

Closed Loop Frequency Response vs Supply Voltage (A_V = +2)



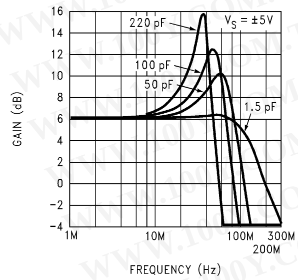
DS012385-35

Closed Loop Frequency Response vs Capacitive Load (A_V = +2)



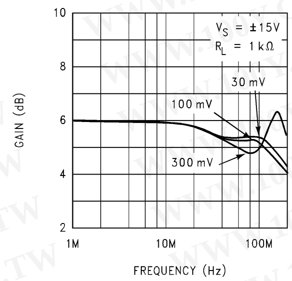
DS012385-36

Closed Loop Frequency Response vs Capacitive Load (A_V = +2)



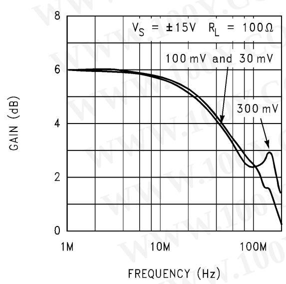
DS012385-37

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)



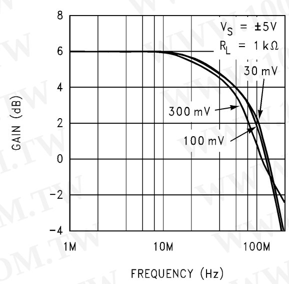
DS012385-38

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)



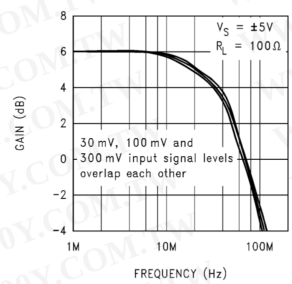
DS012385-43

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)



DS012385-39

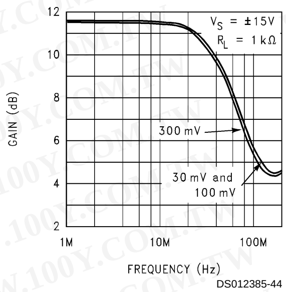
Closed Loop Frequency Response vs Input Signal Level (A_V = +2)



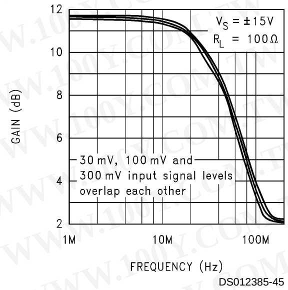
DS012385-40

Typical Performance Characteristics unless otherwise noted, T_A= 25˚C (Continued)

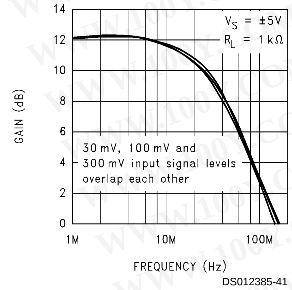
Closed Loop Frequency Response vs Input Signal Level (A_V = +4)



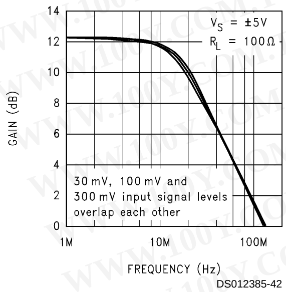
Closed Loop Frequency Response vs Input Signal Level (A_V = +4)



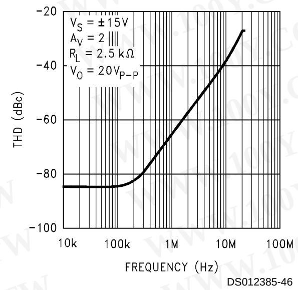
Closed Loop Frequency Response vs Input Signal Level (A_V = +4)



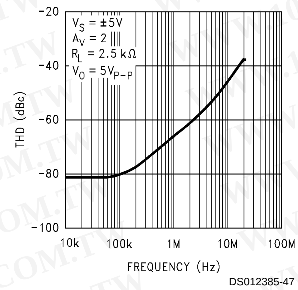
Closed Loop Frequency Response vs Input Signal Level (A_V = +4)



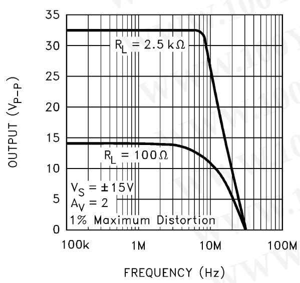
Total Harmonic Distortion vs Frequency (Note 13)



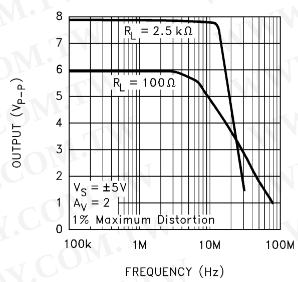
Total Harmonic Distortion vs Frequency (Note 13)



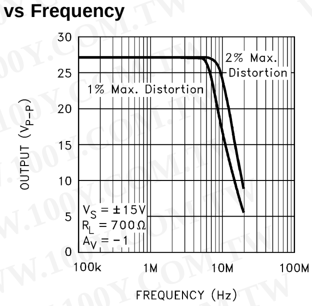
Undistorted Output Swing vs Frequency



Undistorted Output Swing vs Frequency

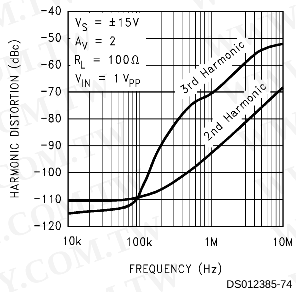


Undistorted Output Swing vs Frequency

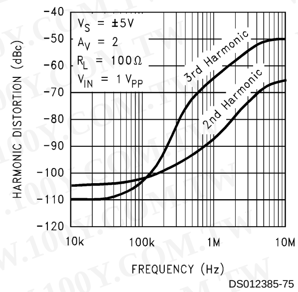


Typical Performance Characteristics unless otherwise noted, T_A= 25˚C (Continued)

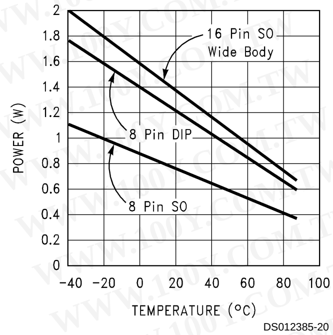
Harmonic Distortion vs Frequency



Harmonic Distortion vs Frequency

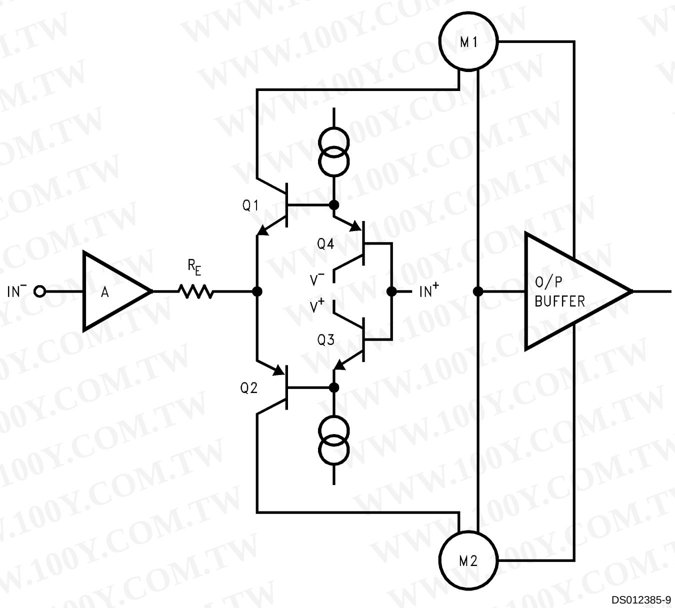


Maximum Power Dissipation vs Ambient Temperature



Note 13: The THD measurement at low frequency is limited by the test instrument.

Simplified Schematic Diagram



Note: M1 and M2 are current mirrors.

Application Notes

LM7171 Performance Discussion

The LM7171 is a very high speed, voltage feedback amplifier. It consumes only 6.5 mA supply current while providing a unity-gain bandwidth of 200 MHz and a slew rate of 4100V/µs. It also has other great features such as low differential gain and phase and high output current.

The LM7171 is a true voltage feedback amplifier. Unlike current feedback amplifiers (CFAs) with a low inverting input impedance and a high non-inverting input impedance, both inputs of voltage feedback amplifiers (VFAs) have high impedance nodes. The low impedance inverting input in CFAs and a feedback capacitor create an additional pole that will lead to instability. As a result, CFAs cannot be used in traditional op amp circuits such as photodiode amplifiers, I-to-V converters and integrators where a feedback capacitor is required.

LM7171 Circuit Operation

The class AB input stage in LM7171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM7171 Simplified Schematic, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buff-

LM7171 Circuit Operation (Continued)

ers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM7171 Slew Rate Characteristic

The slew rate of LM7171 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations. A curve of slew rate versus input voltage level is provided in the "Typical Performance Characteristics".

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external resistor such as 1 kΩ in series with the input of LM7171, the bandwidth is reduced to help lower the overshoot.

Slew Rate Limitation

If the amplifier's input signal has too large of an amplitude at too high of a frequency, the amplifier is said to be slew rate limited; this can cause ringing in time domain and peaking in frequency domain at the output of the amplifier.

In the "Typical Performance Characteristics" section, there are several curves of $A_V = +2$ and $A_V = +4$ versus input signal levels. For the $A_V = +4$ curves, no peaking is present and the LM7171 responds identically to the different input signal levels of 30 mV, 100 mV and 300 mV.

For the $A_V = +2$ curves, with slight peaking occurs. This peaking at high frequency (>100 MHz) is caused by a large input signal at high enough frequency that exceeds the amplifier's slew rate. The peaking in frequency response does not limit the pulse response in time domain, and the LM7171 is stable with noise gain of ≥+2.

Layout Consideration

PRINTED CIRCUIT BOARDS AND HIGH SPEED OP AMPS

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect high frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENT SELECTION AND FEEDBACK RESISTOR

It is important in high speed applications to keep all component leads short. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM7171, a feedback resistor of 510Ω gives optimal performance.

Compensation for Input Capacitance

The combination of an amplifier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F$$

can be used to cancel that pole. For LM7171, a feedback capacitor of 2 pF is recommended. *Figure 1* illustrates the compensation circuit.

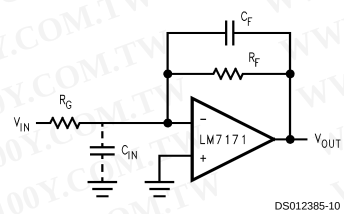


FIGURE 1. Compensating for Input Capacitance

Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 µF ceramic capacitors directly to power supply pins and 2.2 µF tantalum capacitors close to the power supply pins.

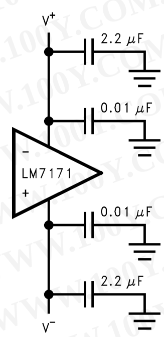


FIGURE 2. Power Supply Bypassing

Termination

In high frequency applications, reflections occur if signals are not properly terminated. *Figure 3* shows a properly terminated signal while *Figure 4* shows an improperly terminated signal.

Termination (Continued)

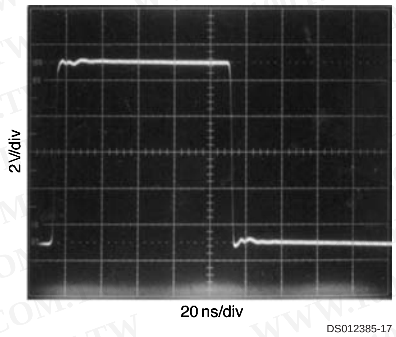


FIGURE 3. Properly Terminated Signal

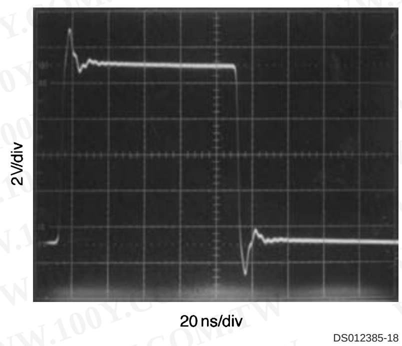


FIGURE 4. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown below in *Figure 5* The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM7171, a 50Ω isolation resistor is recommended for initial evaluation. *Figure 6* shows the LM7171 driving a 150 pF load with the 50Ω isolation resistor.

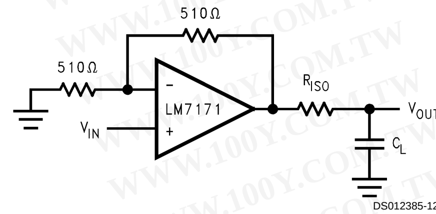


FIGURE 5. Isolation Resistor Used to Drive Capacitive Load

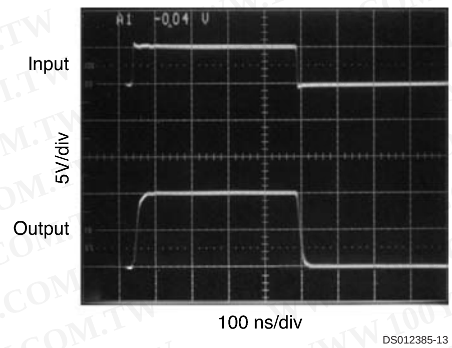


FIGURE 6. The LM7171 Driving a 150 pF Load with a 50Ω Isolation Resistor

Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A)/\theta_{JA}$$

Where

PD	is the power dissipation in a device
$T_{J(max)}$	is the maximum junction temperature
T_A	is the ambient temperature
θ_{JA}	is the thermal resistance of a particular package

For example, for the LM7171 in a SO-8 package, the maximum power dissipation at 25˚C ambient temperature is 730 mW.

Thermal resistance, θ_{JA}, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin DIP package has a lower thermal resistance (108˚C/W) than that of 8-pin SO (172˚C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L$$

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

P_Q:	=	supply current x total supply voltage with no load
P_L:	=	output current x (voltage difference between supply voltage and output voltage of the same side of supply voltage)

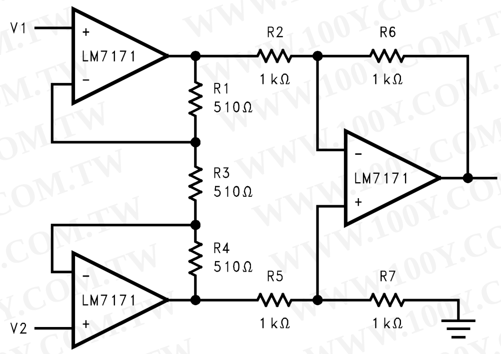
Power Dissipation (Continued)

For example, the total power dissipated by the LM7171 with $V_S = \pm15V$ and output voltage of 10V into 1 kΩ is

$$\begin{aligned} P_D &= P_Q + P_L \\ &= (6.5\text{ mA}) \times (30V) + (10\text{ mA}) \times (15V - 10V) \\ &= 195\text{ mW} + 50\text{ mW} \\ &= 245\text{ mW} \end{aligned}$$

Application Circuit

Fast Instrumentation Amplifier



DS012385-14

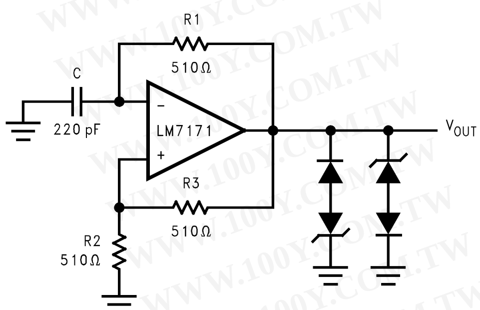
$$V_{IN} = V_2 - V_1$$

if R6 = R2, R7 = R5, and R1 = R4

$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2}\left(1 + 2\frac{R1}{R3}\right) = 3$$

DS012385-80

Multivibrator



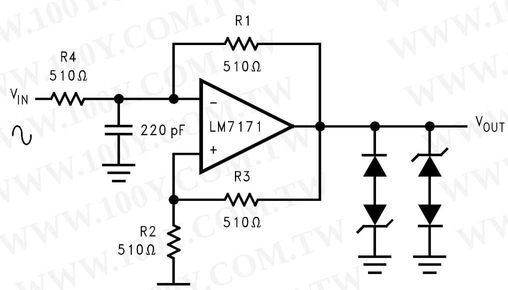
DS012385-15

$$f = \frac{1}{2\left(R1\,C\,\ln\left(1 + 2\frac{R2}{R3}\right)\right)}$$

f = 4 MHz

DS012385-81

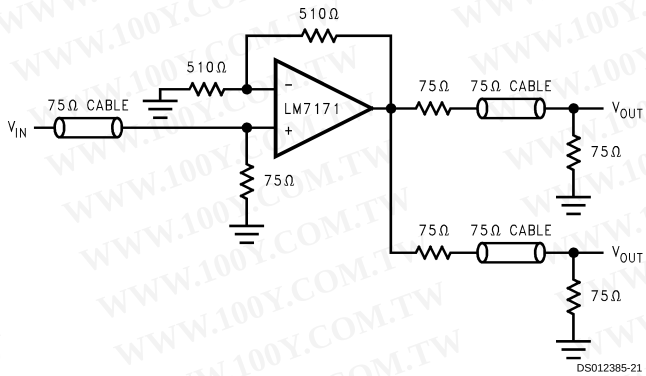
Pulse Width Modulator



DS012385-16

Application Circuit (Continued)

Video Line Driver



Design Kit

A design kit is available for the LM7171. The design kit contains:

- High Speed Evaluation Board
- LM7171 in 8-pin DIP Package
- LM7171 Datasheet
- Pspice Macromodel DIskette With The LM7171 Macromodel
- Amplifier Selection Guide

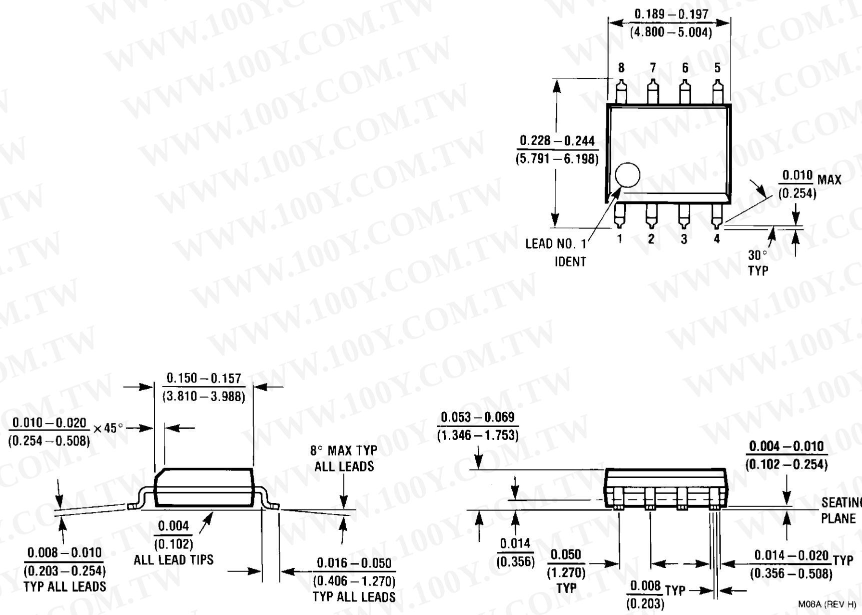
Pitch Pack

A pitch pack is available for the LM7171. The pitch pack contains:

- LM7171 in 8-pin DIP Package
- LM7171 Datasheet
- Pspice Macromodel DIskette With The LM7171 Macromodel
- Amplifier Selection Guide

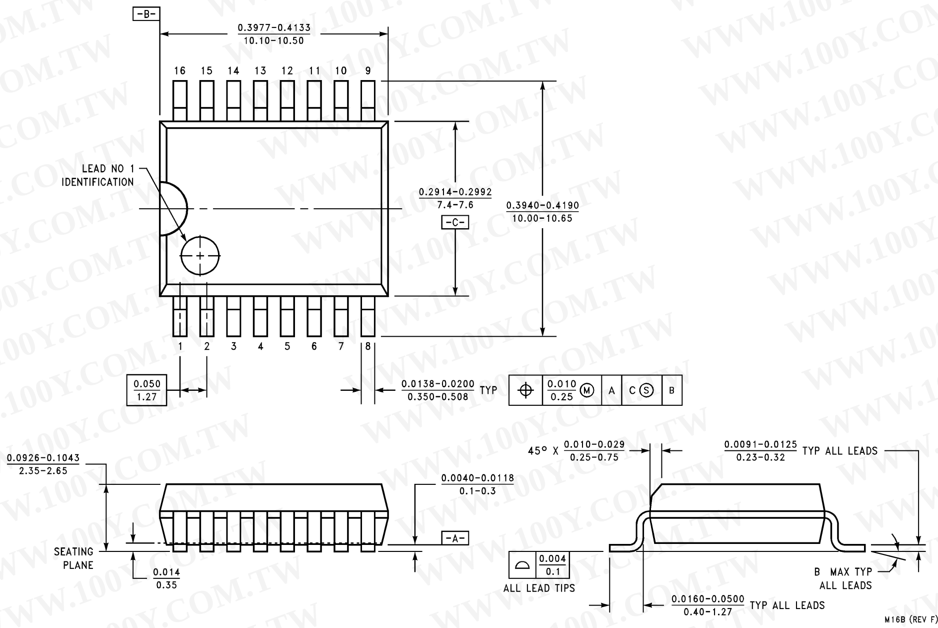
Contact your local National Semiconductor sales office to obtain a pitch pack and design kit.

Physical Dimensions inches (millimeters) unless otherwise noted

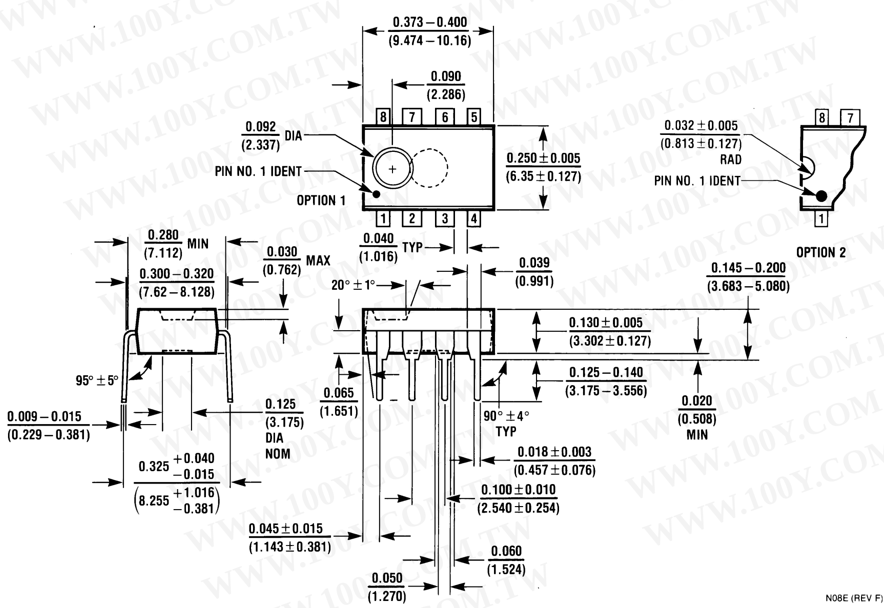


Order Number LM7171AIM, LM7171BIM,
LM7171AIMX or LM7171BIMX
8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Order Number LM7171AIWM, LM7171BIWM, LM7171AIWMX or LM7171BIWMX
16-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16B



Order Number LM7171AIN or LM7171BIN
8-Lead (0.300" Wide) Molded Dual-In-Line Package, JEDEC
NS Package Number N08E

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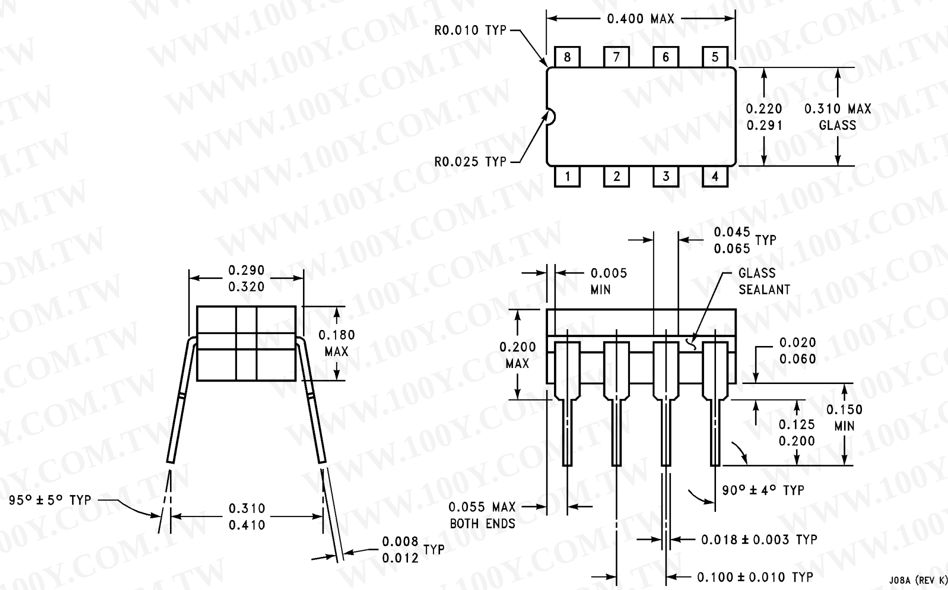

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8-Lead Dual-In-Line Package
NS Package Number J08A
NSID is LM7171AMJ/883

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