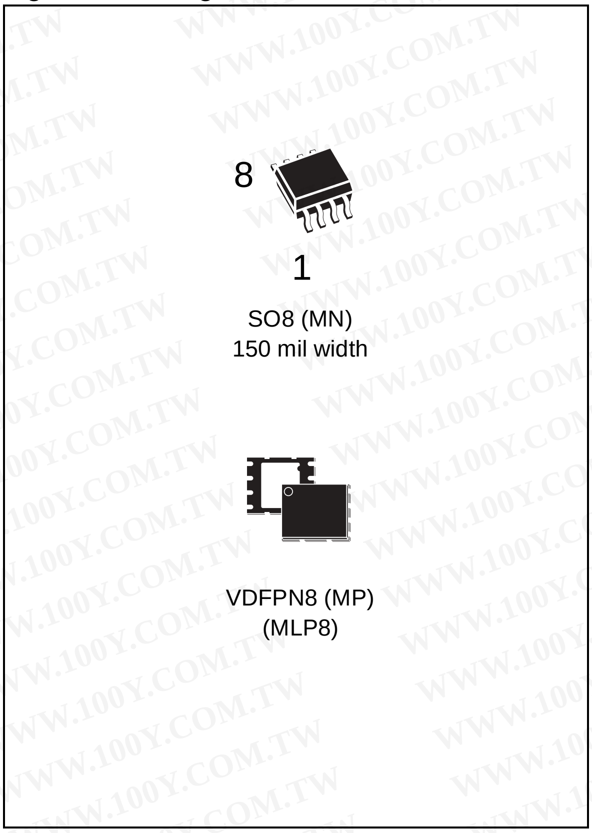
M25P40

4 Mbit, Low Voltage, Serial Flash Memory With 40MHz SPI Bus Interface

FEATURES SUMMARY

- 4 Mbit of Flash Memory
- Page Program (up to 256 Bytes) in 1.5ms (typical)
- Sector Erase (512 Kbit) in 1s (typical)
- Bulk Erase (4 Mbit) in 4.5s (typical)
- 2.7 to 3.6V Single Supply Voltage
- SPI Bus Compatible Serial Interface
- 40MHz Clock Rate (maximum)
- Deep Power-down Mode 1µA (typical)
- Electronic Signature (12h)

Figure 1. Packages



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SUMMARY DESCRIPTION

The M25P40 is a 4 Mbit (512K x 8) Serial Flash Memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The memory is organized as 8 sectors, each containing 256 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 2048 pages, or 524,288 bytes.

The whole memory can be erased using the Bulk Erase instruction, or a sector at a time, using the Sector Erase instruction.

Figure 2. Logic Diagram

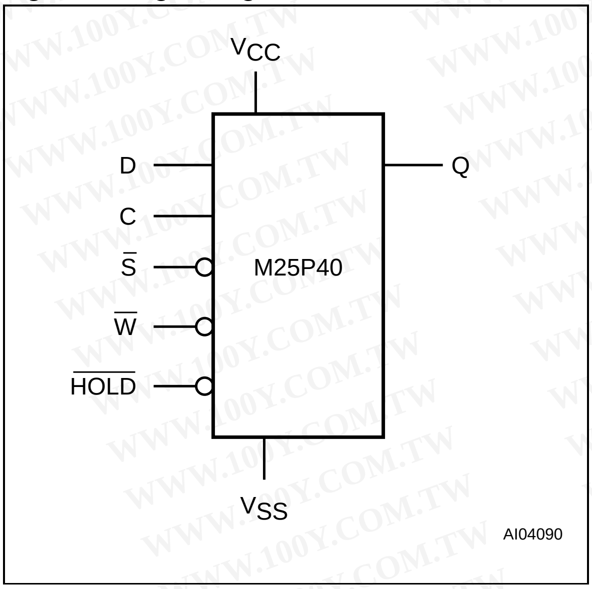
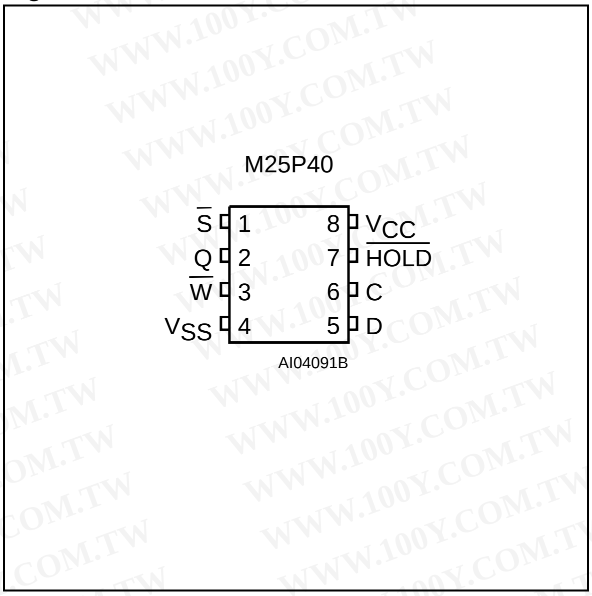


Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 3. SO and VDFPN Connections



Note: 1. There is an exposed die paddle on the underside of the MLP8 package. This is pulled, internally, to V_{SS}, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

SIGNAL DESCRIPTION

Serial Data Output (Q). This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

Serial Data Input (D). This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

Serial Clock (C). This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

Chip Select ($\overline{S}$). When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select ($\overline{S}$) Low enables the device, placing it in the active power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

Hold ($\overline{HOLD}$). The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.

Write Protect ($\overline{W}$). The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP2, BP1 and BP0 bits of the Status Register).

SPI MODES

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

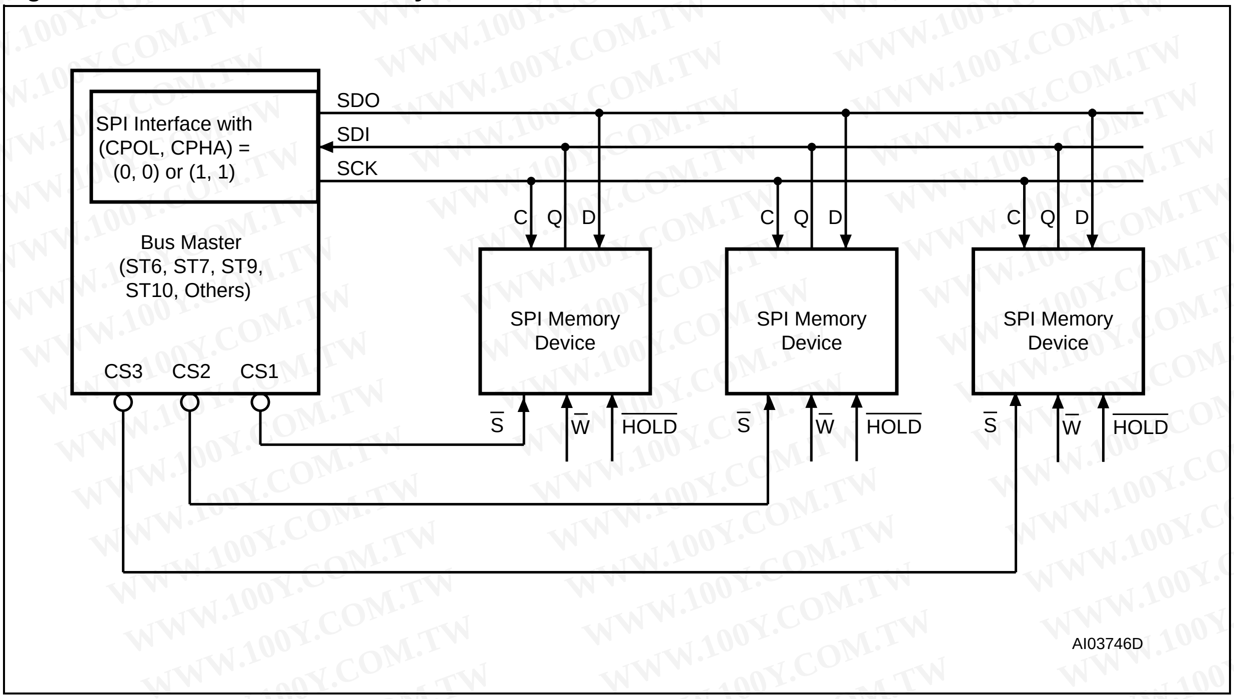
– CPOL=0, CPHA=0
– CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in Figure 5., is the clock polarity when the bus master is in Stand-by mode and not transferring data:

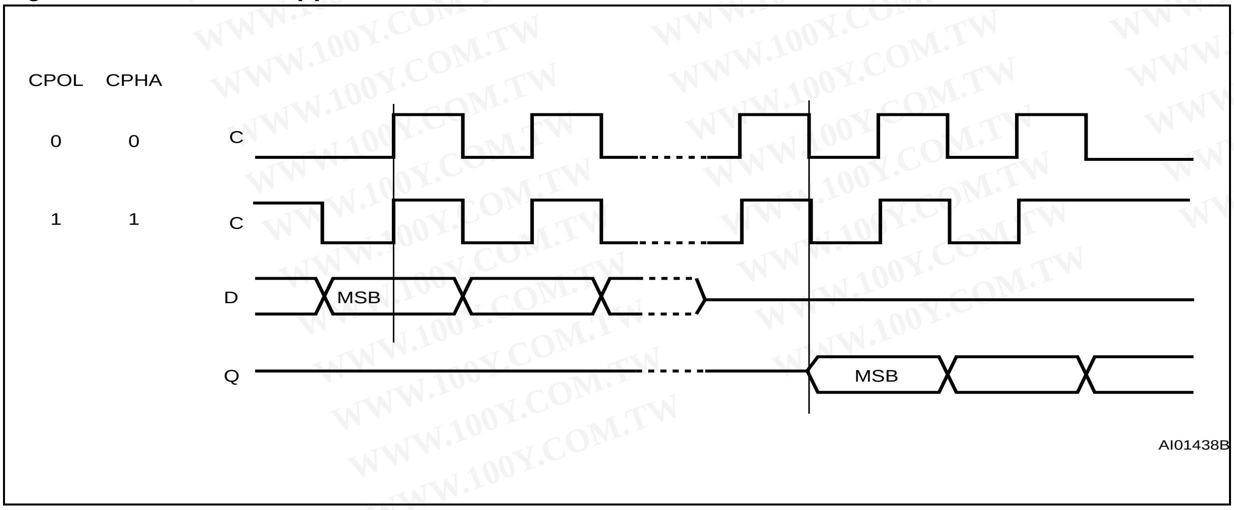
– C remains at 0 for (CPOL=0, CPHA=0)
– C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. Bus Master and Memory Devices on the SPI Bus



Note: The Write Protect (W) and Hold (HOLD) signals should be driven, High or Low as appropriate.

Figure 5. SPI Modes Supported



OPERATING FEATURES

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Sector Erase and Bulk Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a sector at a time, using the Sector Erase (SE) instruction, or throughout the entire memory, using the Bulk Erase (BE) instruction. This starts an internal Erase cycle (of duration t_{SE} or t_{BE}).

The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE or BE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, or t_{BE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select ($\overline{S}$) is Low, the device is enabled, and in the Active Power mode.

When Chip Select ($\overline{S}$) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes in to the Stand-by Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Electronic Signature (RES) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions.

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

SRWD bit. The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits.

Protection Modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M25P40 boasts the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertant changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit . This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Page Program (PP) instruction completion
  - Sector Erase (SE) instruction completion
  - Bulk Erase (BE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect ($\overline{W}$) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Write Disable (SRWD) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertant Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 2. Protected Area Sizes

Status Register Content			Memory Content	
BP2 Bit	**BP1 Bit**	**BP0 Bit**	**Protected Area**	**Unprotected Area**
0	0	0	none	All sectors[1] (eight sectors: 0 to 7)
0	0	1	Upper eighth (Sector 7)	Lower seven-eighths (seven sectors: 0 to 6)
0	1	0	Upper quarter (two sectors: 6 and 7)	Lower three-quarters (six sectors: 0 to 5)
0	1	1	Upper half (four sectors: 4 to 7)	Lower half (four sectors: 0 to 3)
1	0	0	All sectors (eight sectors: 0 to 7)	none
1	0	1	All sectors (eight sectors: 0 to 7)	none
1	1	0	All sectors (eight sectors: 0 to 7)	none
1	1	1	All sectors (eight sectors: 0 to 7)	none

Note: 1. The device is ready to accept a Bulk Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) are 0.

Hold Condition

The Hold (HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select (S) Low.

The Hold condition starts on the falling edge of the Hold (HOLD) signal, provided that this coincides with Serial Clock (C) being Low (as shown in Figure 6.).

The Hold condition ends on the rising edge of the Hold (HOLD) signal, provided that this coincides with Serial Clock (C) being Low.

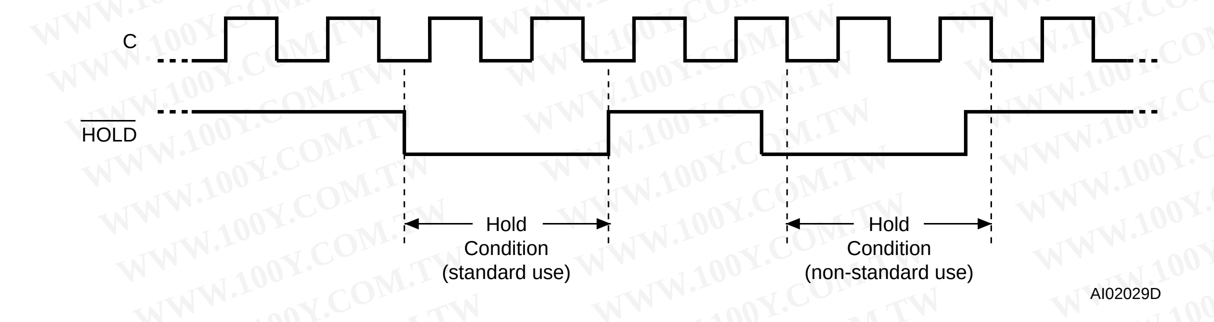
If the falling edge does not coincide with Serial Clock (C) being Low, the Hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the Hold condition ends after Serial Clock (C) next goes Low. (This is shown in Figure 6.).

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

Normally, the device is kept selected, with Chip Select (S) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (S) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD) High, and then to drive Chip Select (S) Low. This prevents the device from going back to the Hold condition.

Figure 6. Hold Condition Activation



MEMORY ORGANIZATION

The memory is organized as:

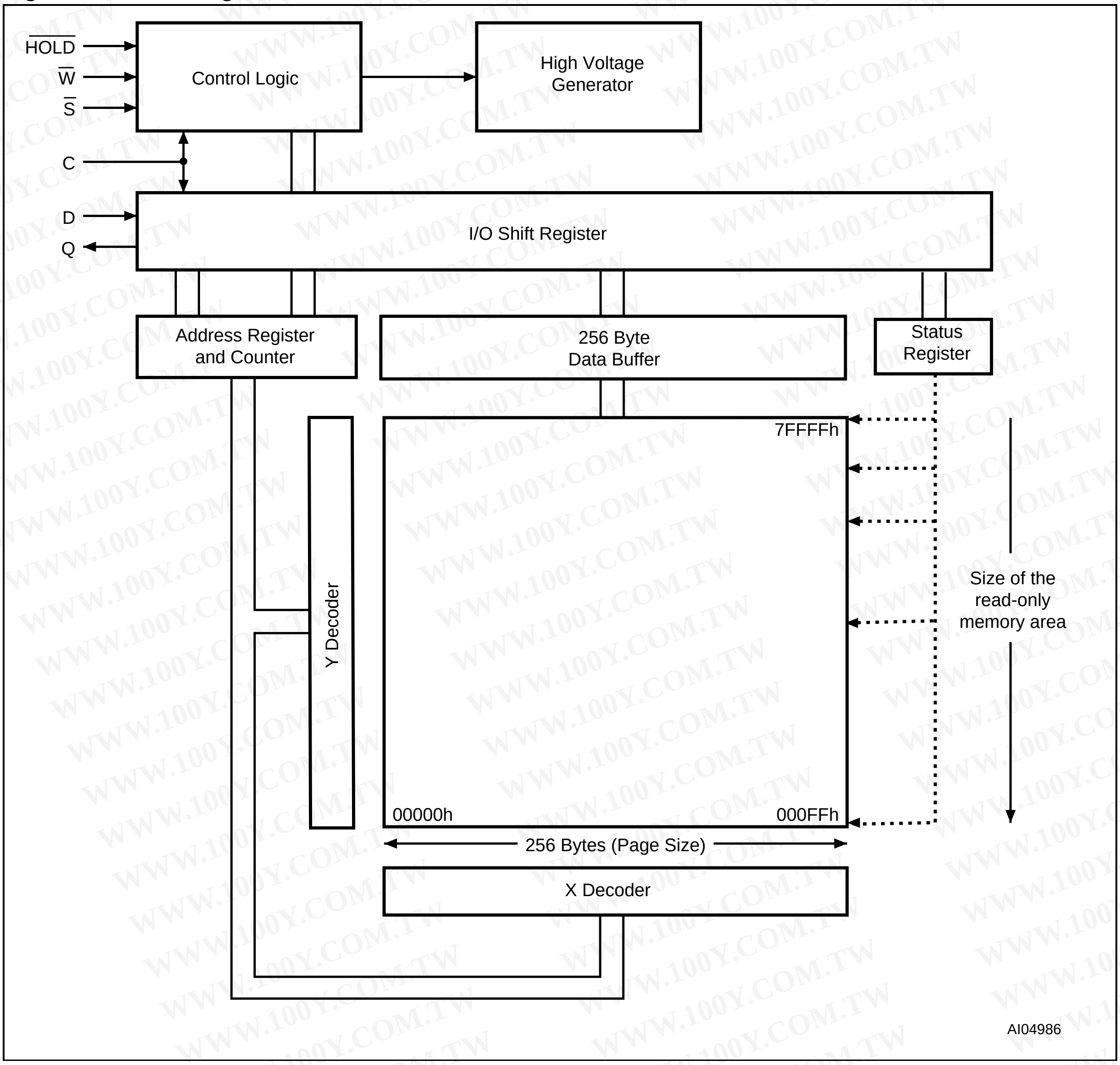
- 524,288 bytes (8 bits each)
- 8 sectors (512 Kbits, 65536 bytes each)
- 2048 pages (256 bytes each).

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector or Bulk Erasable (bits are erased from 0 to 1) but not Page Erasable.

Table 3. Memory Organization

Sector	Address Range	
7	70000h	7FFFFh
6	60000h	6FFFFh
5	50000h	5FFFFh
4	40000h	4FFFFh
3	30000h	3FFFFh
2	20000h	2FFFFh
1	10000h	1FFFFh
0	00000h	0FFFFh

Figure 7. Block Diagram



INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in Table 4..

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select ($\overline{S}$) must be driven High after the last bit of the instruction sequence has been shifted in.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Read Status Register (RDSR) or Release from Deep Power-down, and Read Electronic Signature (RES) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4. Instruction Set

Instruction	Description	One-byte Instruction Code		Address Bytes	Dummy Bytes	Data Bytes
WREN	Write Enable	0000 0110	06h	0	0	0
WRDI	Write Disable	0000 0100	04h	0	0	0
RDSR	Read Status Register	0000 0101	05h	0	0	1 to ∞
WRSR	Write Status Register	0000 0001	01h	0	0	1
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0Bh	3	1	1 to ∞
PP	Page Program	0000 0010	02h	3	0	1 to 256
SE	Sector Erase	1101 1000	D8h	3	0	0
BE	Bulk Erase	1100 0111	C7h	0	0	0
DP	Deep Power-down	1011 1001	B9h	0	0	0
RES	Release from Deep Power-down, and Read Electronic Signature	1010 1011	ABh	0	3	1 to ∞
	Release from Deep Power-down			0	0	0

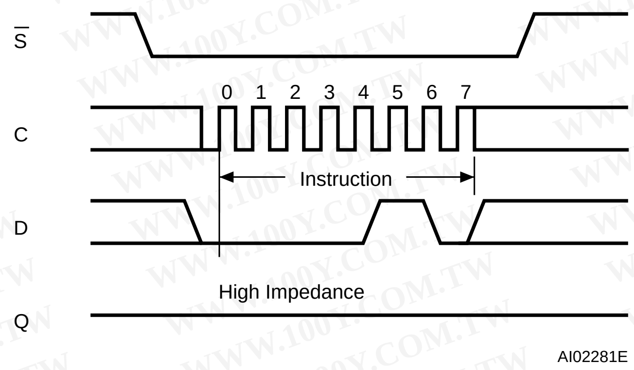
Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 8.) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select (S̄) Low, sending the instruction code, and then driving Chip Select (S̄) High.

Figure 8. Write Enable (WREN) Instruction Sequence



Write Disable (WRDI)

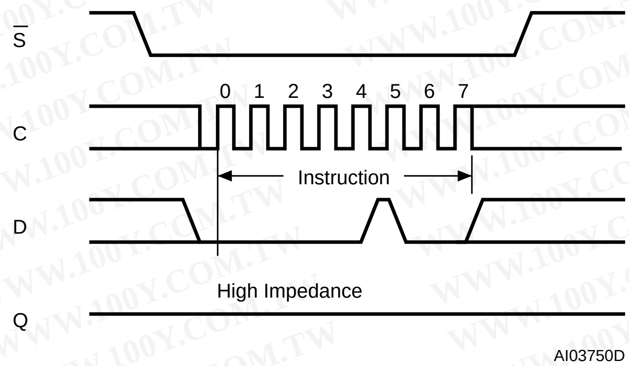
The Write Disable (WRDI) instruction (Figure 9.) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select (S̄) Low, sending the instruction code, and then driving Chip Select (S̄) High.

The Write Enable Latch (WEL) bit is reset under the following conditions:

– Power-up
– Write Disable (WRDI) instruction completion
– Write Status Register (WRSR) instruction completion
– Page Program (PP) instruction completion
– Sector Erase (SE) instruction completion
– Bulk Erase (BE) instruction completion

Figure 9. Write Disable (WRDI) Instruction Sequence



Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 10..

Table 5. Status Register Format

b7							b0
SRWD	0	0	BP2	BP1	BP0	WEL	WIP

- SRWD: Status Register Write Protect
- BP2, BP1, BP0: Block Protect Bits
- WEL: Write Enable Latch Bit
- WIP: Write In Progress Bit

The status and control bits of the Status Register are as follows:

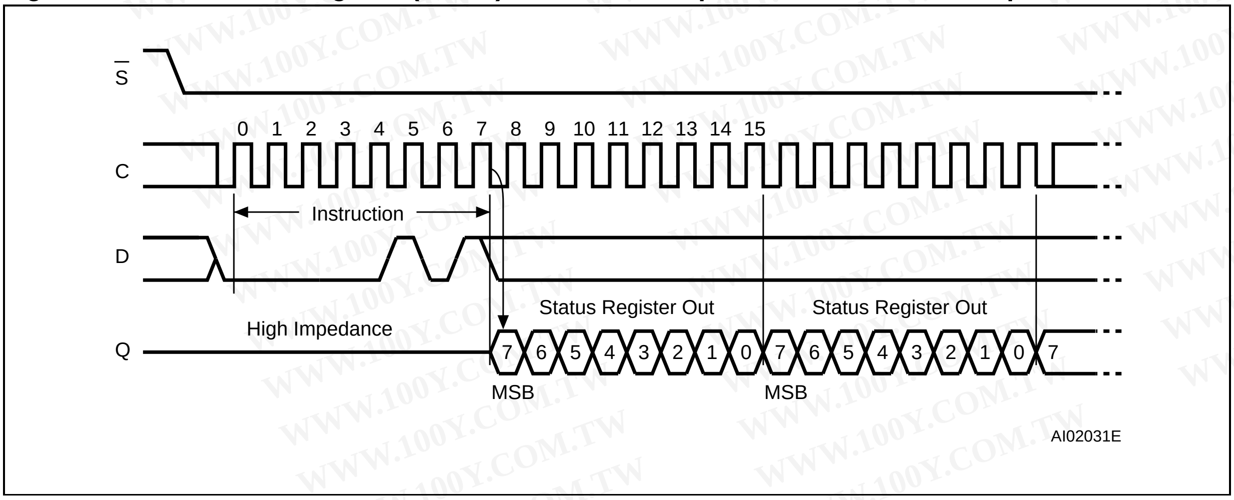
WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 2.) becomes protected against Page Program (PP) and Sector Erase (SE) instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Bulk Erase (BE) instruction is executed if, and only if, both Block Protect (BP2, BP1, BP0) bits are 0.

SRWD bit. The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Figure 10. Read Status Register (RDSR) Instruction Sequence and Data-Out Sequence



Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (S̅) Low, followed by the instruction code and the data byte on Serial Data Input (D).

The instruction sequence is shown in Figure 11..

The Write Status Register (WRSR) instruction has no effect on b6, b5, b1 and b0 of the Status Register. b6 and b5 are always read as 0.

Chip Select (S̅) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (S̅) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 2.. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect (W̅) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W̅) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

Figure 11. Write Status Register (WRSR) Instruction Sequence

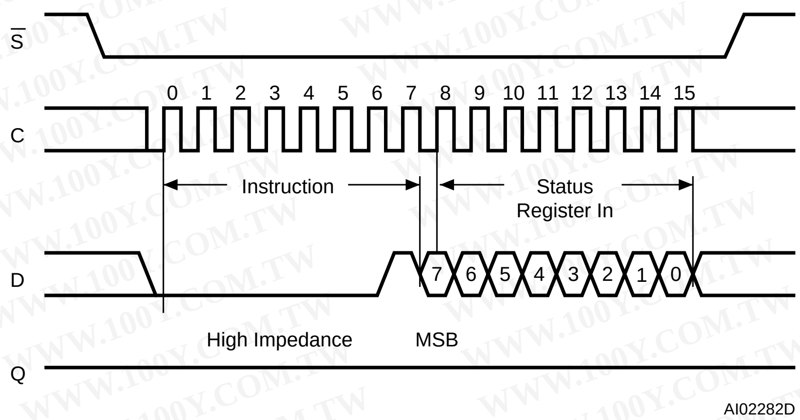


Table 6. Protection Modes

$\overline{W}$ Signal	SRWD Bit	Mode	Write Protection of the Status Register	Memory Content	
				Protected Area[1]	Unprotected Area[1]
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the SRWD, BP2, BP1 and BP0 bits can be changed	Protected against Page Program, Sector Erase and Bulk Erase	Ready to accept Page Program and Sector Erase instructions
0	0				
1	1				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the SRWD, BP2, BP1 and BP0 bits cannot be changed	Protected against Page Program, Sector Erase and Bulk Erase	Ready to accept Page Program and Sector Erase instructions

Note: 1. As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in Table 2..

The protection features of the device are summarized in Table 6..

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect ($\overline{W}$) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

– If Write Protect ($\overline{W}$) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.

– If Write Protect ($\overline{W}$) is driven Low, it is *not* possible to write to the Status Register *even* if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP2, BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

– by setting the Status Register Write Disable (SRWD) bit after driving Write Protect ($\overline{W}$) Low

– or by driving Write Protect ($\overline{W}$) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect ($\overline{W}$) High.

If Write Protect ($\overline{W}$) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP2, BP1, BP0) bits of the Status Register, can be used.

Read Data Bytes (READ)

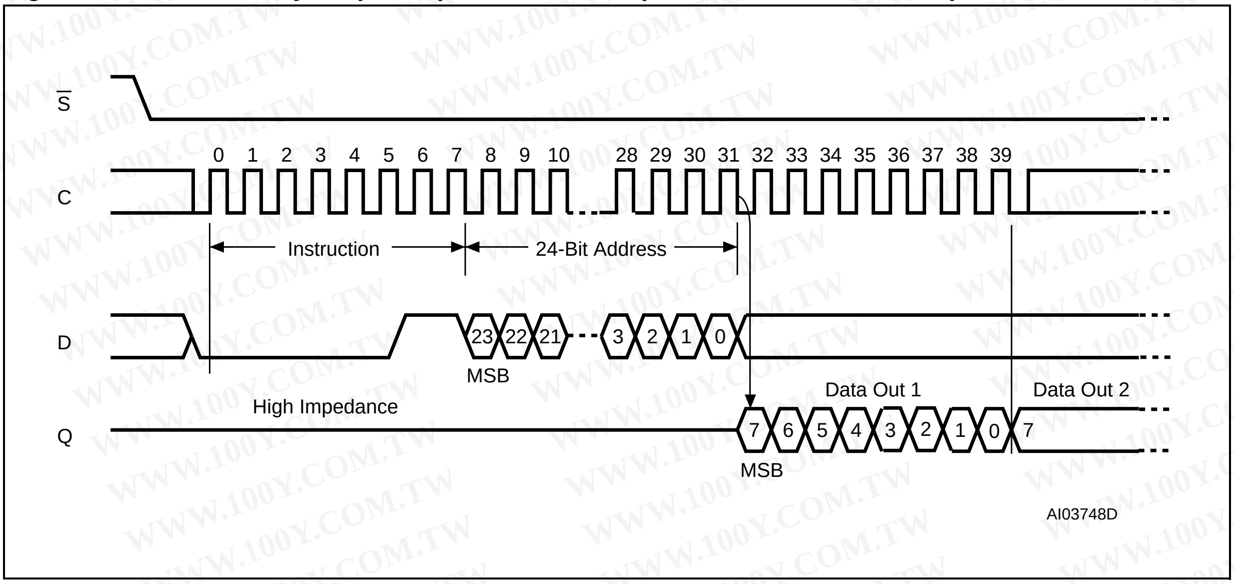
The device is first selected by driving Chip Select (S̅) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 12..

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (S̅) High. Chip Select (S̅) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 12. Read Data Bytes (READ) Instruction Sequence and Data-Out Sequence



Note: 1. Address bits A23 to A19 are Don't Care.

Read Data Bytes at Higher Speed (FAST_READ)

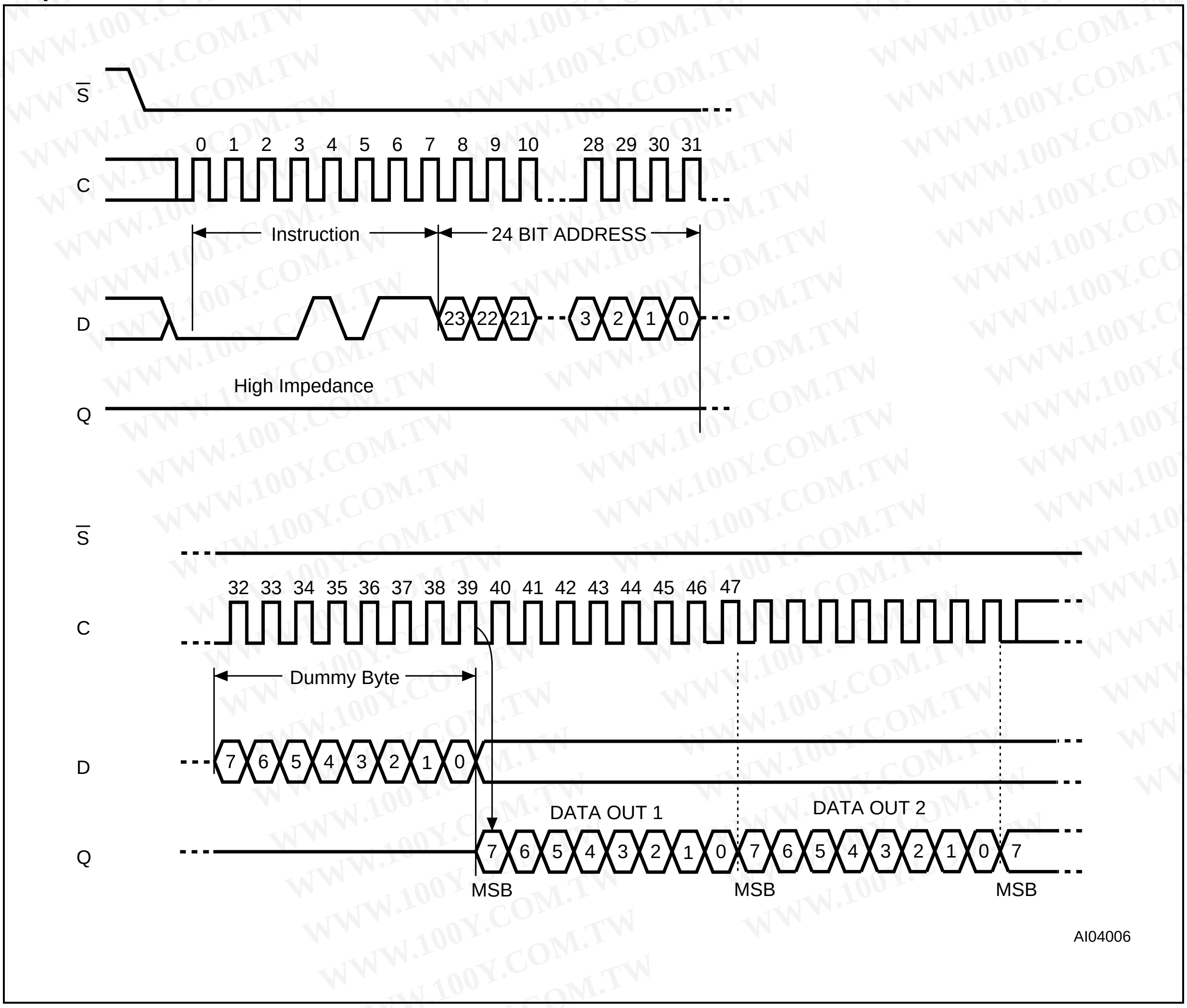
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 13..

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 13. Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence and Data-Out Sequence



Note: 1. Address bits A23 to A19 are Don't Care.

Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (D). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 14..

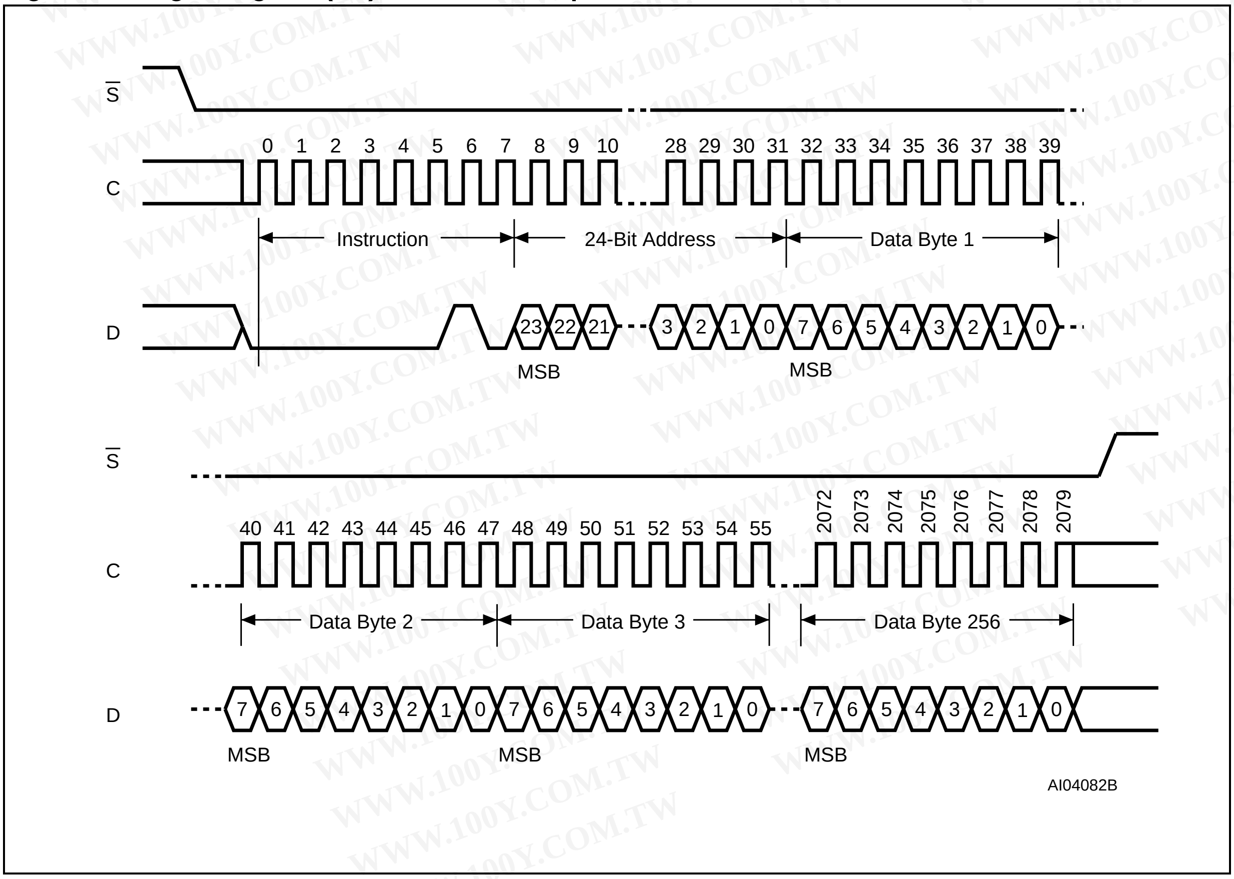
If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3. and Table 2.) is not executed.

Figure 14. Page Program (PP) Instruction Sequence



Note: 1. Address bits A23 to A19 are Don't Care.

Sector Erase (SE)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

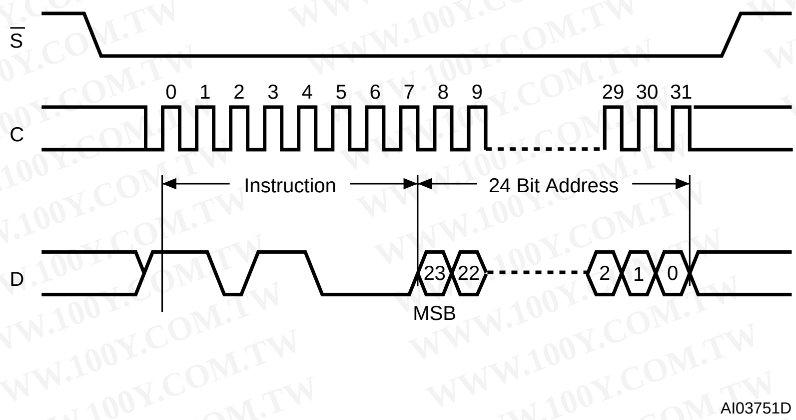
The Sector Erase (SE) instruction is entered by driving Chip Select (S̅) Low, followed by the instruction code, and three address bytes on Serial Data Input (D). Any address inside the Sector (see Table 3.) is a valid address for the Sector Erase (SE) instruction. Chip Select (S̅) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 15..

Chip Select (S̅) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (S̅) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3. and Table 2.) is not executed.

Figure 15. Sector Erase (SE) Instruction Sequence



Note: 1. Address bits A23 to A19 are Don't Care.

Bulk Erase (BE)

The Bulk Erase (BE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

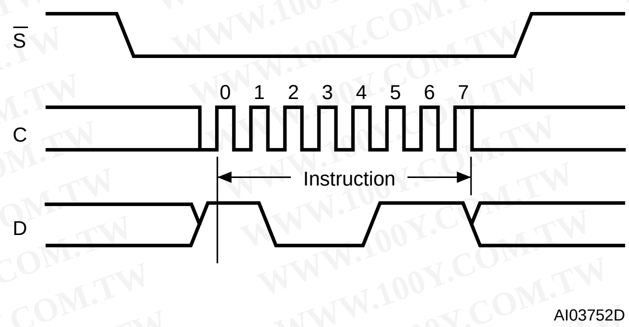
The Bulk Erase (BE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 16..

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Bulk Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Bulk Erase cycle (whose duration is t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Bulk Erase (BE) instruction is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Bulk Erase (BE) instruction is ignored if one, or more, sectors are protected.

Figure 16. Bulk Erase (BE) Instruction Sequence



Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in Table 12.).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Electronic Signature (RES) instruction also allows the Electronic Signature of the device to be output on Serial Data Output (Q).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode.

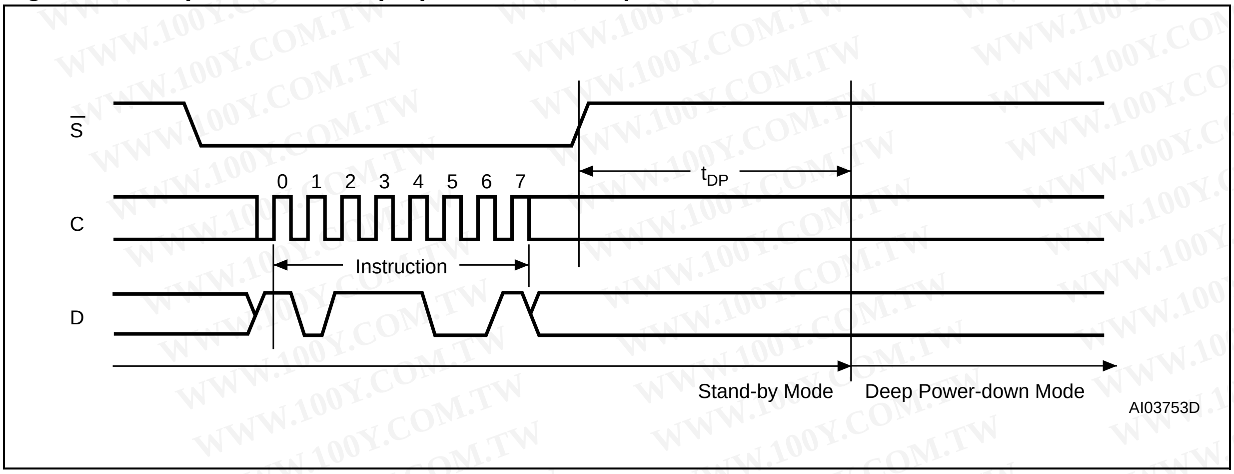
The Deep Power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 17..

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 17. Deep Power-down (DP) Instruction Sequence



Release from Deep Power-down and Read Electronic Signature (RES)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

The instruction can also be used to read, on Serial Data Output (Q), the 8-bit Electronic Signature, whose value for the *M25P40* is *12h*.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Electronic Signature (RES) instruction always provides access to the 8-bit Electronic Signature of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Electronic Signature (RES) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

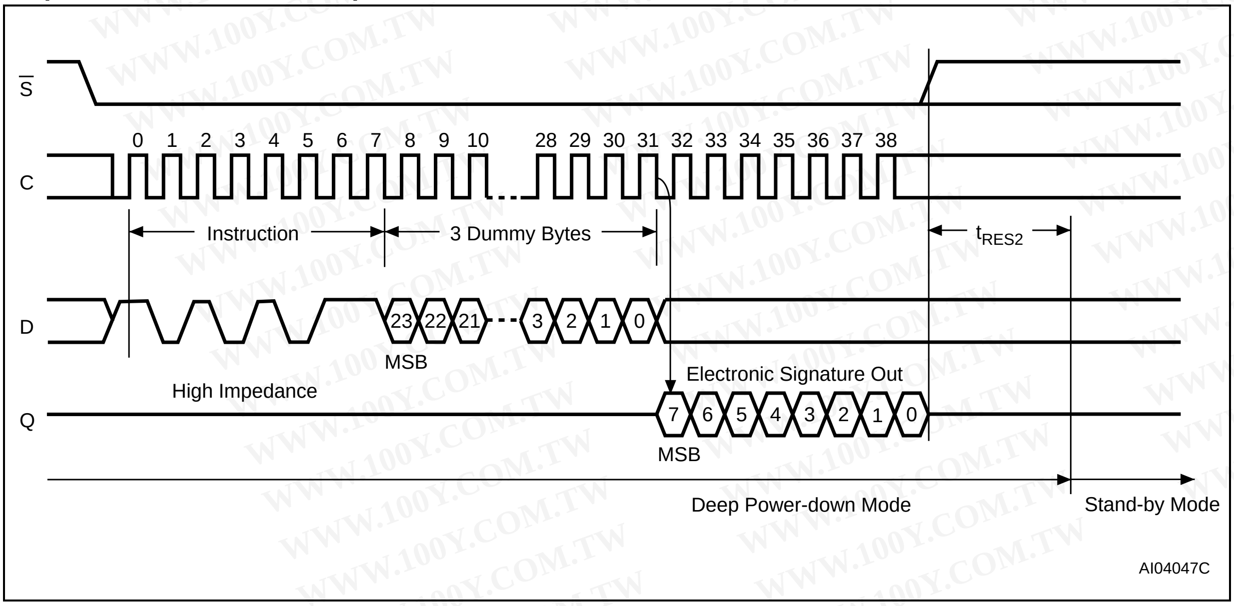
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code is followed by 3 dummy bytes, each bit being latched-in on Serial Data Input (D) during the rising edge of Serial Clock (C). Then, the 8-bit Electronic Signature, stored in the memory, is shifted out on Serial Data Output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 18..

The Release from Deep Power-down and Read Electronic Signature (RES) instruction is terminated by driving Chip Select ($\overline{S}$) High after the Electronic Signature has been read at least once. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the Electronic Signature to be output repeatedly.

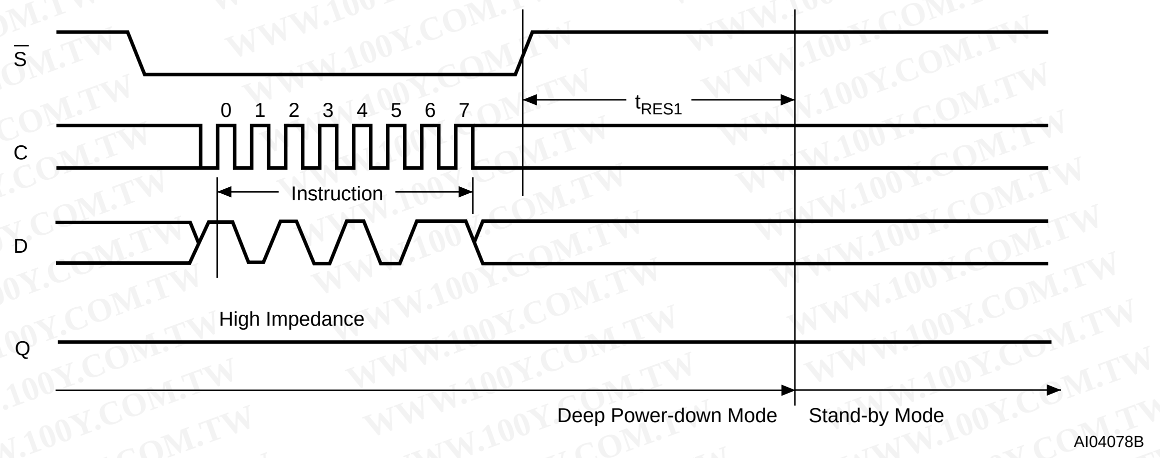
When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES2}, and Chip Select ($\overline{S}$) must remain High for at least t_{RES2}(max), as specified in Table 17.. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 18. Release from Deep Power-down and Read Electronic Signature (RES) Instruction Sequence and Data-Out Sequence



Note: The value of the 8-bit Electronic Signature, for the M25P40, is 12h.

Figure 19. Release from Deep Power-down (RES) Instruction Sequence



Driving Chip Select ($\overline{S}$) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit Electronic Signature has been transmitted for the first time (as shown in Figure 19.), still insures that the device is put into Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES1}, and Chip Select ($\overline{S}$) must remain High for at least t_{RES1}(max), as specified in Table 17.. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

– V_{CC}(min) at Power-up, and then for a further delay of t_{VSL}
– V_{SS} at Power-down

Usually a simple pull-up resistor on Chip Select ($\overline{S}$) can be used to insure safe and proper Power-up and Power-down.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the POR threshold value, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No Write Status Register, Program or Erase instructions should be sent until the later of:

– t_{PUW} after V_{CC} passed the V_{WI} threshold
– t_{VSL} after V_{CC} passed the V_{CC}(min) level

These values are specified in Table 7..

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for READ instructions even if the t_{PUW} delay is not yet fully elapsed.

At Power-up, the device is in the following state:

– The device is in the Standby mode (not the Deep Power-down mode).
– The Write Enable Latch (WEL) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} feed. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 0.1µF).

At Power-down, when V_{CC} drops from the operating voltage, to below the POR threshold value, V_{WI}, all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

Figure 20. Power-up Timing

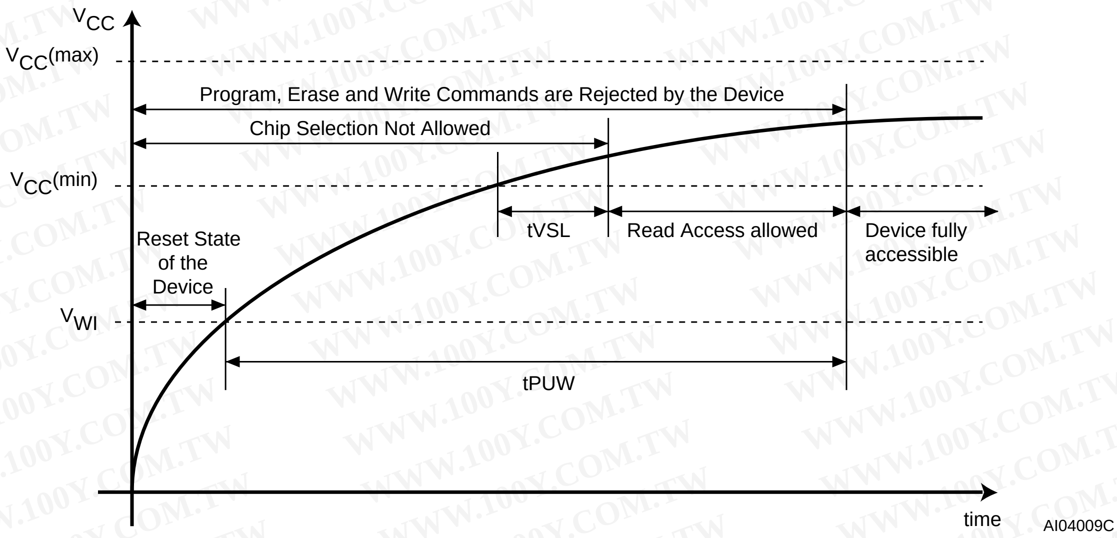


Table 7. Power-Up Timing and V_{WI} Threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL} [1]	V_{CC}(min) to $\overline{S}$ low	10		µs
t_{PUW} [1]	Time delay to Write instruction	1	10	ms
V_{WI} [1]	Write Inhibit Voltage	1	2	V

Note: 1. These parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	See note [1]		°C
V_{IO}	Input and Output Voltage (with respect to Ground)	–0.6	4.0	V
V_{CC}	Supply Voltage	–0.6	4.0	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	–2000	2000	V

Note: 1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 9. Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	

Table 10. Data Retention and Endurance

Parameter	Condition	Min.	Max.	Unit
Erase/Program Cycles	Device Grade 6		100 000	cycles per sector
	Device Grade 3 [1]		10 000	
Data Retention	Device Grade 6		20	years
	Device Grade 3 [1] (at 85°C)		20	

Note: 1. This is preliminary data

Table 11. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance (other pins)	V_{IN} = 0V		6	pF

Note: Sampled only, not 100% tested, at T_A=25°C and a frequency of 20MHz.

Table 12. DC Characteristics (Device Grade 6)

Symbol	Parameter	Test Condition (in addition to those in Table 9.)	Min.	Max.	Unit
I_{LI}	Input Leakage Current			± 2	µA
I_{LO}	Output Leakage Current			± 2	µA
I_{CC1}	Standby Current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		50	µA
I_{CC2}	Deep Power-down Current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		10	µA
I_{CC3}	Operating Current (READ)	C = $0.1V_{CC}$ / $0.9.V_{CC}$ at 40MHz, Q = open		8	mA
		C = $0.1V_{CC}$ / $0.9.V_{CC}$ at 20MHz, Q = open		4	mA
I_{CC4}	Operating Current (PP)	$\overline{S} = V_{CC}$		15	mA
I_{CC5}	Operating Current (WRSR)	$\overline{S} = V_{CC}$		15	mA
I_{CC6}	Operating Current (SE)	$\overline{S} = V_{CC}$		15	mA
I_{CC7}	Operating Current (BE)	$\overline{S} = V_{CC}$		15	mA
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.7V_{CC}$	$V_{CC}+0.4$	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	$V_{CC}–0.2$		V

Table 13. DC Characteristics (Device Grade 3)

Symbol	Parameter	Test Condition (in addition to those in Table 9.)	Min.[1]	Max.[1]	Unit
I_{LI}	Input Leakage Current			± 2	µA
I_{LO}	Output Leakage Current			± 2	µA
I_{CC1}	Standby Current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		100	µA
I_{CC2}	Deep Power-down Current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		50	µA
I_{CC3}	Operating Current (READ)	C = $0.1V_{CC}$ / $0.9.V_{CC}$ at 40MHz, Q = open		8	mA
		C = $0.1V_{CC}$ / $0.9.V_{CC}$ at 20MHz, Q = open		4	mA
I_{CC4}	Operating Current (PP)	$\overline{S} = V_{CC}$		15	mA
I_{CC5}	Operating Current (WRSR)	$\overline{S} = V_{CC}$		15	mA
I_{CC6}	Operating Current (SE)	$\overline{S} = V_{CC}$		15	mA
I_{CC7}	Operating Current (BE)	$\overline{S} = V_{CC}$		15	mA
V_{IL}	Input Low Voltage		– 0.5	$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.7V_{CC}$	$V_{CC}+0.4$	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	$V_{CC}–0.2$		V

Note: 1. This is preliminary data

Table 14. Instruction Times (Device Grade 6)

Test conditions specified in Table 9. and Table 16.						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
t_W		Write Status Register Cycle Time		5	15	ms
t_{PP}		Page Program Cycle Time		1.4	5	ms
t_{SE}		Sector Erase Cycle Time		1	3	s
t_{BE}		Bulk Erase Cycle Time		4.5	10	s

Table 15. Instruction Times (Device Grade 3)

Test conditions specified in Table 9. and Table 16.						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.**[1,2]	**Max.**[2]	**Unit**
t_W		Write Status Register Cycle Time		8	15	ms
t_{PP}		Page Program Cycle Time		1.5	5	ms
t_{SE}		Sector Erase Cycle Time		1	3	s
t_{BE}		Bulk Erase Cycle Time		4.5	10	s

Note: 1. At 85°C
2. This is preliminary data

Table 16. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output Timing Reference Voltages	V_{CC} / 2		V

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Figure 21. AC Measurement I/O Waveform

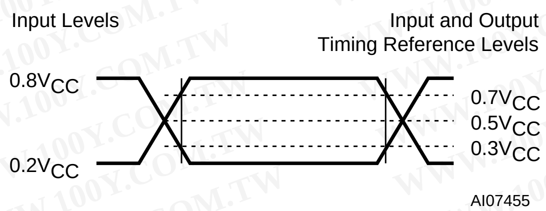


Table 17. AC Characteristics (25MHz Operation, Device Grade 6 or 3)

Test conditions specified in Table 9. and Table 16.						
Symbol	**Alt.**	**Parameter**	**Min.**[5]	**Typ.**	**Max.**[5]	**Unit**
f_C	f_C	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.		25	MHz
f_R		Clock Frequency for READ instructions	D.C.		20	MHz
t_{CH} [1]	t_{CLH}	Clock High Time	18			ns
t_{CL} [1]	t_{CLL}	Clock Low Time	18			ns
t_{CLCH} [2]		Clock Rise Time[3] (peak to peak)	0.1			V/ns
t_{CHCL} [2]		Clock Fall Time[3] (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time (relative to C)	10			ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time (relative to C)	10			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	5			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{CHSH}		$\overline{S}$ Active Hold Time (relative to C)	10			ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time (relative to C)	10			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	100			ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time			15	ns
t_{CLQV}	t_V	Clock Low to Output Valid			15	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{HLCH}		$\overline{HOLD}$ Setup Time (relative to C)	10			ns
t_{CHHH}		$\overline{HOLD}$ Hold Time (relative to C)	10			ns
t_{HHCH}		HOLD Setup Time (relative to C)	10			ns
t_{CHHL}		HOLD Hold Time (relative to C)	10			ns
t_{HHQX} [2]	t_{LZ}	HOLD to Output Low-Z			15	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ to Output High-Z			20	ns
t_{WHSL} [4]		Write Protect Setup Time	20			ns
t_{SHWL} [4]		Write Protect Hold Time	100			ns
t_{DP} [2]		$\overline{S}$ High to Deep Power-down Mode			3	µs
t_{RES1} [2]		$\overline{S}$ High to Standby Mode without Electronic Signature Read			3	µs
t_{RES2} [2]		$\overline{S}$ High to Standby Mode with Electronic Signature Read			1.8	µs

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/f_C$
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. For device grade 3, this is Preliminary Data

Table 18. AC Characteristics (40MHz Operation, Device Grade 6)

40MHz available for products marked since week 20 of 2004, only[5] Test conditions specified in Table 9. and Table 16.						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
f_C	f_C	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.		40	MHz
f_R		Clock Frequency for READ instructions	D.C.		20	MHz
t_{CH} [1]	t_{CLH}	Clock High Time	11			ns
t_{CL} [1]	t_{CLL}	Clock Low Time	11			ns
t_{CLCH} [2]		Clock Rise Time[3] (peak to peak)	0.1			V/ns
t_{CHCL} [2]		Clock Fall Time[3] (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{CHSH}		$\overline{S}$ Active Hold Time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	100			ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time			9	ns
t_{CLQV}	t_V	Clock Low to Output Valid			9	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{HLCH}		$\overline{HOLD}$ Setup Time (relative to C)	5			ns
t_{CHHH}		$\overline{HOLD}$ Hold Time (relative to C)	5			ns
t_{HHCH}		HOLD Setup Time (relative to C)	5			ns
t_{CHHL}		HOLD Hold Time (relative to C)	5			ns
t_{HHQX} [2]	t_{LZ}	HOLD to Output Low-Z			9	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ to Output High-Z			9	ns
t_{WHSL} [4]		Write Protect Setup Time	20			ns
t_{SHWL} [4]		Write Protect Hold Time	100			ns
t_{DP} [2]		$\overline{S}$ High to Deep Power-down Mode			3	µs
t_{RES1} [2]		$\overline{S}$ High to Standby Mode without Electronic Signature Read			3	µs
t_{RES2} [2]		$\overline{S}$ High to Standby Mode with Electronic Signature Read			1.8	µs

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/f_C$
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. Details of how to find the date of marking are given in Application Note, *AN1995*.

Figure 22. Serial Input Timing

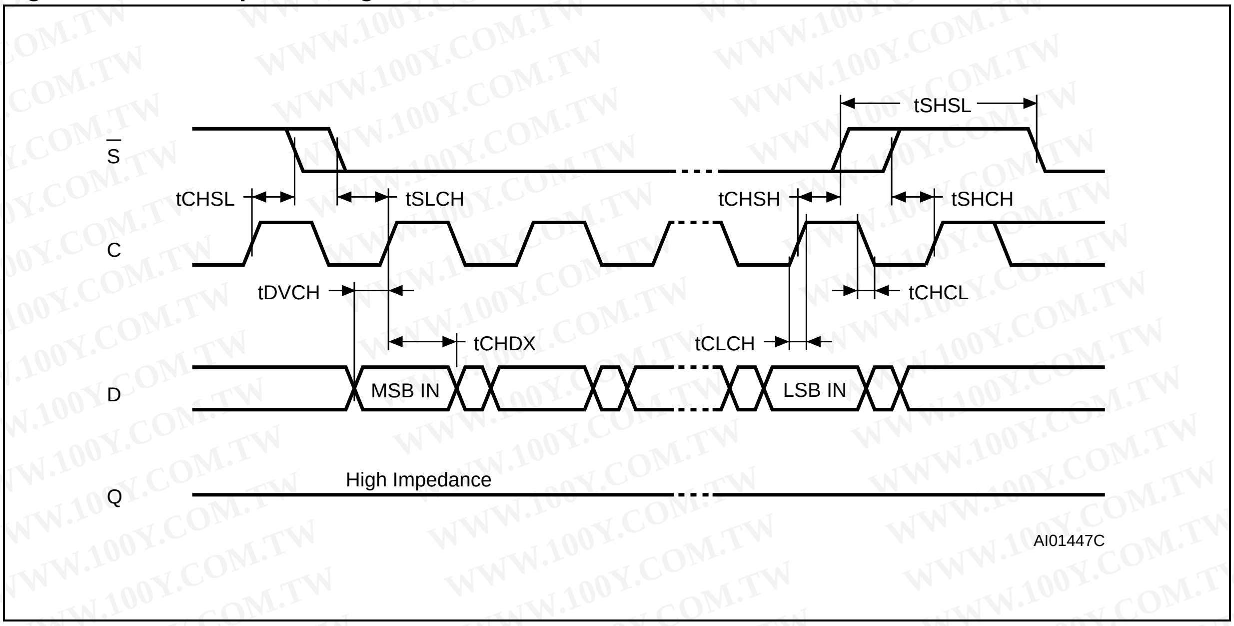


Figure 23. Write Protect Setup and Hold Timing during WRSR when SRWD=1

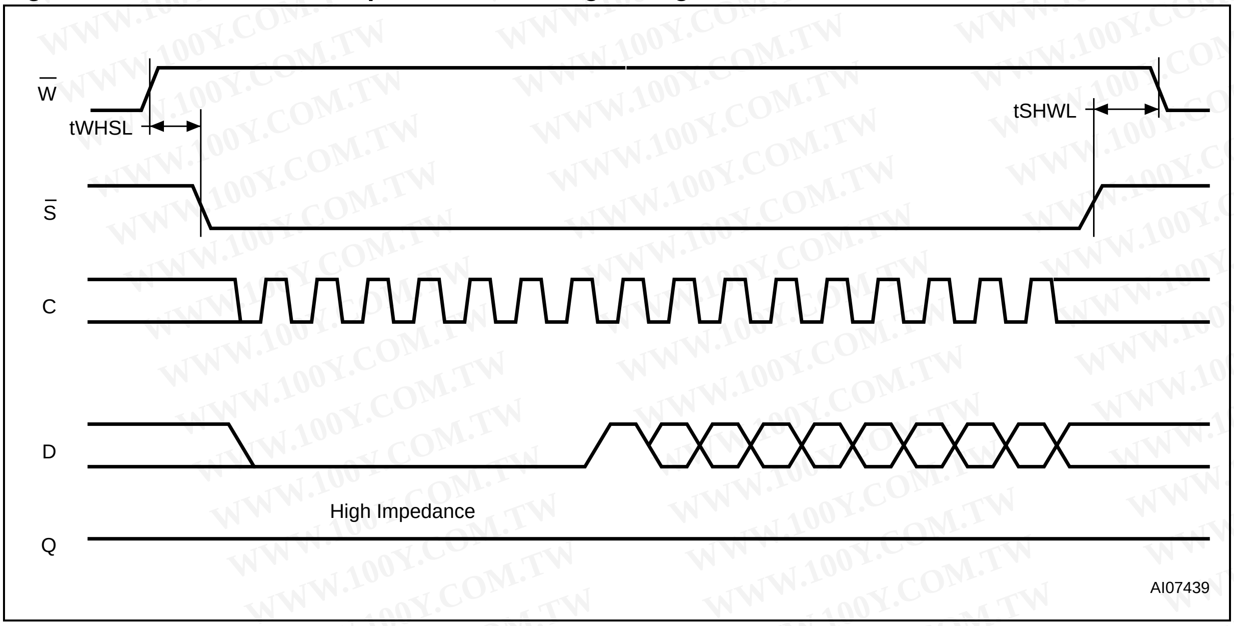


Figure 24. Hold Timing

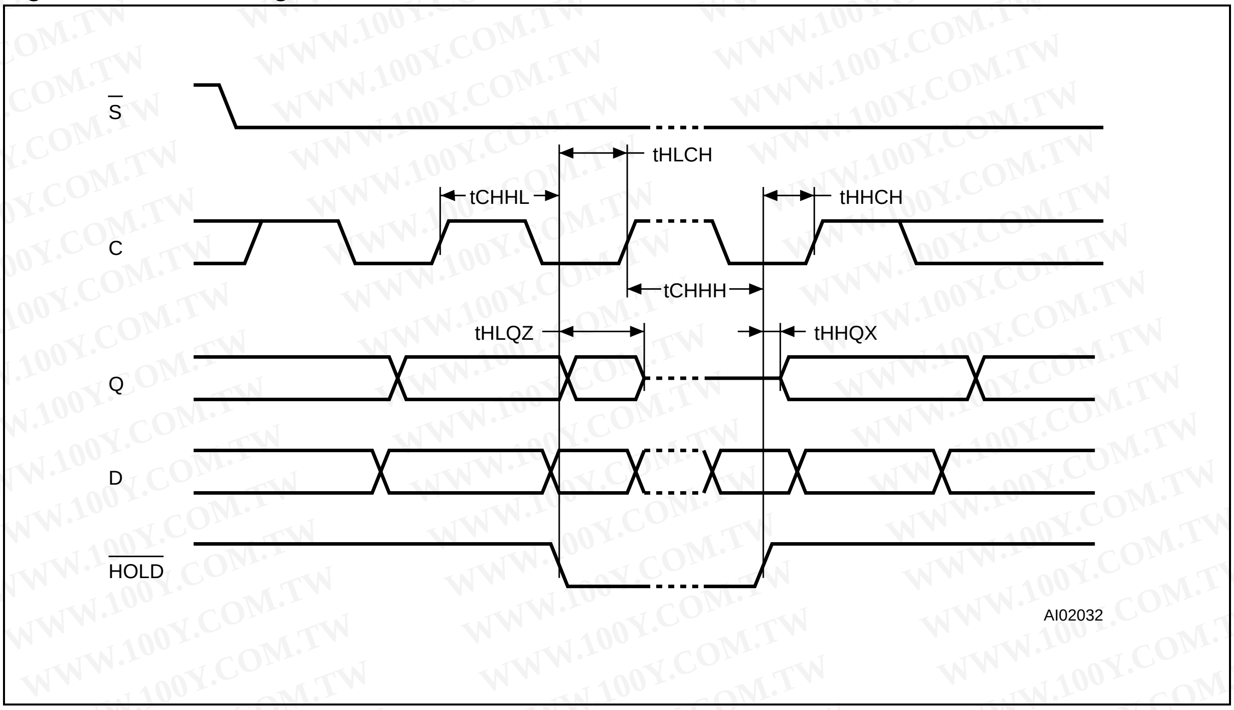
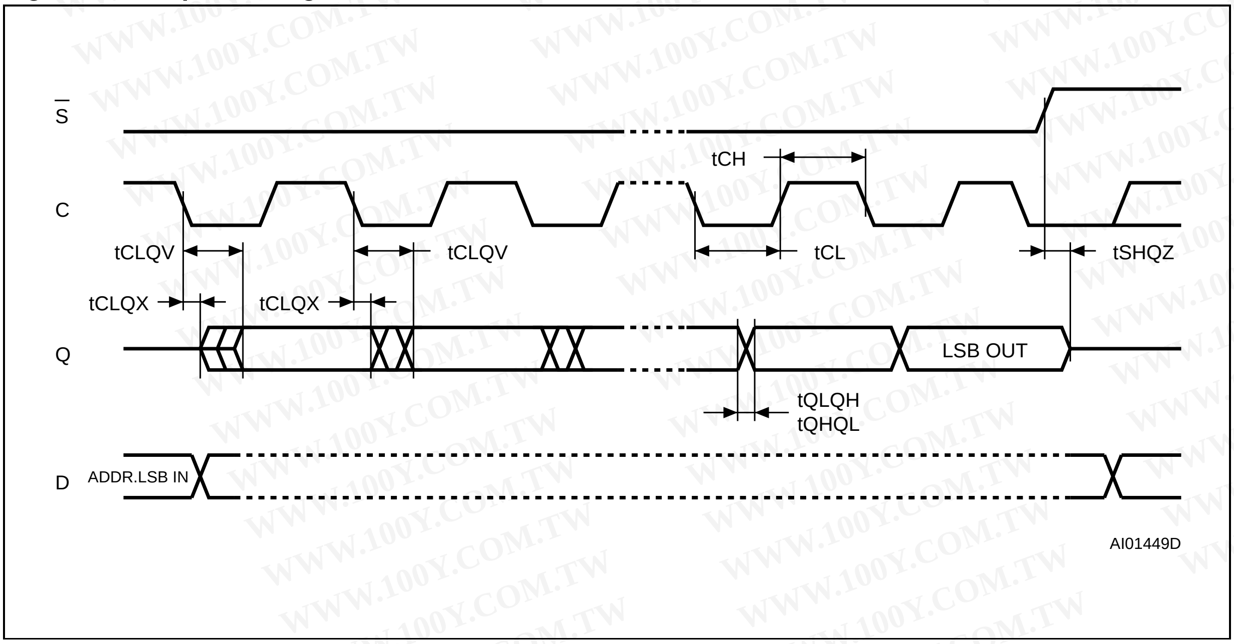
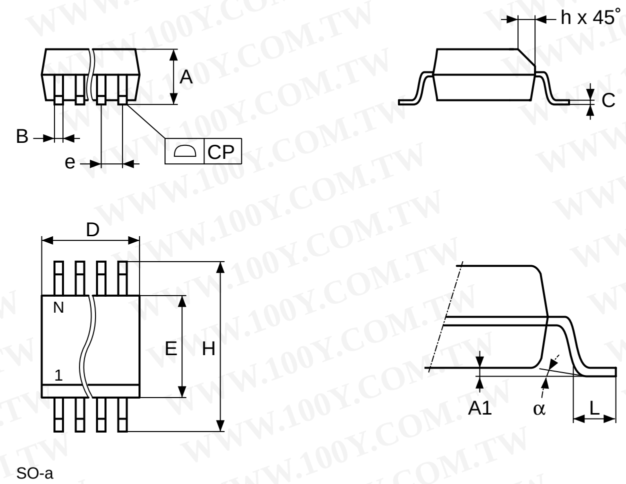


Figure 25. Output Timing



PACKAGE MECHANICAL

Figure 26. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Outline

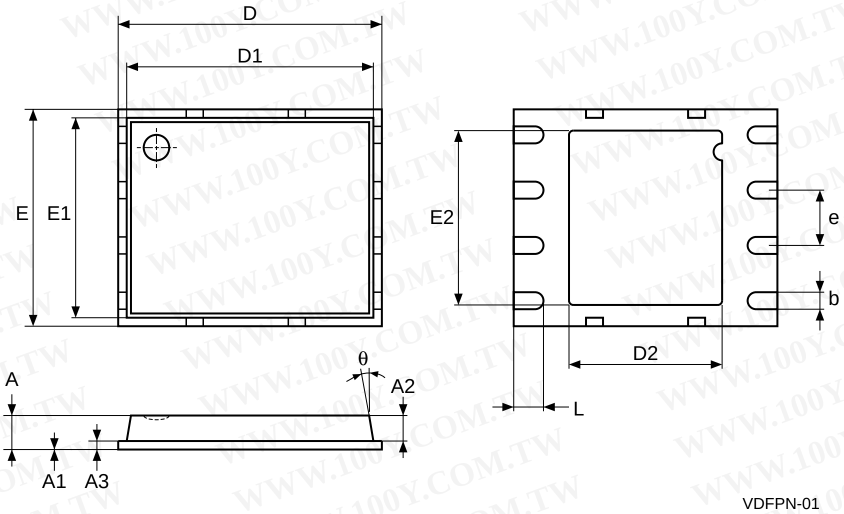


Note: Drawing is not to scale.

Table 19. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

Figure 27. MLP8, 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Outline



Note: Drawing is not to scale.

Table 20. MLP8, 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.85		1.00	0.0335		0.0394
A1		0.00	0.05		0.0000	0.0020
A2	0.65			0.0256		
A3	0.20			0.0079		
b	0.40	0.35	0.48	0.0157	0.0138	0.0189
D	6.00			0.2362		
D1	5.75			0.2264		
D2	3.40	3.20	3.60	0.1339	0.1260	0.1417
E	5.00			0.1969		
E1	4.75			0.1870		
E2	4.00	3.80	4.20	0.1575	0.1496	0.1654
e	1.27			0.0500		
L	0.60	0.50	0.75	0.0236	0.0197	0.0295
θ			12°			12°

PART NUMBERING

Table 21. Ordering Information Scheme

Example: M25P40 – V MN 6 T P

Device Type
M25P = Serial Flash Memory for Code Storage

Device Function
40 = 4 Mbit (512K x 8)

Operating Voltage
V = V_{CC} = 2.7 to 3.6V

Package
MN = SO8 (150 mil width)
MP = VDFPN8 6x5mm (MLP8)

Device Grade
6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow
3 [4] = Device tested with High Reliability Certified Flow[1].
Automotive temperature range (–40 to 125 °C)

Option
blank = Standard Packing
T = Tape and Reel Packing

Plating Technology
blank = Standard SnPb plating
P[2] = Lead-Free and RoHS compliant
G[3] = Lead-Free, RoHS compliant, Sb_2O_3-free and TBBA-free

Note: 1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Available for SO8 package only
3. Available for MLP package only
4. Device grade 3 available in SO8 Lead-free and RoHS compliant package

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

REVISION HISTORY

Table 22. Document Revision History

Date	Rev.	Description of Revision
12-Apr-2001	1.0	Document written
25-May-2001	1.1	Serial Paged Flash Memory renamed as Serial Flash Memory
11-Sep-2001	1.2	Changes to text: Signal Description/Chip Select; Hold Condition/1st para; Protection modes; Release from Power-down and Read Electronic Signature (RES); Power-up Repositioning of several tables and illustrations without changing their contents Power-up timing illustration; SO8W package removed Changes to tables: Abs Max Ratings/V_{IO}; DC Characteristics/V_{IL}
16-Jan-2002	1.3	FAST_READ instruction added. Document revised with new timings, V_{WI}, I_{CC3} and clock slew rate. Descriptions of Polling, Hold Condition, Page Programming, Release for Deep Power-down made more precise. Value of t_W(max) modified.
12-Sep-2002	1.4	Clarification of descriptions of entering Stand-by Power mode from Deep Power-down mode, and of terminating an instruction sequence or data-out sequence. VFQFPN8 package (MLP8) added. Document promoted to Preliminary Data.
13-Dec-2002	1.5	Typical Page Program time improved. Deep Power-down current changed. Write Protect setup and hold times specified, for applications that switch Write Protect to exit the Hardware Protection mode immediately before a WRSR, and to enter the Hardware Protection mode again immediately after.
12-Jun-2003	1.6	Document promoted from Preliminary Data to full Datasheet
24-Nov-2003	2.0	Table of contents, warning about exposed paddle on MLP8, and Pb-free options added. 40MHz AC Characteristics table included as well as 25MHz. I_{CC3}(max), t_{SE}(typ) and t_{BE}(typ) values improved. Change of naming for VDFPN8 package
12-Mar-2004	3.0	Automotive range added. Soldering temperature information clarified for RoHS compliant devices
05-Aug-2004	4.0	Device Grade information clarified. Data-retention measurement temperature corrected. Details of how to find the date of marking added.