M25P40

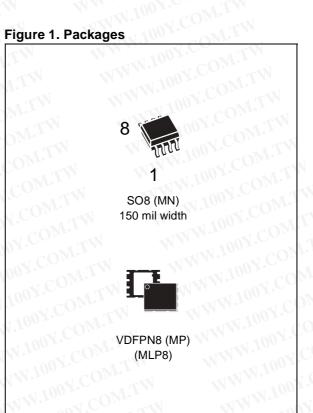
4 Mbit, Low Voltage, Serial Flash Memory With 40MHz SPI Bus Interface

WWW.100Y.COM

WWW.101

FEATURES SUMMARY

- 4 Mbit of Flash Memory
- Page Program (up to 256 Bytes) in 1.5ms É (typical)
- Sector Erase (512 Kbit) in 1s (typical)
- Bulk Erase (4 Mbit) in 4.5s (typical)
- 2.7 to 3.6V Single Supply Voltage
- SPI Bus Compatible Serial Interface
- 40MHz Clock Rate (maximum)
- Deep Power-down Mode 1µA (typical) 1
- Electronic Signature (12h)



WWW.100Y.COM

WWW.

V.100Y.COM.TW M25P40

NW.100Y.CON TABLE OF CONTENTS

WWW.100Y.COM.TW

DY.COM.TW

TABLE OF CONTENTS
FEATURES SUMMARY1
Figure 1. Packages1
SUMMARY DESCRIPTION
Figure 2. Logic Diagram
Figure 3. SO and VDFPN Connections 5 Table 1. Signal Names 5
SIGNAL DESCRIPTION
Serial Data Output (Q)
Serial Data Input (D) 6 Serial Clock (C) 6
Chip Select (S)
Hold (HOLD)
Write Protect (W)
SPI MODES
Figure 4. Bus Master and Memory Devices on the SPI Bus. 7 Figure 5. SPI Modes Supported 7
OPERATING FEATURES
Page Programming
Sector Erase and Bulk Erase
Active Power, Stand-by Power and Deep Power-Down Modes.
Status Register
WIP bit
WEL bit
SRWD bit
Protection Modes9
Table 2. Protected Area Sizes. 9 Use Id Condition 10
Hold Condition 10 Figure 6. Hold Condition Activation 10
MEMORY ORGANIZATION
Table 3. Memory Organization 11
Figure 7. Block Diagram
INSTRUCTIONS
Table 4. Instruction Set
Write Enable (WREN)

57

WWW.100Y.COM.T

M25P40

CONTRA WWW.100Y.COM	胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw	M25P40
Figure 8 Write Enable (WREN) Ins	struction Sequence	11
	truction Sequence	
	······	
	ومعادية والمعالية والمعالية والمعالمة والمعالية والمعالية والمعالية والمعالية والمعالية والمعالية والمعالية وا	
	0.0000000000000000000000000000000000000	
Figure 10.Read Status Register (RD	OSR) Instruction Sequence and Data-Out Sequ	uence 15
Write Status Register (WRSR)		
Figure 11.Write Status Register (WF	RSR) Instruction Sequence	16
Table 6. Protection Modes		
Read Data Bytes (READ)	N 100	
	Instruction Sequence and Data-Out Sequence	
	I (FAST_READ)	
	er Speed (FAST_READ) Instruction Sequence	
guonoo 10		
Bago Brogram (BB)	WWW. TUDE CONTENN WWW	1001. 20
	uction Sequence	
	ction Sequence	
-	on Sequence	
	nstruction Sequence	
	and Read Electronic Signature (RES)	
	er-down and Read Electronic Signature (RES)	Instruction Se-
quence and Data-Out Sequence24		
Figure 19.Release from Deep Powe	er-down (RES) Instruction Sequence	
POWER-UP AND POWER-DOWN	er-down (RES) Instruction Sequence	
Figure 20.Power-up Timing	WILLING MARKEN WILLING	
Table 7. Power-Up Timing and VM	/I Threshold	
INITIAL DELIVERY STATE		
INITIAL DELIVERY STATE	ON THE WWW. 1002.CO.	
	gs	
DC AND AC PARAMETERS	X.COM. T.W. WWW.ING COM	
Table 9. Operating Conditions	N.COMPTIN. NYNN.	
	rance	
-	ce Grade 6)	
	ce Grade 3)	

N.100Y.COM.TW

V.100Y.COM.TW M25P40

WWW.100Y.COM.TV

	14. Instruction Times (Device Grade 6)	
Table	15. Instruction Times (Device Grade 3)	31
Table	16. AC Measurement Conditions	31
Figure	e 21.AC Measurement I/O Waveform	31
Table	17. AC Characteristics (25MHz Operation, Device Grade 6 or 3)	32
Table	18. AC Characteristics (40MHz Operation, Device Grade 6)	33
Figure	e 22.Serial Input Timing	34
Figure	e 23.Write Protect Setup and Hold Timing during WRSR when SRWD=1	34
	e 24.Hold Timing	
Figure	e 25.Output Timing	
PACKAG	E MECHANICAL	3e
Figure	e 26.SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Outline	36
Table	19. SO8 narrow - 8 lead Plastic Small Outline, 150 mils body width, Package Mechan	ical Dat
36		
Figure	e 27.MLP8, 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Outline	37
Table	20. MLP8, 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Mechanical	Data37
	MBERING	
	21. Ordering Information Scheme	
REVISION	N HISTORY	39
Table	22. Document Revision History	39

SUMMARY DESCRIPTION

The M25P40 is a 4 Mbit (512K x 8) Serial Flash Memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The memory is organized as 8 sectors, each containing 256 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 2048 pages, or 524,288 bytes.

The whole memory can be erased using the Bulk Erase instruction, or a sector at a time, using the Sector Erase instruction.

Figure 2. Logic Diagram

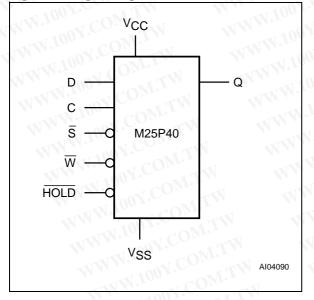
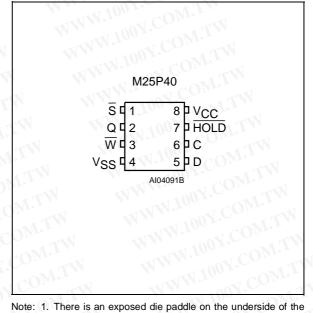


Table 1. Signal Names

С	Serial Clock	
D	Serial Data Input	
Q	Serial Data Output	
S	Chip Select	
W	Write Protect	
HOLD	Hold	
V _{CC}	Supply Voltage	
V _{SS}	Ground	
	WWW.1003.COM.1	





must not be allowed to be connected to any other voltage or signal line on the PCB.2. See PACKAGE MECHANICAL section for package di-

MLP8 package. This is pulled, internally, to V_{SS}, and

mensions, and how to identify pin-1.

M25P40

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

SIGNAL DESCRIPTION

Serial Data Output (Q). This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

Serial Data Input (D). This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

Serial Clock (C). This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

Chip Select (S). When this input signal is High, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in the Standby mode

(this is not the Deep Power-down mode). Driving Chip Select (\overline{S}) Low enables the device, placing it in the active power mode.

After Power-up, a falling edge on Chip Select (\overline{S}) is required prior to the start of any instruction.

Hold (HOLD). The Hold (HOLD) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select (\overline{S}) driven Low.

Write Protect (\overline{W}). The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP2, BP1 and BP0 bits of the Status Register).

Á7/

SPI MODES

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

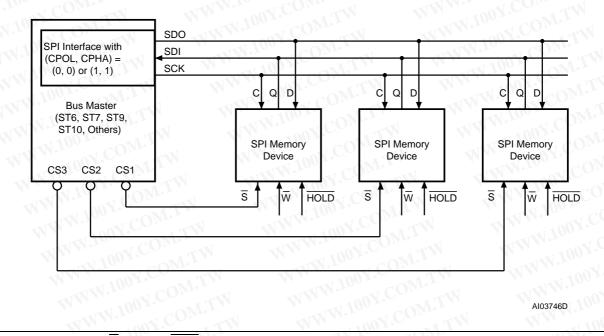
For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data

is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in Figure 5., is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. Bus Master and Memory Devices on the SPI Bus



Note: The Write Protect (\overline{W}) and Hold (\overline{HOLD}) signals should be driven, High or Low as appropriate.

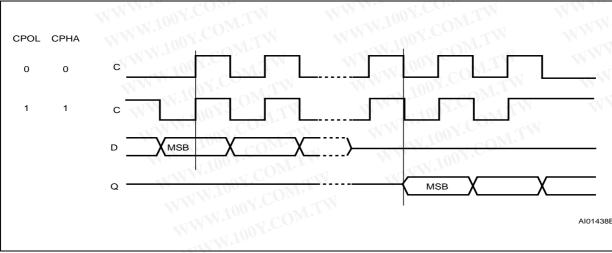


Figure 5. SPI Modes Supported

M25P40

M25P40

OPERATING FEATURES

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Sector Erase and Bulk Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a sector at a time, using the Sector Erase (SE) instruction, or throughout the entire memory, using the Bulk Erase (BE) instruction. This starts an internal Erase cycle (of duration t_{SE} or t_{BE}).

The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE or BE) can be achieved by not waiting for the worst case delay (t_W , t_{PP} , t_{SE} , or t_{BE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (\overline{S}) is Low, the device is enabled, and in the Active Power mode.

When Chip Select (\overline{S}) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program,

Erase, Write Status Register). The device then goes in to the Stand-by Power mode. The device consumption drops to I_{CC1} .

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2} . The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Electronic Signature (RES) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions.

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

SRWD bit. The Status Register Write Disable (SRWD) bit is <u>op</u>erated in conjunction with the Write Protect (\overline{W}) signal. The Status Register Write Disable (SRWD) bit and Write Protect (\overline{W}) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits.

47/

M25P40

W.100X.COM.T **Protection Modes**

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M25P40 boasts the following data protection mechanisms:

- Power-On Reset and an internal timer (tPUW) can provide protection against inadvertant changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit . This bit is returned to its reset state by the following events:
 - Power-up

Write Disable (WRDI) instruction completion

- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Bulk Erase (BE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as readonly. This is the Software Protected Mode (SPM).
- The Write Protect (\overline{W}) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Write Disable (SRWD) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertant Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Powerdown instruction).

Sta	tus Regi Content		Memo	ry Content
BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	0	none	All sectors ¹ (eight sectors: 0 to 7)
0	0	110	Upper eighth (Sector 7)	Lower seven-eighths (seven sectors: 0 to 6)
0	1	0	Upper quarter (two sectors: 6 and 7)	Lower three-quarters (six sectors: 0 to 5)
0	1	1	Upper half (four sectors: 4 to 7)	Lower half (four sectors: 0 to 3)
1	0 🔨	0	All sectors (eight sectors: 0 to 7)	none
1	0	1	All sectors (eight sectors: 0 to 7)	none
1	1	0	All sectors (eight sectors: 0 to 7)	none
1	1	1	All sectors (eight sectors: 0 to 7)	none

Note: 1. The device is ready to accept a Bulk Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) are 0. WWW.100Y.CO

M25P40

Hold Condition

The Hold (HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select (\overline{S}) Low.

The H<u>old con</u>dition starts on the falling edge of the Hold (HOLD) signal, provided that this coincides with Serial Clock (C) being Low (as shown in Figure 6.).

The H<u>old condition</u> ends on the rising edge of the Hold (HOLD) signal, provided that this coincides with Serial Clock (C) being Low.

If the falling edge does not coincide with Serial Clock (C) being Low, the Hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the Hold condition ends after Serial Clock (C) next goes Low. (This is shown in Figure 6.).

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

Normally, the device is kept selected, with Chip Select (\overline{S}) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (\overline{S}) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD) High, and then to drive Chip Select (\overline{S}) Low. This prevents the device from going back to the Hold condition.

47/

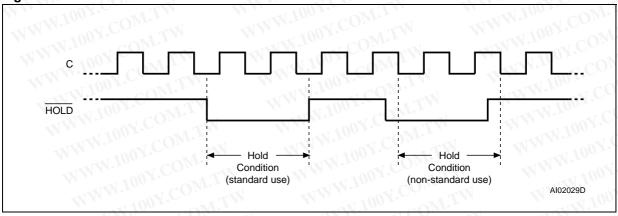


Figure 6. Hold Condition Activation

M25P40

W.100Y.COM.TW **MEMORY ORGANIZATION**

The memory is organized as:

V.100Y.COM.TW

- 524,288 bytes (8 bits each)
- 8 sectors (512 Kbits, 65536 bytes each)
- 2048 pages (256 bytes each).

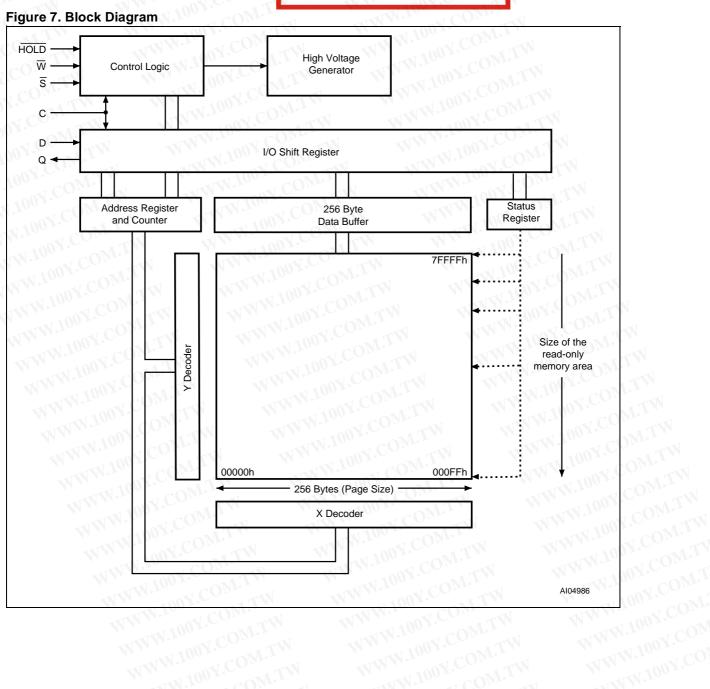
Table 3 Memory Organization

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector or Bulk Erasable (bits are erased from 0 to 1) but not Page Erasable. WWW.100Y.C

Sector	Add	Iress Range
7	70000h	7FFFh
6	60000h	6FFFFh
05	50000h	5FFFFh
C4	40000h	4FFFFh
3	30000h	3FFFFh C
2	20000h	2FFFh CO
1 coM.1	10000h	1FFFFh
000 0 0M.	00000h	0FFFh







INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select (\overline{S}) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in Table 4..

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (\overline{S}) must be driven High after the last bit of the instruction sequence has been shifted in.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Read Status Register (RDSR) or Release from Deep Power-down, and Read Electronic Signature (RES) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (\overline{S}) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select (\overline{S}) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (\overline{S}) must driven High when the number of clock pulses after Chip Select (\overline{S}) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Instruction	Description	One-byte Instructi	on Code	Address Bytes	Dummy Bytes	Data Bytes
WREN	Write Enable	0000 0110	06h	0	0	0
WRDI	Write Disable	0000 0100	04h	0	0	0
RDSR	Read Status Register	0000 0101	05h	0	0	1 to ∞
WRSR	Write Status Register	0000 0001	01h	0	0	1.101
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0Bh	3	1	1 to ∞
PP 🚿	Page Program	0000 0010	02h	3	0	1 to 256
SE	Sector Erase	1101 1000	D8h	3	0	0
BE	Bulk Erase	1100 0111	C7h	0	0	0
DP	Deep Power-down	1011 1001	B9h	0	0	0
RES	Release from Deep Power-down, and Read Electronic Signature	1010 1011	ABh	.001.1	3	1 to ∞
	Release from Deep Power-down		VN.100	0	0	0

Table 4. Instruction Set

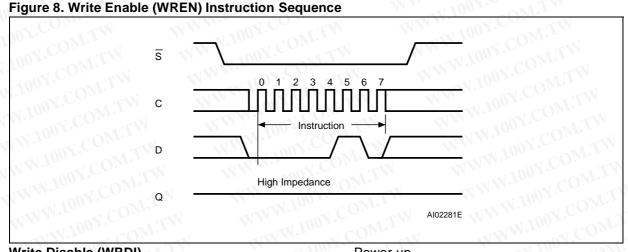
M25P40

Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 8.) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select (\overline{S}) Low, sending the instruction code, and then driving Chip Select (\overline{S}) High.



Write Disable (WRDI)

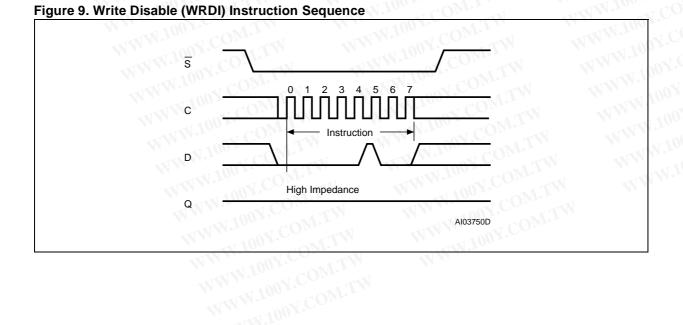
The Write Disable (WRDI) instruction (Figure 9.) resets the Write Enable Latch (WEL) bit. The Write Disable (WRDI) instruction is entered by driving Chip Select (\overline{S}) Low, sending the instruction code, and then driving Chip Select (\overline{S}) High. The Write Enable Latch (WEL) bit is reset under the following conditions: Power-up

- Write Disable (WRDI) instruction completion

 Write Status Register (WRSR) instruction completion

Page Program (PP) instruction completion

- Sector Erase (SE) instruction completion
- Bulk Erase (BE) instruction completion

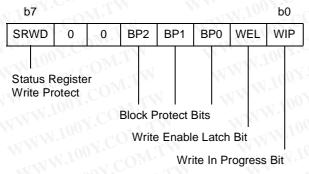


M25P40

Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 10..

Table 5. Status Register Format



The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

A7/

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 2.) becomes protected against Page Program (PP) and Sector Erase (SE) instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Bulk Erase (BE) instruction is executed if, and only if, both Block Protect (BP2, BP1, BP0) bits are 0.

SRWD bit. The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (\overline{W}) signal. The Status Register Write Disable (SRWD) bit and Write Protect (\overline{W}) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect (\overline{W}) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

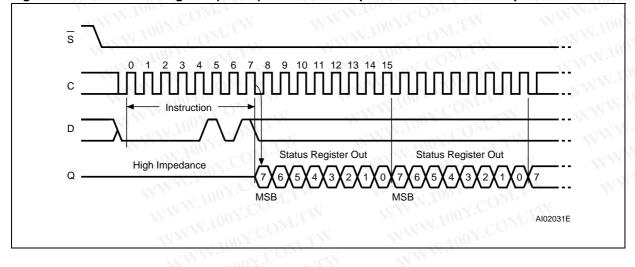


Figure 10. Read Status Register (RDSR) Instruction Sequence and Data-Out Sequence

15/40

M25P40

Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (\overline{S}) Low, followed by the instruction code and the data byte on Serial Data Input (D).

The instruction sequence is shown in Figure 11..

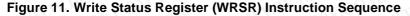
The Write Status Register (WRSR) instruction has no effect on b6, b5, b1 and b0 of the Status Register. b6 and b5 are always read as 0.

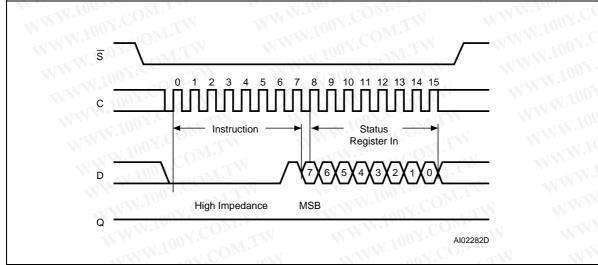
Chip Select (\overline{S}) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (\overline{S}) is driven High, the self-timed Write Status Register cycle

(whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 2.. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable_(SRWD) bit in accordance with the Write Protect (W) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

47/





M25P40

W	SRWD		Write Protection of the	Memor	emory Content	
Signal	Bit	Mode	Status Register	Protected Area ¹	Unprotected Area ¹	
1	0	Software Protected	Status Register is Writable	WW.1003	CONT	
0	0		(if the WREN instruction has set the WEL bit)	Protected against Page Program, Sector Erase	Ready to accept Page Program and Sector Erase	
ov ¹ .CC	M.TW 1	(SPM)	The values in the SRWD, BP2, BP1 and BP0 bits can be changed	and Bulk Erase	instructions	
00Y.C	com.T	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the SRWD, BP2, BP1 and BP0 bits cannot be changed	Protected against Page Program, Sector Erase and Bulk Erase	Ready to accept Page Program and Sector Erase instructions	

Table 6. Protection Modes

Note: 1. As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in Table 2..

The protection features of the device are summarized in Table 6..

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect (W) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect (W):

- If Write Protect (W) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect (W) is driven Low, it is not possible to write to the Status Register even if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the

Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP2, BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect (W) Low
- or by driving Write Protect (W) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect (\overline{W}) High.

If Write Protect (\overline{W}) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP2, BP1, BP0) bits of the Status Register, can be used.

لركم

M25P40

Read Data Bytes (READ)

The device is first selected by driving Chip Select (\overline{S}) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency f_R , during the falling edge of Serial Clock (C).

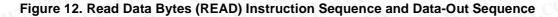
The instruction sequence is shown in Figure 12..

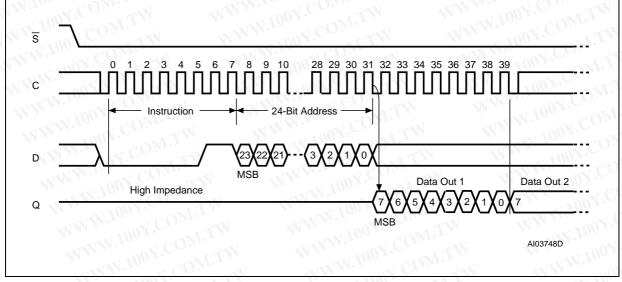
The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

> The Read Data Bytes (READ) instruction is terminated by driving Chip Select (\overline{S}) High. Chip Select (\overline{S}) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

> > **47/**





Note: 1. Address bits A23 to A19 are Don't Care.



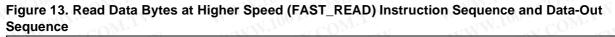
Read Data Bytes at Higher Speed (FAST_READ)

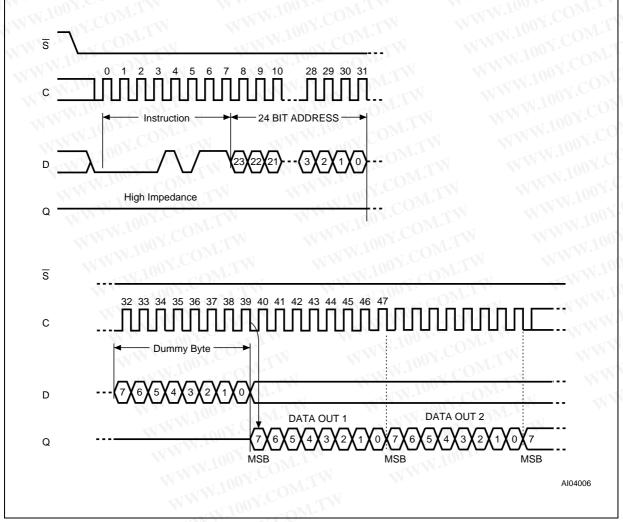
The device is first selected by driving Chip Select (\overline{S}) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency f_C , during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 13..

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (\overline{S}) High. Chip Select (\overline{S}) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.





Note: 1. Address bits A23 to A19 are Don't Care.

M25P40

Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (\overline{S}) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (D). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (\overline{S}) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 14..

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed cor-

Figure 14. Page Program (PP) Instruction Sequence

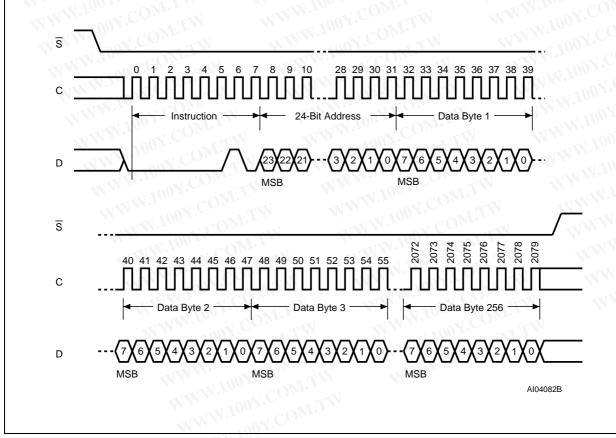
rectly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (\overline{S}) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (\overline{S}) is driven High, the selftimed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the selftimed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3. and Table 2.) is not executed.

47/



Note: 1. Address bits A23 to A19 are Don't Care.



Sector Erase (SE)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL). The Sector Erase (SE) instruction is entered by driving Chip Select (S) Low, followed by the instruction code, and three address bytes on Serial Data Input (D). Any address inside the Sector Erase (SE) instruction. Chip Select (S) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 15...

Chip Select (\overline{S}) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (\overline{S}) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

M25P40

A Sector Erase (SE) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3. and Table 2.) is not executed.

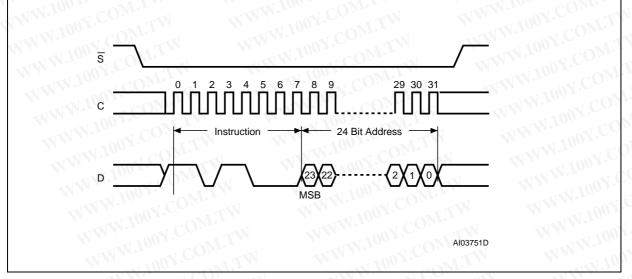
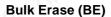


Figure 15. Sector Erase (SE) Instruction Sequence

Note: 1. Address bits A23 to A19 are Don't Care.

A7/

M25P40



The Bulk Erase (BE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Bulk Erase (BE) instruction is entered by driving Chip Select (\overline{S}) Low, followed by the instruction code on Serial Data Input (D). Chip Select (\overline{S}) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 16..

Chip Select (\overline{S}) must be driven High after the eighth bit of the instruction code has been latched

in, otherwise the Bulk Erase instruction is not executed. As soon as Chip Select (\overline{S}) is driven High, the self-timed Bulk Erase cycle (whose duration is t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the selftimed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

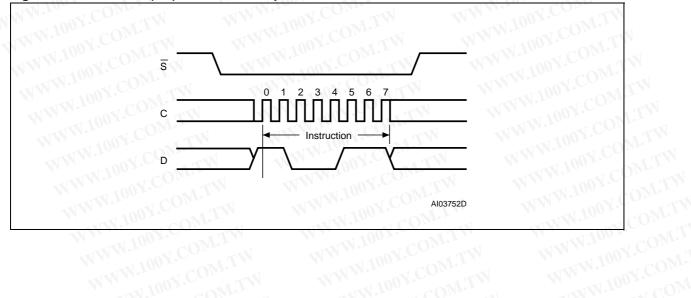
勝特力材料 886-3-5753170

胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

> The Bulk Erase (BE) instruction is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Bulk Erase (BE) instruction is ignored if one, or more, sectors are protected.

> > **47/**





M25P40

Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select (\overline{S}) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in Table 12.).

Once the device has entered the Deep Powerdown mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Electronic Signature (RES) instruction also allows the Electronic Signature of the device to be output on Serial Data Output (Q).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode.

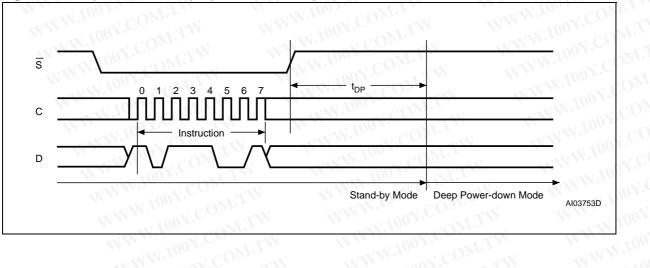
The Deep Power-down (DP) instruction is entered by driving Chip Select (\overline{S}) Low, followed by the instruction code on Serial Data Input (D). Chip Select (\overline{S}) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 17..

Chip Select (\overline{S}) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (\overline{S}) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 17. Deep Power-down (DP) Instruction Sequence



A7/

M25P40

Release from Deep Power-down and Read Electronic Signature (RES)

Once the device has entered the Deep Powerdown mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

The instruction can also be used to read, on Serial Data Output (Q), the 8-bit Electronic Signature, whose value for the M25P40 is 12h.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Electronic Signature (RES) instruction always provides access to the 8bit Electronic Signature of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Electronic Signature (RES) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select (\overline{S}) Low. The instruction code is followed by 3 dummy bytes, each bit being latched-in on Serial

Data Input (D) during the rising edge of Serial Clock (C). Then, the 8-bit Electronic Signature, stored in the memory, is shifted out on Serial Data Output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 18..

The Release from Deep Power-down and Read Electronic Signature (RES) instruction is terminated by driving Chip Select (S) High after the Electronic Signature has been read at least once. Sending additional clock cycles on Serial Clock (C), while Chip Select (\overline{S}) is driven Low, cause the Electronic Signature to be output repeatedly.

When Chip Select (\overline{S}) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by tRES2, and Chip Select (\overline{S}) must remain High for at least t_{RES2}(max), as specified in Table 17.. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

47/

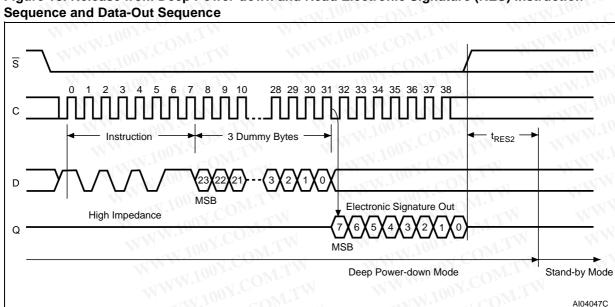
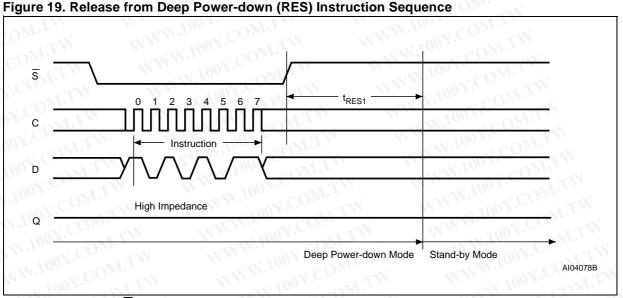


Figure 18. Release from Deep Power-down and Read Electronic Signature (RES) Instruction

Note: The value of the 8-bit Electronic Signature, for the M25P40, is 12h.



M25P40



Driving Chip Select (\overline{S}) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit Electronic Signature has been transmitted for the first time (as shown in Figure 19.), still insures that the device is put into Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If

the device was previously in the Deep Powerdown mode, though, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (\overline{S}) must remain High for at least t_{RES1}(max), as specified in Table 17.. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

V.100Y.COM.TW

W.100Y.COM.

M25P40

POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must not be selected (that is Chip Select (\overline{S}) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC}(min) at Power-up, and then for a further delay of t_{VSL}
- V_{SS} at Power-down

Usually a simple pull-up resistor on Chip Select (\overline{S}) can be used to insure safe and proper Power-up and Power-down.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the POR threshold value, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC} (min). No Write Status Register,

Program or Erase instructions should be sent until the later of:

t_{PUW} after V_{CC} passed the V_{WI} threshold

- t_{VSL} afterV_{CC} passed the V_{CC}(min) level These values are specified in Table 7..

If the delay, t_{VSL} , has elapsed, after V_{CC} has risen above V_{CC} (min), the device can be selected for READ instructions even if the t_{PUW} delay is not yet fully elapsed.

At Power-up, the device is in the following state:

- The device is in the Standby mode (not the Deep Power-down mode).
- The Write Enable Latch (WEL) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} feed. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 0.1μ F).

At Power-down, when V_{CC} drops from the operating voltage, to below the POR threshold value, V_{WI} , all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

M25P40

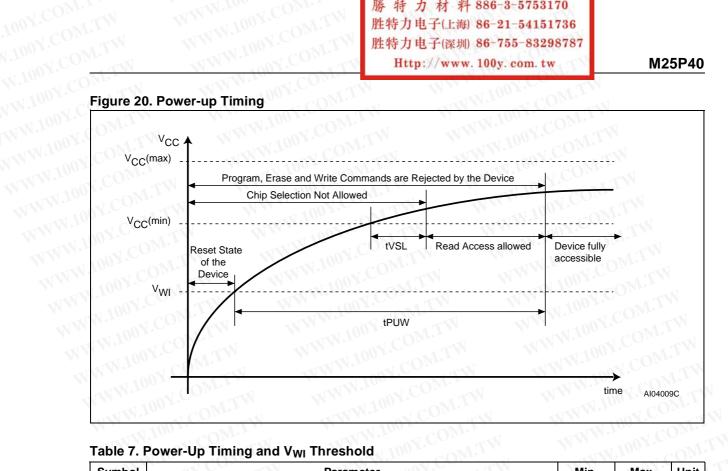


Table 7. Power-Up Timing and V_{WI} Threshold

Symbol	Parameter	Min.	Max.	Uni
t _{VSL} 1	$V_{CC}(min)$ to \overline{S} low	10	W.1007	μs
t _{PUW} 1	Time delay to Write instruction	1	10	ms
V _{WI} ¹ 🔨	Write Inhibit Voltage	1	2	V

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains

WWW.100Y.COM.TW ...uspy.COMT FFh). The Status Register contains 00h (all Status WWW.100Y.COM.T Register bits are 0). WWW.100Y.COM.TW WWW.100Y

A7/

<u>M2</u>5P40

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T _{STG}	Storage Temperature	-65	150	°C
T _{LEAD}	Lead Temperature during Soldering	See I	note ¹	°C
Vio	Input and Output Voltage (with respect to Ground)	-0.6	4.0	V
Vcc	Supply Voltage	-0.6	4.0	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model) ²	-2000	2000	V

Note: 1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK[®] 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU

2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)



M25P40

W.100Y.COM.TW DC AND AC PARAMETERS

V.100Y.COM.TW

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters. W 100Y.COM.

Symbol	Parameter	Min.	Max.	Un
Vcc	Supply Voltage	2.7	3.6	V
00¥.CO	Ambient Operating Temperature (Device Grade 6)	-40	85	
TA	Ambient Operating Temperature (Device Grade 3)	-40	125	- °C

Table 10. Data Retention and Endurance

Parameter	Condition	Min.	Max.	Unit
Erase/Program Cycles	Device Grade 6	M.	100 000	cycles per
	Device Grade 3 ¹	DW.	10 000	sector
Data Retention	Device Grade 6	WT. NO.	20	NY.COM
	Device Grade 3 ¹ (at 85°C)	COMPT	20	years

Table 11. Capacitance

nbol	Parameter	Test Condition	Min.	Max.	Unit
OUT	Output Capacitance (Q)	V _{OUT} = 0V	WTI	8	pF
CIN	Input Capacitance (other pins)	$V_{IN} = 0V$	COM	6	pF

A7/

N.100Y.COM.TW M25P40

Symbol	Parameter	Test Condition (in addition to those in Table 9.)	Min.	Max.	Uni
CQù	Input Leakage Current	TW WW 100Y.	TIM	N ± 2	μA
ILO	Output Leakage Current	COULAN WWW MOD	COM	± 2	μA
I _{CC1}	Standby Current	$\overline{S} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$	A.COm	50	μA
I _{CC2}	Deep Power-down Current	$\overline{S} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$	N.COM	10	μA
00Y.C	Operating Current (READ)	$C = 0.1V_{CC} / 0.9.V_{CC} \text{ at } 40MHz, \\ Q = open$	DOX.CO	8	mA
I _{CC3}	Operating Current (READ)	$C = 0.1V_{CC} / 0.9.V_{CC} \text{ at } 20MHz, \\ Q = open$	100 1.C	4	mA
I _{CC4}	Operating Current (PP)	$\overline{S} = V_{CC}$	Yont	15	mA
I _{CC5}	Operating Current (WRSR)	$\overline{S} = V_{CC}$	1005	15	mA
I _{CC6}	Operating Current (SE)	$\overline{S} = V_{CC}$	WW.200	15	mA
I _{CC7}	Operating Current (BE)	$\overline{S} = V_{CC}$	WW.ro	15	mA
VIL	Input Low Voltage	WW.100 COM. TW	-0.5	0.3V _{CC}	V
V _{IH}	Input High Voltage	NW.100 COM. TW	0.7V _{CC}	V _{CC} +0.4	v
V _{OL}	Output Low Voltage	I _{OL} = 1.6mA	WWW	0.4	V
V _{OH}	Output High Voltage	I _{OH} = −100μA	V _{CC} -0.2	1.100	CV

Table 12. DC Characteristics (Device Grade 6)

Table 13. DC Characteristics (Device Grade 3)

Symbol	Parameter	Test Condition (in addition to those in Table 9.)	Min. ¹	Max. ¹	Unit
ILI	Input Leakage Current	WWW.LOOV.COM. TW	WWW.IU" OX.COM. TW		μA
I _{LO}	Output Leakage Current	MWW.100 COMP.	4	± 2	μA
I _{CC1}	Standby Current	$\overline{S} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$	N	100	μA
I _{CC2}	Deep Power-down Current	$\overline{S} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$		50	μA
	Operating Current (PEAD)	$C = 0.1V_{CC} / 0.9.V_{CC} \text{ at 40MHz},$ Q = open	WT.	8	mA
I _{CC3}	Operating Current (READ)	$C = 0.1V_{CC} / 0.9.V_{CC} \text{ at } 20MHz,$ Q = open	NT.N	4	mA
I _{CC4}	Operating Current (PP)	$\overline{S} = V_{CC}$	M. I	15	mA
I _{CC5}	Operating Current (WRSR)	$\overline{S} = V_{CC}$	OW.1	15	mA
I _{CC6}	Operating Current (SE)	$\overline{S} = V_{CC}$	CO _{M.1}	15	mA
I _{CC7}	Operating Current (BE)	$\overline{S} = V_{CC}$	CON.	15	mA
VIL	Input Low Voltage	OM.TW	- 0.5	0.3V _{CC}	V
VIH	Input High Voltage	CONTINUE	0.7V _{CC}	V _{CC} +0.4	V
V _{OL}	Output Low Voltage	I _{OL} = 1.6mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = −100μA	V _{CC} -0.2		V

Note: 1. This is preliminary data

M25P40

		Test conditions specified in Table 9	and Table 16.			
Symbol	Alt.	Parameter	Min.	Тур.	Max.	Uni
t _W	N	Write Status Register Cycle Time	W.100	5	15	ms
tpp	N	Page Program Cycle Time	W 100	1.4	5	ms
t _{SE}	LW	Sector Erase Cycle Time	W.W.I	1	3	s
t _{BE}	NT.	Bulk Erase Cycle Time	N. C. S.	4.5	10	s

W.100Y.COM.TW Table 14. Instruction Times (Device Grade 6)

TAM TOOX CONTA

Table 15. Instruction Times (Device Grade 3)

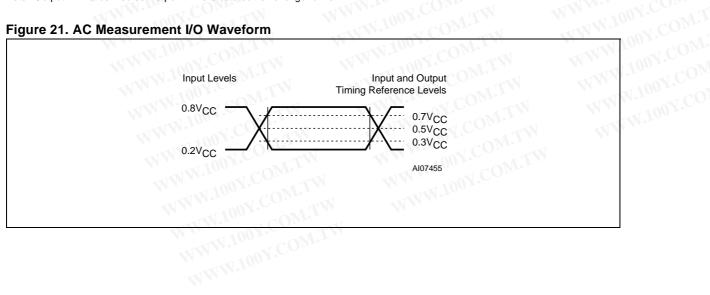
		Test conditions specified in Table 9. ar	d Table 16.			
Symbol	Alt.	Parameter	Min.	Typ. ^{1,2}	Max. ²	Uni
tw	COM.	Write Status Register Cycle Time	V	8	15	ms
tpp	COM.,	Page Program Cycle Time		1.5	5	ms
t _{SE}	V COM	Sector Erase Cycle Time	N	11.3	3	s
t _{BE}	T CON	Bulk Erase Cycle Time	177	4.5	10	s

V.100Y.COM.TW

Table 16. AC Measurement Conditions

ymbol	Parameter	Min.	Max.	Unit
CL	Load Capacitance	001. 01. 3	80	pF
4M	Input Rise and Fall Times	1002. COM.T.W.	5	ns
W	Input Pulse Voltages	0.2V _{CC} t	o 0.8V _{CC}	V
1	Input Timing Reference Voltages	0.3V _{CC} t	o 0.7V _{CC}	V
1	Output Timing Reference Voltages	Vc	c/2	V.100

Figure 21. AC Measurement I/O Waveform



M25P40

SymbolAlt.ParameterMin.*Typ.Max.*UnitfcfcClock Frequency for the following instructions: WREN, WRDI, RDSR, WRSRD.C.2.0MHzfRClock Frequency for READ instructionsD.C.2.0MHzfgR1cLHClock High Time182.0MHztcL1tLLClock Krequency for READ instructionsD.C.2.0MHztcL041cLLClock Name182.0MstcL041cLLClock Aligh Time182.0MstcL042Clock Rise Time* (peak to peak)0.12.0MstcL041csS Active Setup Time (relative to C)101.01.01.0tbCHtbsuData In Setup Time (relative to C)101.01.01.01.0tbCHtbsuData In Hold Time (relative to C)101.01.01.01.01.0tbcHXtbyuData In Hold Time (relative to C)101.	M		Test conditions specified in Table 9. and	Table 16.	COMPL		
fcfcFAST_READ. PR SE, BE, DR RES. WREN, WRDI, RDSR, WRSRD.C.25MHzfRClock Frequency for READ instructionsD.C.20MHzt _{CH} 1t _{CLL} Clock High Time18t _{CL} 1t _{CLL} Clock Low Time18t _{CLC} 2Clock Rise Time3 (peak to peak)0.1t _{CLCL} 2Clock Rait Time3 (peak to peak)0.1t _{CLCL} 2Clock Fail Time3 (peak to peak)0.1t _{CLCL} 2Clock Fail Time3 (peak to peak)0.1t _{CHCL} 2Clock Fail Time3 (peak to peak)0.1t _{CHSL} S Active Setup Time (relative to C)10t _{CHSL} TosuData In Hold Time (relative to C)10t _{CHSH} S Active Hold Time (relative to C)10t _{CHSH} S Not Active Betup Time (relative to C)10t _{CHSH} S So to Active Setup Time (relative to C)10t _{SHSL} t _{CSH} S Deselect Time100t _{SHSL} t _{CSH} S Deselect Time100	Symbol	Alt.	Parameter	Min. ⁵	Тур.	Max. ⁵	Unit
t_{CH}^1 t_{CLH} Clock High Time181818 t_{CL}^1 t_{CLL} Clock Low Time18 t_{CLC}^2 Clock Rise Time³ (peak to peak)0.1V/ns t_{CLCL}^2 Clock Fall Time³ (peak to peak)0.1V/ns t_{CLCL}^2 Clock Fall Time³ (peak to peak)0.1V/ns t_{CLCL}^2 Clock Fall Time³ (peak to peak)0.1V/ns t_{CLL} t_{CSS} S Active Setup Time (relative to C)10 t_{CHSL} t_{CSS} S Active Hold Time (relative to C)10 t_{CHSH} t_{DH} Data In Setup Time t_{CHSH} t_{DH} Data In Hold Time t_{CHSH} t_{DH} Data In Hold Time (relative to C)10 t_{CLQ} t_{DH} Data In Hold Time (relative to C)10 t_{SHCH} S Active Hold Time (relative to C)10 t_{SHCH} t_{CSH} S Deselect Time100 <t< td=""><td>fc</td><td>fc</td><td>FAST_READ, PP, SE, BE, DP, RES,</td><td>D.C.</td><td>Y.CON</td><td>25</td><td>MHz</td></t<>	fc	fc	FAST_READ, PP, SE, BE, DP, RES,	D.C.	Y.CON	25	MHz
t_{CL} t_{CLL} Clock Low Time181818 t_{CLCH}^2 Clock Rise Time ³ (peak to peak)0.1V/ns t_{CHCL}^2 Clock Fall Time ³ (peak to peak)0.1V/ns t_{CHCL}^2 Clock Fall Time ³ (peak to peak)0.1V/ns t_{CHCL}^2 Clock Fall Time ³ (peak to peak)0.1V/ns t_{CHSL} t_{CSS} \overline{S} Active Setup Time (relative to C)10Ns t_{CHSL} \overline{S} Not Active Hold Time (relative to C)10Ns t_{CHDX} t_{DH} Data In Setup Time5Ns t_{CHSH} \overline{S} Active Hold Time (relative to C)10Ns t_{CHSH} \overline{S} Active Hold Time (relative to C)10Ns t_{SHCH} \overline{S} Not Active Setup Time (relative to C)10Ns t_{SHSL} t_{CSH} \overline{S} Deselect Time100Ns t_{SHSL} t_{CSH} \overline{S} Deselect Time100Ns t_{SHQZ}^2 t_{DIS} Output Disable Time100Ns t_{LCAV} t_V Clock Low to Output ValidNsNs t_{LCAV} t_V Clock Low to Output ValidNsNs t_{HCAH} HOLD Edup Time (relative to C)10NsNs t_{HCAV} HOLD Edup Time (relative to C)10NsNs t_{HCAV} HOLD Edup Time (relative to C)10NsNs t_{HCAH} HOLD Edup Time (relative to C)10NsNs t_{HCAV} HOLD Hold Time (rela	f _R	I.M.	Clock Frequency for READ instructions	D.C.	N C	20	MHz
t_{CLCH}^2 Clock Rise Time ³ (peak to peak)0.1V/ns t_{CHCL}^2 Clock Fall Time ³ (peak to peak)0.1V/ns t_{CHCL} t_{CSS} \bar{S} Active Setup Time (relative to C)10N t_{CHSL} \bar{S} Not Active Hold Time (relative to C)10N t_{CHSL} \bar{S} Not Active Hold Time (relative to C)10N t_{CHSL} \bar{S} Not Active Hold Time (relative to C)10N t_{CHDX} t_{DH} Data In Hold Time5N t_{CHSH} \bar{S} Active Hold Time (relative to C)10N t_{SHCH} \bar{S} Not Active Setup Time (relative to C)10N t_{SHCH} \bar{S} Not Active Setup Time (relative to C)10N t_{SHCH} \bar{S} Deselect Time100NNs t_{SHSL} t_{CSH} \bar{S} Deselect Time100N t_{CLOY} t_V Clock Low to Output Valid15ns t_{CLOY} t_V Clock Low to Output ValidNN t_{CLOY} t_V Clock Low to Clock Low CO10N t_{HHQ} HOLD Betup Time (relative to C)10NN t_{HHCH} HOLD Hold Time (relative to C)10NN t_{HHCH} HOLD Hold Time (relative to C)10 </td <td>t_{CH}¹</td> <td>tCLH</td> <td>Clock High Time</td> <td>18</td> <td>00 × .0</td> <td>DW</td> <td>ns</td>	t _{CH} ¹	tCLH	Clock High Time	18	00 × .0	DW	ns
t_{CHCL}^2 Clock Fall Time ³ (peak to peak)0.1V/ns t_{SLCH} t_{CSS} \overline{S} Active Setup Time (relative to C)10ns t_{CHSL} \overline{S} Not Active Hold Time (relative to C)1010ns t_{CHSL} t_{DSU} Data In Setup Time5ns t_{CHDX} t_{DH} Data In Hold Time5ns t_{CHSH} \overline{S} Active Hold Time (relative to C)10ns t_{CHSH} \overline{S} Active Hold Time (relative to C)10ns t_{SHCH} \overline{S} Active Hold Time (relative to C)10ns t_{SHCH} \overline{S} Active Hold Time (relative to C)10ns t_{SHCH} \overline{S} Not Active Setup Time (relative to C)10ns t_{SHSL} t_{CSH} \overline{S} Deselect Time100ns t_{LQZ}^2 t_{DIS} Output Disable Time10ns t_{LQA} t_{HO} Output Disable Time0ns t_{LCAV} t_{V} Clock Low to Output Validns t_{LCAV} t_{HO} Output Hold Time (relative to C)10ns t_{LCAV} $HOLD$ Setup Time (relative to C)10ns t_{HLCH} HOLD Hold Time (relative to C)10ns t_{HCAV}^2 t_{LZ} HOLD Hold Time (relative to C)10ns t_{HHAX}^2 HOLD Hold Time (relative to C) <td>tcL¹</td> <td>tCLL</td> <td>Clock Low Time</td> <td>18</td> <td>Toor</td> <td>CONT</td> <td>ns</td>	tcL ¹	tCLL	Clock Low Time	18	Toor	CONT	ns
tsLcHtcss \overline{S} Active Setup Time (relative to C)10nstcHsL \overline{S} Not Active Hold Time (relative to C)10nstbVcHtbsuData In Setup Time5nstcHDXtpHData In Hold Time (relative to C)10nstcHBH \overline{S} Active Hold Time (relative to C)10nstcHSH \overline{S} Active Hold Time (relative to C)10nstsHcH \overline{S} Not Active Setup Time (relative to C)10nstsHcH \overline{S} Not Active Setup Time (relative to C)10nstsHcLtcsH \overline{S} Deselect Time100nstsHsLtcsH \overline{S} Deselect Time100nstcLQVtvClock Low to Output Valid15nstcLQVtvClock Low to Output Valid15nstcLQVtvClock Low to Output Valid10nstHLCHHOLD Setup Time (relative to C)10nstHHCHHOLD Edup Time (relative to C)10nstHHCHHOLD Hold Time (relative to C)10nstHHQX ² tLzHOLD to Output High-Z20nstHHQx ² tLzHOLD to Output High-Z20nstsHqutWrite Protect Setup Time100nstsHqutWrite Protect Hold Time100nstginature Read3 μ stsginature Read3 μ stsginature Read3 μ stcH2S High to Standby Mode withet Electronic </td <td>tCLCH²</td> <td>M.I.W</td> <td>Clock Rise Time³ (peak to peak)</td> <td>0.1</td> <td>1.100</td> <td>COM.</td> <td>V/ns</td>	tCLCH ²	M.I.W	Clock Rise Time ³ (peak to peak)	0.1	1.100	COM.	V/ns
tCHSL \overline{S} Not Active Hold Time (relative to C)1010nstDVCHtDSUData In Setup Time5nstCHDXtDHData In Hold Time5nstCHBH \overline{S} Active Hold Time (relative to C)10nstSHOH \overline{S} Not Active Setup Time (relative to C)10nstSHOH \overline{S} Deselect Time100nstSHSLtCSH \overline{S} Deselect Time100nstGLQVtVClock Low to Output ValidnstLQVtVClock Low to Output ValidnstHLCHHOLD Setup Time (relative to C)10nstHLCHHOLD Setup Time (relative to C)10nstHLCHHOLD Setup Time (relative to C)10nstHHCHHOLD Nold Time (relative to C)10nstHHCHHOLD Setup Time (relative to C)10nstHHCHHOLD Nold Time (relative to C)10nstHHCHHOLD to Output Low-ZtHHCX ² tLzHOLD to Output High-ZtHHCX ⁴ Write Protect Setup Time20nstHLCA ⁴ Write Protect Hold Time100ns <trr>tHCX²S Hig</trr>	tCHCL ²	ON.	Clock Fall Time ³ (peak to peak)	0.1	110	N.COm	V/ns
tbvcHtbsuData In Setup Time5InstcHDXtpHData In Hold Time5InstcHBH \overline{S} Active Hold Time (relative to C)10InstsHCH \overline{S} Not Active Setup Time (relative to C)10InstsHCH \overline{S} Deselect Time100InstsHSLtcSH \overline{S} Deselect Time100InstsHQ2 ² tbisOutput Disable Time100InstcLQVtvClock Low to Output ValidInsInstcLQXtHOOutput Hold Time (relative to C)10InsthLCHHOLD Setup Time (relative to C)10InstHLCHHOLD Setup Time (relative to C)10InstHHCHHOLD Setup Time (relative to C)10InstHHCHHOLD Doutput Low-Z10InstHHQ2 ² tLzHOLD to Output High-Z20InstsHL2 ⁴ Write Protect Setup Time20InstsHL2 ⁴ Write Protect Setup Time100InstsHL4Write Protect Setup Time3 μ stsHL4S High to Standby Mode without Electronic3 μ stsH2 ⁴ S High to Standby Mode without Electronic1414	t _{SLCH}	tcss	S Active Setup Time (relative to C)	10	1	oy.cox	ns
tcHDXtDHData In Hold Time5nstcHSH \overline{S} Active Hold Time (relative to C)10nstSHCH \overline{S} Not Active Setup Time (relative to C)10nstSHCH \overline{S} Not Active Setup Time (relative to C)10nstSHSLtCSH \overline{S} Deselect Time100nstSHQ2totsOutput Disable Time100nstCLOVtVClock Low to Output Valid15nstCLOVtVClock Low to Output Valid10nstLCHHOUD Setup Time (relative to C)10nstHCHHOLD Betup Time (relative to C)10nstHHCHHOLD Hold Time (relative to C)10nstHHCHHOLD Detup Time (relative to C)10nstHHCHHOLD Doutput Low-Z10nstHHQ2tLzHOLD to Output High-Z20nstMHSL4Write Protect Setup Time20nstSHML4Write Protect Hold Time100nstSHML4Write Protect Hold Time100nstSHWL4S High to Standby Mode without Electronic3 μs tRES12S High to Standby Mode with Electronic14u	tCHSL	I.COM.	S Not Active Hold Time (relative to C)	10 🔨	AM.	nov.co	ns
tchsh \overline{S} Active Hold Time (relative to C)10nstshCH \overline{S} Not Active Setup Time (relative to C)10nstshCH \overline{S} Not Active Setup Time (relative to C)10nstshSLtcSH \overline{S} Deselect Time100nstshQ2 ² tbisOutput Disable Time100nstcLQVtvClock Low to Output Valid15nstcLQXthOOutput Hold Time0nsthLCHHOLD Setup Time (relative to C)10nsthHCHHOLD Hold Time (relative to C)10nsthHCHHOLD Setup Time (relative to C)10nsthHCHHOLD Doutput High-Z10nsthHQ2 ² tLzHOLD to Output High-Z20nsthHA2 ⁴ Write Protect Setup Time20nstsHP4 ⁴ Write Protect Hold Time100nstsHP2 \overline{S} High to Standby Mode without Electronic3 μ stres1 ² \overline{S} High to Standby Mode with Electronic1414	t _{DVCH}	tDSU	Data In Setup Time	5	NAM.	. NOY.C	ns
tshCH \overline{S} Not Active Setup Time (relative to C)10nstshSLtcSH \overline{S} Deselect Time100nstshQ2toIsOutput Disable Time10015nstcLQVtvClock Low to Output Valid15nstcLQXthOOutput Hold Time0nsthLCHHOLD Setup Time (relative to C)10nstcHHHHOLD Fold Time (relative to C)10nsthHCHHOLD Netup Time (relative to C)10nstcHHLHOLD Netup Time (relative to C)10nstHCHHOLD Netup Time (relative to C)10nstHHCHHOLD Netup Time (relative to C)10nstHHQXtLZHOLD to Output Low-Z10nstHHQXthZHOLD to Output High-Z20nstype?S High to Deep Power-down Mode100nstgP2S High to Standby Mode without Electronic3 μ stracs1S High to Standby Mode with Electronic18uc	t _{CHDX}	t _{DH}	Data In Hold Time	5	MAN	.100Y.	ns
t_{SHSL} t_{CSH} \overline{S} Deselect Time100ns t_{SHQZ}^2 t_{DIS} Output Disable Time10015ns t_{CLQV} t_V Clock Low to Output Valid15ns t_{CLQX} t_{HO} Output Hold Time0ns t_{HLCH} HOLD Setup Time (relative to C)10ns t_{HLCH} HOLD Hold Time (relative to C)10ns t_{HHCH} HOLD Setup Time (relative to C)10ns t_{HHCH} HOLD Dold Time (relative to C)10ns t_{HHCH} HOLD Setup Time (relative to C)10ns t_{HHCH} HOLD Dold Time (relative to C)10ns t_{HHCA}^2 t_{LZ} HOLD to Output Low-Z10ns t_{HLQZ}^2 t_{LZ} HOLD to Output High-Z20ns t_{WHSL}^4 Write Protect Setup Time20nsns t_{SHWL}^4 Write Protect Hold Time100nsns t_{DP}^2 \overline{S} High to Deep Power-down Mode3 μ_S t_{RES1}^2 \overline{S} High to Standby Mode without Electronic3 μ_S	t _{CHSH}	NCO'	S Active Hold Time (relative to C)	10	WW	YOOT	ns
tstuctotaOutput Disable Time15ns t_{SHQZ}^2 totsOutput Disable Time15ns t_{CLQV} tvClock Low to Output Valid15ns t_{CLQX} thoOutput Hold Time010ns t_{LCH} HOLD Setup Time (relative to C)1010nst_CHHHHOLD Hold Time (relative to C)10nsnst_HHCHHOLD Setup Time (relative to C)10nsnst_HHCHHOLD Hold Time (relative to C)10nsnst_HHQX^2t_LzHOLD to Output Low-Z10nst_HLQ2^2tHzHOLD to Output High-Z20nst_WHSL^4Write Protect Setup Time20nst_DP^2S High to Deep Power-down Mode3 μ st_RES1^2S High to Standby Mode without Electronic3 μ s	tsнсн	LOO L. C	S Not Active Setup Time (relative to C)	10	WW	N.100	ns
truetruetruetruetruetcLQVtvClock Low to Output Valid15nstcLQXtHOOutput Hold Time0nstHLCHHOLD Setup Time (relative to C)10nstCHHHHOLD Hold Time (relative to C)10nstHHCHHOLD Setup Time (relative to C)10nstHHCHHOLD Detup Time (relative to C)10nstHHQXtLzHOLD to Output Low-Z10nstHLQ2tLzHOLD to Output High-Z20nstSHWL4Write Protect Setup Time20nstDP ² S High to Deep Power-down Mode3 μ stRES1 ² S High to Standby Mode without Electronic3 μ s	tSHSL	t _{CSH}	S Deselect Time	100	W	N.N. 10	ns
tcLQXtHOOutput Hold Time0nstHLCHHOLD Setup Time (relative to C)10nstCHHHHOLD Hold Time (relative to C)10nstHHCHHOLD Setup Time (relative to C)10nstHHCHHOLD Hold Time (relative to C)10nstCHHLHOLD Hold Time (relative to C)10nstCHHLHOLD Hold Time (relative to C)10nstHCHHOLD to Output Low-Z10nstHLQZ ² tHZHOLD to Output High-Z20nstWHSL ⁴ Write Protect Setup Time20nstSHWL ⁴ Write Protect Hold Time100nstDP ² S High to Deep Power-down Mode3 μ stRES1 ² S High to Standby Mode with Electronic3 μ s	t _{SHQZ} ²	t _{DIS}	Output Disable Time	WT	7	15	ns
tHLCHHOLD Setup Time (relative to C)10nstCHHHHOLD Hold Time (relative to C)10nstHHCHHOLD Setup Time (relative to C)10nstCHHLHOLD Hold Time (relative to C)10nstCHHLHOLD Hold Time (relative to C)10nstCHHLHOLD To Output Low-Z10nstHLQZ ² tLzHOLD to Output Low-Z15tHLQZ ² tHzHOLD to Output High-Z20nstWHSL ⁴ Write Protect Setup Time20nstDP ² S High to Deep Power-down Mode3 μ stRES1 ² S High to Standby Mode with Electronic Signature Read3 μ s	t _{CLQV}	t _V	Clock Low to Output Valid	WT	-	15	ns
tCHHHHOLD Hold Time (relative to C)10nstHHCHHOLD Setup Time (relative to C)10nstCHHLHOLD Hold Time (relative to C)10nstHHQXtLzHOLD to Output Low-Z1015tHLQZtHZHOLD to Output High-Z20nstWHSLWrite Protect Setup Time20nstSHWLS High to Deep Power-down Mode100nstRES1S High to Standby Mode without Electronic Signature Read3 μ s	tCLQX	tно	Output Hold Time	0		MMM.	ns
tHHCHHOLD Setup Time (relative to C)10nstCHHLHOLD Hold Time (relative to C)10nstHHQXtLzHOLD to Output Low-Z1015tHLQZtHZHOLD to Output High-Z20nstWHSLWrite Protect Setup Time20nstSHWLWrite Protect Hold Time100nstDPS High to Deep Power-down Mode3 μ stRES1S High to Standby Mode with Electronic3 μ s	t _{HLCH}	WW.IO	HOLD Setup Time (relative to C)	10	N I	WWV	ns
tCHHLHOLD Hold Time (relative to C)10ns t_{HHQX}^2 t_{LZ} HOLD to Output Low-Z1015ns t_{HLQZ}^2 t_{HZ} HOLD to Output High-Z20ns t_{HLQZ}^4 Write Protect Setup Time20nsns t_{SHWL}^4 Write Protect Hold Time100nsns t_{DP}^2 S High to Deep Power-down Mode3 μ s t_{RES1}^2 S High to Standby Mode without Electronic3 μ s	tсннн	I.WW.I	HOLD Hold Time (relative to C)	10	N	WW	ns
t_{HHQX}^2 t_{LZ} HOLD to Output Low-Z15ns t_{HLQZ}^2 t_{HZ} HOLD to Output High-Z20ns t_{WHSL}^4 Write Protect Setup Time20ns t_{SHWL}^4 Write Protect Hold Time100ns t_{DP}^2 \overline{S} High to Deep Power-down Mode3 μs t_{RES1}^2 \overline{S} High to Standby Mode without Electronic3 μs	tннсн	WWW.	HOLD Setup Time (relative to C)	10	W	WV	ns
t_{HLQZ}^2 t_{HZ} $HOLD$ to Output High-Z20ns t_{WHSL}^4 Write Protect Setup Time20ns t_{SHWL}^4 Write Protect Hold Time100ns t_{DP}^2 \overline{S} High to Deep Power-down Mode3 μs t_{RES1}^2 \overline{S} High to Standby Mode without Electronic Signature Read3 μs	t _{CHHL}	WW	HOLD Hold Time (relative to C)	10	WT	N	ns
t_{WHSL}^4 Write Protect Setup Time20ns t_{SHWL}^4 Write Protect Hold Time100ns t_{DP}^2 \overline{S} High to Deep Power-down Mode3 μs t_{RES1}^2 \overline{S} High to Standby Mode without Electronic Signature Read3 μs t_{RES1}^2 \overline{S} High to Standby Mode with Electronic18 μs	t _{HHQX} ²	t _{LZ}	HOLD to Output Low-Z	NY.CON	WT	15	ns
t_{WHSL}^4 Write Protect Setup Time20ns t_{SHWL}^4 Write Protect Hold Time100ns t_{DP}^2 \overline{S} High to Deep Power-down Mode3 μs t_{RES1}^2 \overline{S} High to Standby Mode without Electronic Signature Read3 μs t_{RES1}^2 \overline{S} High to Standby Mode with Electronic18 μs	t _{HLQZ} 2	t _{HZ}	HOLD to Output High-Z	NOY.CO	WT.I.	20	ns
tDP 2\$\overline{S}\$ High to Deep Power-down Mode3μstRES1 2\$\overline{S}\$ High to Standby Mode without Electronic Signature Read3μst = 2\$\overline{S}\$ High to Standby Mode with Electronic11		W	Write Protect Setup Time	20.0	T.M	N.	ns
t _{RES1} ² S̄ High to Standby Mode without Electronic Signature Read 3 μs t 2 S̄ High to Standby Mode with Electronic 1.8 μs	t _{SHWL} ⁴	V	Write Protect Hold Time	100	COM!	W	ns
tRES1 Signature Read Signature Read 1 2 S High to Standby Mode with Electronic 1.8	t _{DP} ²	-	S High to Deep Power-down Mode	N.100Y	Mo.	3	μs
	t _{RES1} 2			W.100	N.CON	3	μs
	t _{RES2} ²			MW.IO.		1.8	μs

Table 17. AC Characteristics (25MHz Operation, Device Grade 6 or 3)

Note: 1. t_{CH} + t_{CL} must be greater than or equal to 1/ f_C

2. Value guaranteed by characterization, not 100% tested in production.

3. Expressed as a slew-rate.

4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.

5. For device grade 3, this is Preliminary Data



M25P40

	4	0MHz available for products marked since week Test conditions specified in Table 9. and	Table 16.	, only		
Symbol	Alt.	Parameter	Min.	Тур.	Max.	Unit
fc	fc	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.	ox.col	40	MHz
f _R	WT.	Clock Frequency for READ instructions	D.C.	004.0	20	MHz
t _{CH} ¹	tCLH	Clock High Time	11	100Y.C	OM.T	ns
t _{CL} 1	tCLL	Clock Low Time	11	V.100Y.	COM.	ns
tCLCH ²	OM.TW	Clock Rise Time ³ (peak to peak)	0.1	W.1005	COM	V/ns
t _{CHCL} ²	COM.T	Clock Fall Time ³ (peak to peak)	0.1	VN.100		V/ns
t _{SLCH}	tcss	S Active Setup Time (relative to C)	5	WW.IC		ns
tCHSL	COM	S Not Active Hold Time (relative to C)	5	WW.	N C	ns
t _{DVCH}	tDSU	Data In Setup Time	2	WW	100 7.	ns
t _{CHDX}	tDH	Data In Hold Time	5		1.100 2	ns
tCHSH	001.00	S Active Hold Time (relative to C)	5		W.1003	ns
tshch	1001.0	S Not Active Setup Time (relative to C)	5		W.100	ns
tSHSL	tCSH	S Deselect Time	100		NW.10	ns
t _{SHQZ} ²	tDIS	Output Disable Time	I.TW	1	9	ns
tCLQV	ty	Clock Low to Output Valid	M.I.		9	ns
tCLQX	tно	Output Hold Time	0	с Т		ns
thlch 🔨	1	HOLD Setup Time (relative to C)	5	-1		ns
t _{СННН}	NWW	HOLD Hold Time (relative to C)	5	N.		ns
tннсн	MM	HOLD Setup Time (relative to C)	5	L.M.		ns
t _{CHHL}	MMM	HOLD Hold Time (relative to C)	5	TW	Ń	ns
t _{HHQX} ²	tLZ	HOLD to Output Low-Z	01.0	N.T.W	9	ns
t _{HLQZ} 2	t _{HZ}	HOLD to Output High-Z	001.00	M.T.Y	9	ns
t _{WHSL} ⁴	N	Write Protect Setup Time	20	OM.T		ns
t _{SHWL} ⁴	N	Write Protect Hold Time	100	COM.3	NT-	ns
t _{DP} ²		S High to Deep Power-down Mode	N.100 .	COM	3	μs
t _{RES1} ²		S High to Standby Mode without Electronic Signature Read	1W.100	N.CON	3	μs
t _{RES2} 2		S High to Standby Mode with Electronic Signature Read	1 4 4 7 7 1		1.8	μs

W.100Y.COM.TW Table 18. AC Characteristics (40MHz Operation, Device Grade 6)

Note: 1. t_{CH} + t_{CL} must be greater than or equal to 1/ f_C

2. Value guaranteed by characterization, not 100% tested in production.

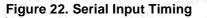
3. Expressed as a slew-rate.

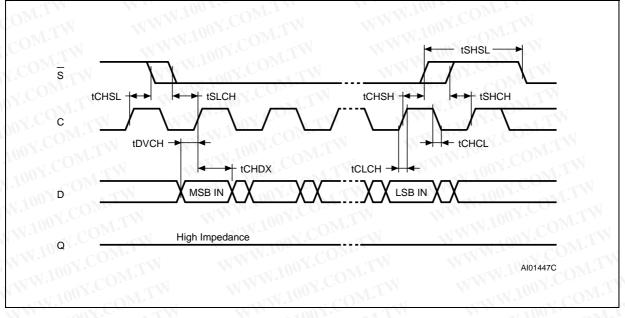
A. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
 Details of how to find the date of marking are given in Application Note, *AN1995*.

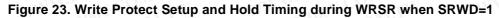
V.100Y.COM.TW

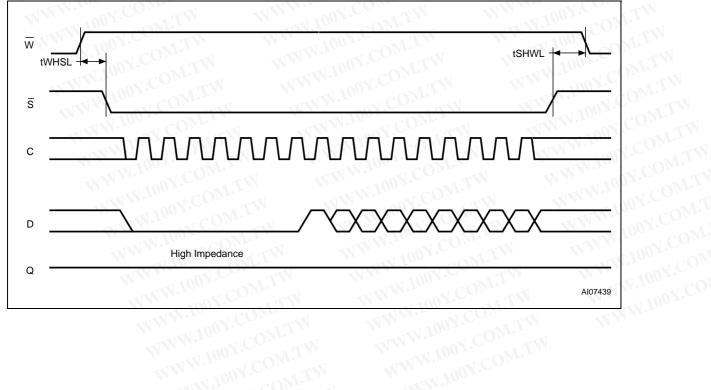






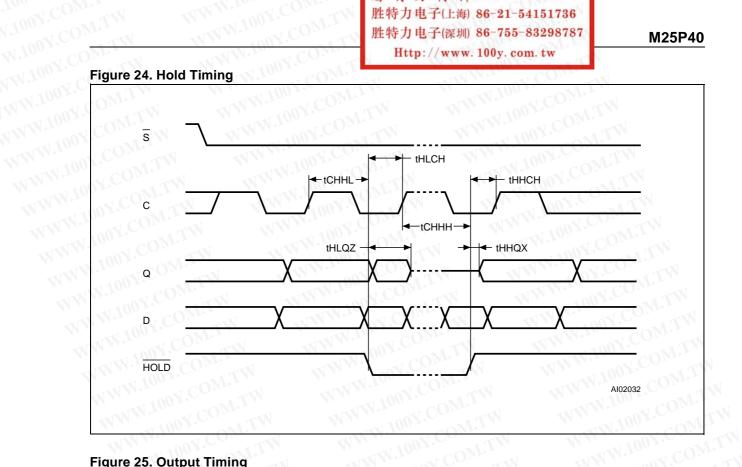






57

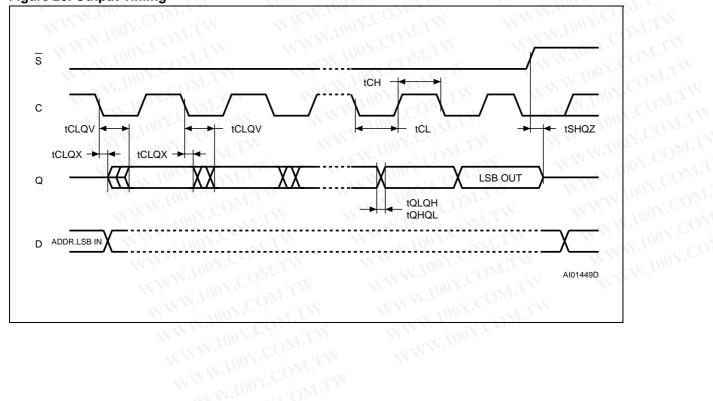
M25P40



TWW.100Y.COM.TW

Figure 25. Output Timing

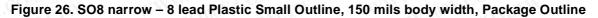
N.100Y.COM.TW

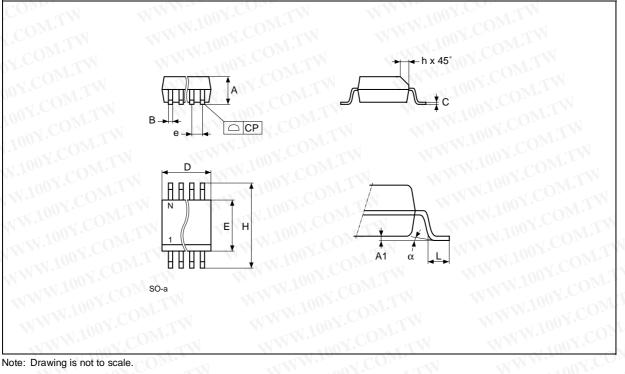


57

M25P40

PACKAGE MECHANICAL



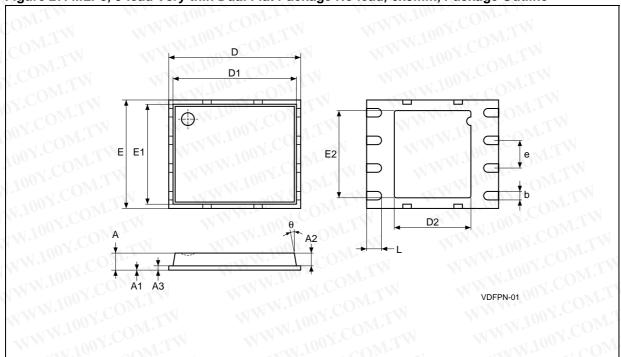


Cumb	MONY.COM	mm		N.LU. TV	inches	
Symb.	Тур.	Min.	Max.	Тур.	🔨 Min. 📢	Max.
A	W. LOT N.CC	1.35	1.75	ON.COM	0.053	0.069
A1	V.W.LOWNY.C	0.10	0.25	LOOX.COM	0.004	0.010
В	WW.IOUN	0.33	0.51	V.COP	0.013	0.020
С	WW.IOO	0.19	0.25	N.P. CC	0.007	0.010
D	WW.100	4.80	5.00	N.V. CC	0.189	0.197
E	WW.100	3.80	4.00	WW.IOONC	0.150	0.157
е	1.27	COM.1	-	0.050	CONFILM	
Н	L.WW.	5.80	6.20	WW.100	0.228	0.244
h	WW	0.25	0.50	WW.100	0.010	0.020
L	W	0.40	0.90	W.100	0.016	0.035
α	N.	0°	8°	1.11	0°	8°
Ν	4m	8	ON.TW		8	
CP	N,	1007.6	0.10			0.004

A7

Table 19. SO8 narrow - 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data







57

V.100Y.COM.TW

Symb.		mm		COM.	inches	
Symb.	Тур.	Min.	Max.	Тур.	Min.	Max.
A	0.85	T.I.M	1.00	0.0335		0.0394
A1	N 100Y.C.C.	0.00	0.05	DOX.COM.	0.0000	0.0020
A2	0.65	M.TW	WW	0.0256	Tu	WIG
A3 🔨	0.20	WI.W	MM	0.0079	I.I.W	WIT
b 🔨	0.40	0.35	0.48	0.0157	0.0138	0.0189
D	6.00	.Com TW	MM	0.2362	M.TW	2111
D1	5.75	Y.COMITY	W	0.2264	WILL	AN N
D2	3.40	3.20	3.60 📢	0.1339	0.1260	0.1417
E	5.00	NY.COM.	· W	0.1969	.COMTW	
E1	4.75	ON.COM.	WT	0.1870	Y.COMTY	
E2	4.00	3.80	4.20	0.1575	0.1496	0.1654
е	1.27	1.100 CO	W.	0.0500	N.COM.	
L	0.60	0.50	0.75	0.0236	0.0197	0.0295
θ		W.100 C	12°			12°

Table 20. MLP8, 8-lead Very thin Dual Flat Package No lead, 6x5mm, Package Mechanical Data

Note: Drawing is not to scale.

WWW.100

V.100Y.COM.TW M25P40

PART NUMBERING

Table 21. Ordering Information Scheme

Table 21. Ordering Information Scheme		
Example:	M25P40 –	V MN 6
RUCENTRY WWW 1002.0	T.IM	M 1001.
Device Type	NT TY	YODE WW
M25P = Serial Flash Memory for Code Storage	ON.	WWW.L
101. WILLIN WILLION	COM.	N.100
Device Function	CO. TW	NN 10
40 = 4 Mbit (512K x 8)		WWW.1
Operating Voltage		WWW.
$V = V_{CC} = 2.7$ to 3.6V	CON.TH	
Package		N WN
MN = SO8 (150 mil width)	Too CON.	
MP = VDFPN8 6x5mm (MLP8)		LM A.
		WW WT
Device Grade	N.100 COM	
6 = Industrial temperature range, -40 to 85 °C. Device tested with standard test flow		
3 ⁴ = Device tested with High Reliability Certified Flo Automotive temperature range (-40 to 125 °C)	ow ¹ .	
Option	W.100Y.C	COM.TW
blank = Standard Packing		
T = Tape and Reel Packing		
Plating Technology		
blank = Standard SnPb plating	WW.10	N.COM
P^2 = Lead-Free and RoHS compliant		

 G^3 = Lead-Free, RoHS compliant, Sb₂O₃-free and TBBA-free

100X.COM.TW .100X.COM.T Note: 1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.

- 2. Available for SO8 package only

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office. WWW.100Y.COM WWW.100Y.COM.

100Y.COM.

M25P40

W.100Y.COM.TW NW.100Y.COT **REVISION HISTORY**

N.100Y.COM.TW

NN.			ION THE OWNER AND THE TOPY OF
WW.100	Table 22. Do	cumer	nt Revision History
NWW.IO	Date	Rev.	Description of Revision
WWW.1	12-Apr-2001	1.0	Document written
WWW	25-May-2001	1.1	Serial Paged Flash Memory renamed as Serial Flash Memory
WWY	N100X.COM	LM.	Changes to text: Signal Description/Chip Select; Hold Condition/18 Release from Power-down and Read Electronic Signature (RES);

WW.100Y.COM.TW

N.COM.TW

OM.TW

12-Apr-2001	1.0	Document written
25-May-2001	1.1	Serial Paged Flash Memory renamed as Serial Flash Memory
11-Sep-2001	1.2	Changes to text: Signal Description/Chip Select; Hold Condition/1st para; Protection modes; Release from Power-down and Read Electronic Signature (RES); Power-up Repositioning of several tables and illustrations without changing their contents Power-up timing illustration; SO8W package removed Changes to tables: Abs Max Ratings/V _{IO} ; DC Characteristics/V _{IL}
16-Jan-2002	1.3	FAST_READ instruction added. Document revised with new timings, V _{WI} , I _{CC3} and clock slew rate. Descriptions of Polling, Hold Condition, Page Programming, Release for Deep Powerdown made more precise. Value of $t_W(max)$ modified.
12-Sep-2002	1.4	Clarification of descriptions of entering Stand-by Power mode from Deep Power-down mode, and of terminating an instruction sequence or data-out sequence. VFQFPN8 package (MLP8) added. Document promoted to Preliminary Data.
13-Dec-2002	1.5	Typical Page Program time improved. Deep Power-down current changed. Write Protect setup and hold times specified, for applications that switch Write Protect to exit the Hardware Protection mode immediately before a WRSR, and to enter the Hardware Protection mode again immediately after.
12-Jun-2003	1.6	Document promoted from Preliminary Data to full Datasheet
24-Nov-2003	2.0	Table of contents, warning about exposed paddle on MLP8, and Pb-free options added. 40MHz AC Characteristics table included as well as 25MHz. $I_{CC3}(max)$, $t_{SE}(typ)$ and $t_{BE}(typ)$ values improved. Change of naming for VDFPN8 package
12-Mar-2004	3.0	Automotive range added. Soldering temperature information clarified for RoHS compliant devices
05-Aug-2004	4.0	Device Grade information clarified. Data-retention measurement temperature corrected. Details of how to find the date of marking added.

A7

V.100Y.COM.TW M25P40 NW.100Y.CO

WW.100X.COM.TW

WWW.100Y.COM.TW

WWW.100Y.C

勝特力材料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

WWW.100Y.COM Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequ of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is c by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are s to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products a authorized for use as critical components in life support devices or systems without express written approval of STMicroelectron

> The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

> > © 2004 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

47/

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Ja Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America www.st.com