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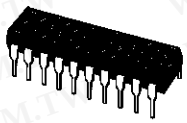
SGS-THOMSON MICROELECTRONICS

M54HC356
M74HC356

8 CHANNEL MULTIPLEXER/REGISTER WITH LATCHES (3-STATE)

- HIGH SPEED
  t_{PD} = 25 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS356



B1R
(Plastic Package)

F1R
(Ceramic Package)

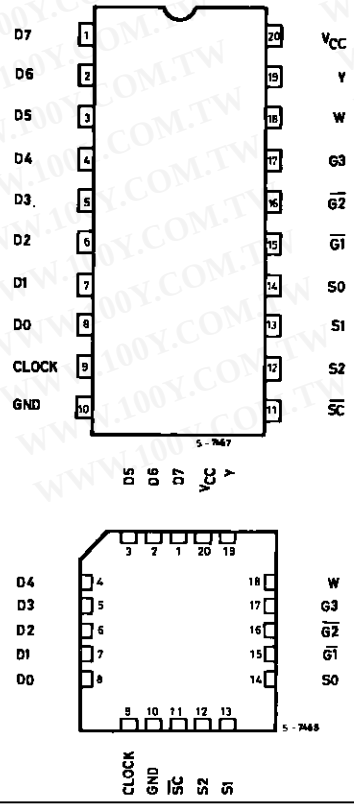
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC356F1R	M74HC356M1R
M74HC356B1R	M74HC356C1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

The M54/74HC356 is a high speed CMOS 8-CHANNEL MULTIPLEXER/REGISTER (3-State) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.

This device contains an 8 channel digital multiplexer with an 8-bit input data register and a 3-bit address input register with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) is determineted by the address data.

The information at the data inputs (D0 to D7) is stored in the 8-bit flip-flop at the positive going edge of clock input (CLOCK). The information at the address inputs (S0 to S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when input $\overline{G1}$ is held high, input $\overline{G2}$ is held high or input G3 is held low. This device is suitable for interfacing with bus lines in a bus organized system. The M54/74HC356 is similar in function to the M54/74HC354, which has an 8-bit latch as the data register instead of an 8-bit flip-flop. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

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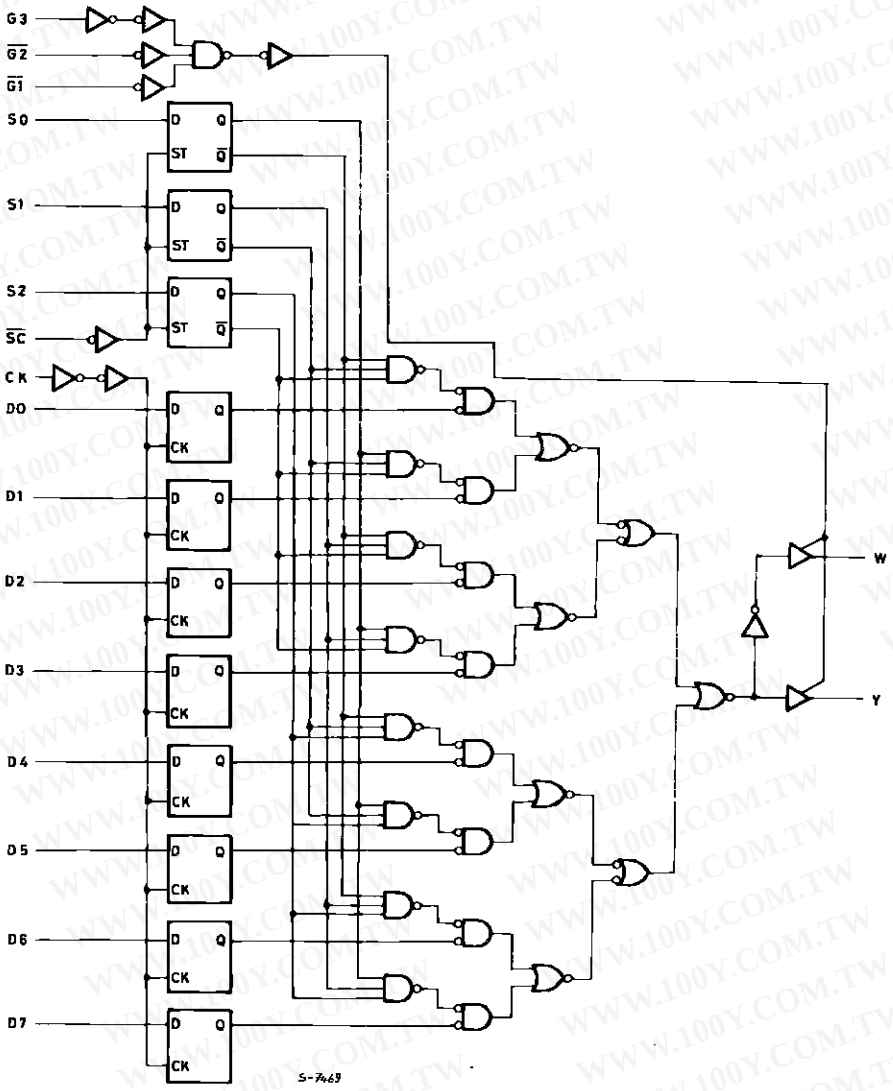
LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE

Qn: DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE

TRUTH TABLE OF INTERNAL LATCH (FLIP FLOP)

D	CK	Q
L	⌐¯	L
H	⌐¯	H
X	¯⌐	Qn

X: DON'T CARE

Qn: NO CHANGE

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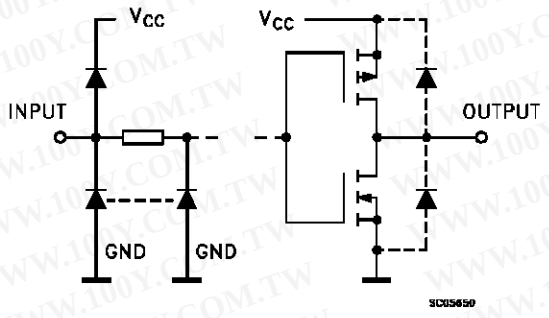
TRUTH TABLE

INPUTS							W	Y
SELECT *			CLOCK	OUTPUT ENABLES				
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3		
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	↓	L	L	H	$\overline{D0n}$	D0n
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	↓	L	L	H	$\overline{D1n}$	D1n
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	↓	L	L	H	$\overline{D2n}$	D2n
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	↓	L	L	H	$\overline{D3n}$	D3n
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	↓	L	L	H	$\overline{D4n}$	D4n
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	↓	L	L	H	$\overline{D5n}$	D5n
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	↓	L	L	H	$\overline{D6n}$	D6n
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	↓	L	L	H	$\overline{D7n}$	D7n

X: DON'T CARE Z: HIGH IMPEDANCE *: This column shows the input adress setup with SC LOW.
D1 ..... D7: The level of steady state inputs at input D1 through D7, respectively, at the time of the LOW to HIGH transition of the clock.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



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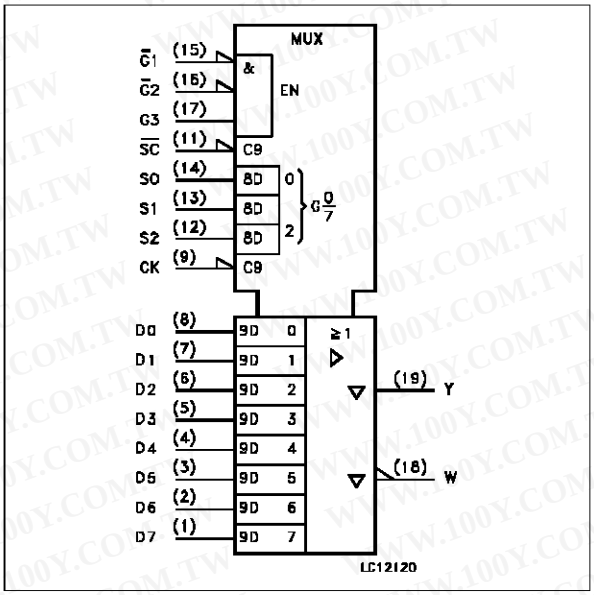
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
8, 7,, 6, 5, 4, 3, 2, 1	D0 to D7	Data Inputs
9	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
11	$\overline{SC}$	Latch Enable Input (Active LOW)
14, 13, 12	S0, S1, S2	Select Inputs
15, 16	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs (Active LOW)
17	G3	Output Enable Inputs (Active HIGH)
18	W	3 State Multiplexer Output (Active LOW)
19	Y	3 State Multiplexer Output (Active HIGH)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

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DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Y, W)	2.0	50			99	240		300		360	ns
		4.5				28	48		60		72	
		6.0				22	41		51		61	
		2.0	150			117	280		350		420	ns
		4.5				33	56		70		84	
		6.0				26	48		60		71	

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (Sn - Y, W)	2.0	50			111	260		325		390	ns
		4.5				32	52		65		78	
		6.0				24	44		55		66	
		2.0	150			128	300		375		450	ns
		4.5				37	60		75		90	
		6.0				28	51		64		77	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{SC}$ - Y, W)	2.0	50			115	270		340		405	ns
		4.5				33	54		68		81	
		6.0				25	46		58		69	
		2.0	150			132	310		390		465	ns
		4.5				38	62		78		93	
		6.0				29	53		66		79	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		48	125		155		190	ns
		4.5				14	25		31		38	
		6.0				11	21		26		32	
		2.0	150	R_L = 1 KΩ		65	165		205		250	ns
		4.5				19	33		41		50	
		6.0				15	28		35		43	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		43	155		195		235	ns
		4.5				18	31		39		47	
		6.0				16	26		33		40	
f_{MAX}	Maximum Clock Frequency	2.0	50		6.2	20		5		4.2		ns
		4.5			31	80		25		21		
		6.0			37	82		30		25		
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0	50			25	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{SC}$)	2.0	50			13	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time (Dn)	2.0	50			21	50		65		75	ns
		4.5				4	10		113		15	
		6.0				3	9		11		13	
t_s	Minimum Set-up Time (Sn)	2.0	50			9	50		65		75	ns
		4.5				2	10		13		15	
		6.0				2	9		11		13	
t_h	Minimum Hold Time (Dn) (Sn)	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					59						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

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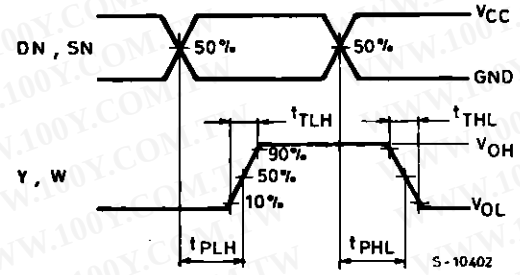
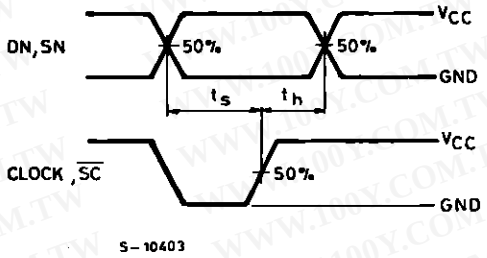
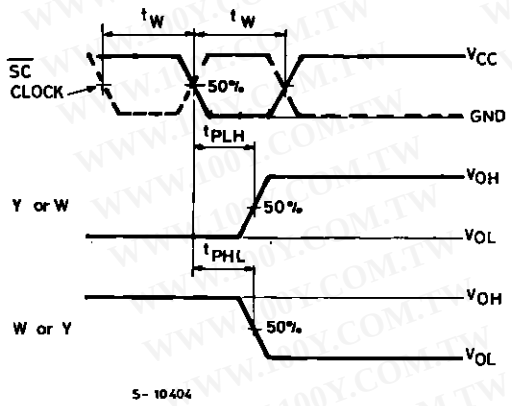
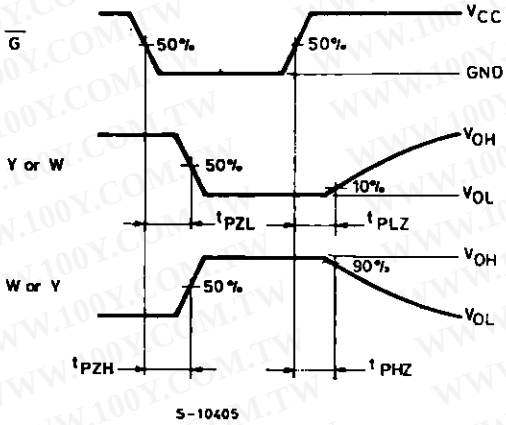
SWITCHING CHARACTERISTICS TEST WAVEFORM

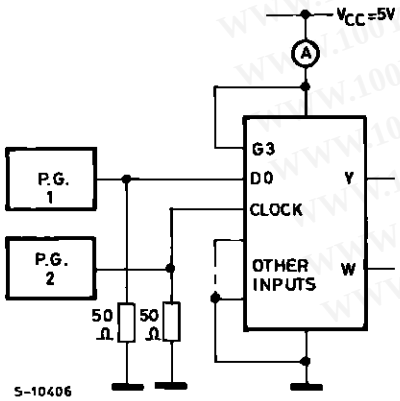


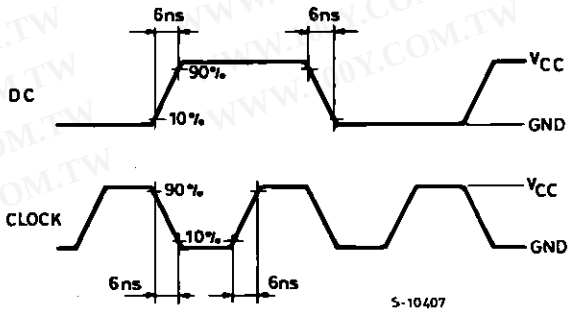






TEST CIRCUIT WAVEFORM I_{CC} (Opr.)





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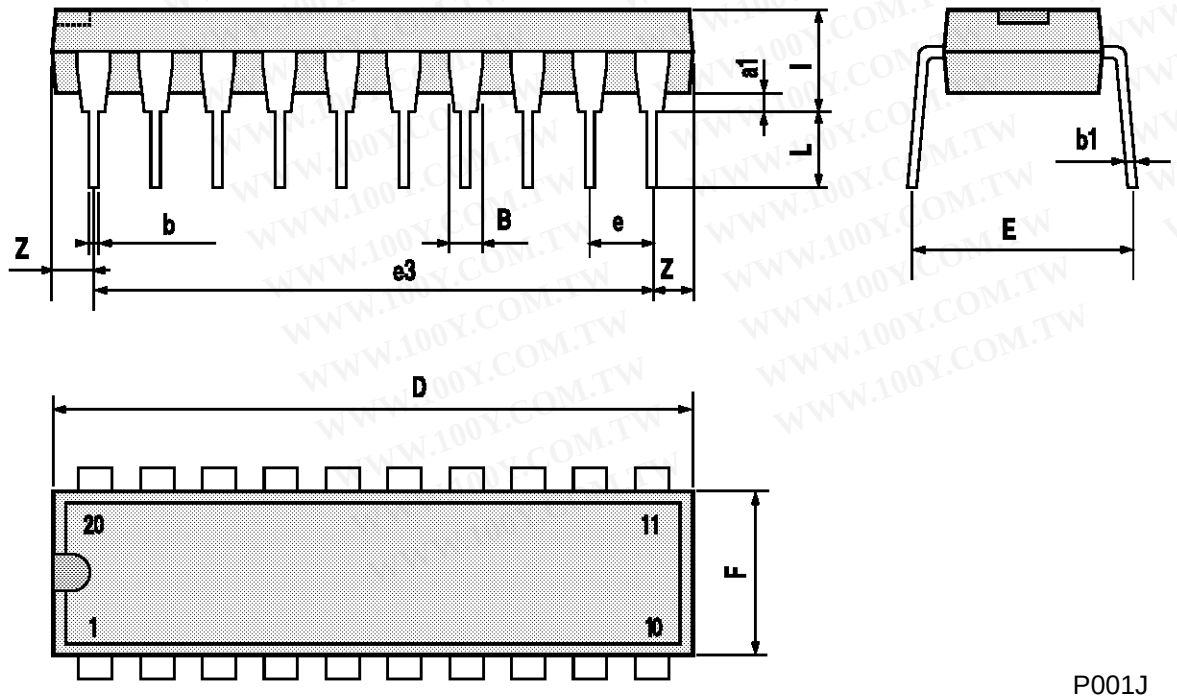
Plastic DIP20 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

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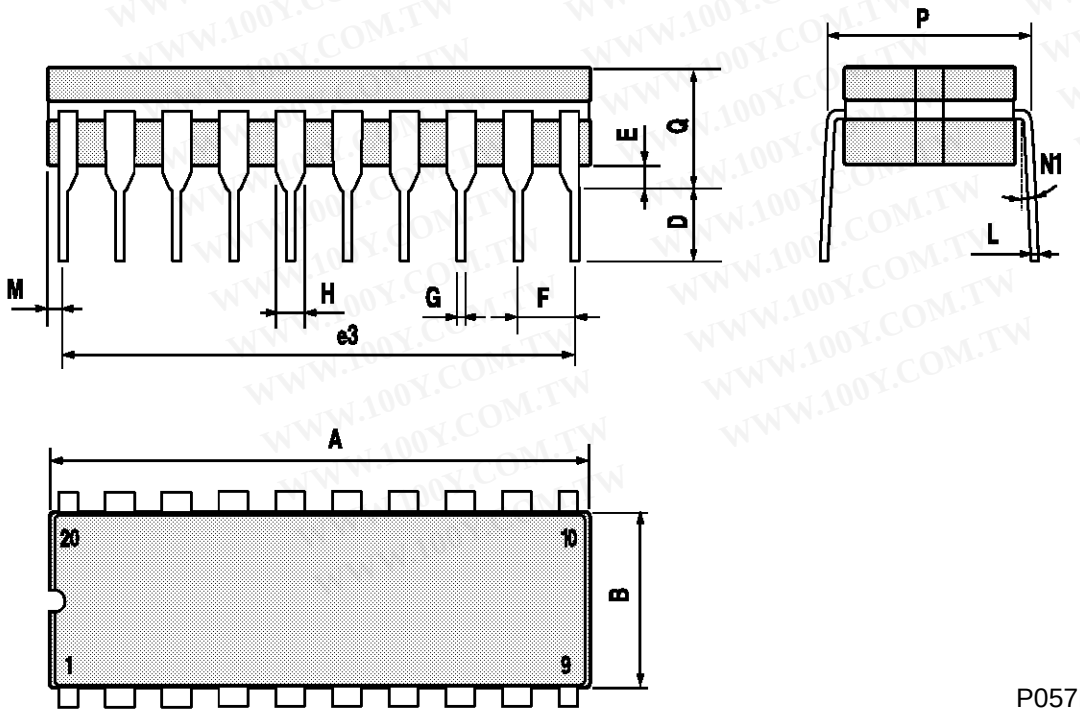
Ceramic DIP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			25			0.984
B			7.8			0.307
D		3.3			0.130	
E	0.5		1.78	0.020		0.070
e3		22.86			0.900	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N1	4° (min.), 15° (max.)					
P	7.9		8.13	0.311		0.320
Q			5.71			0.225



P057H

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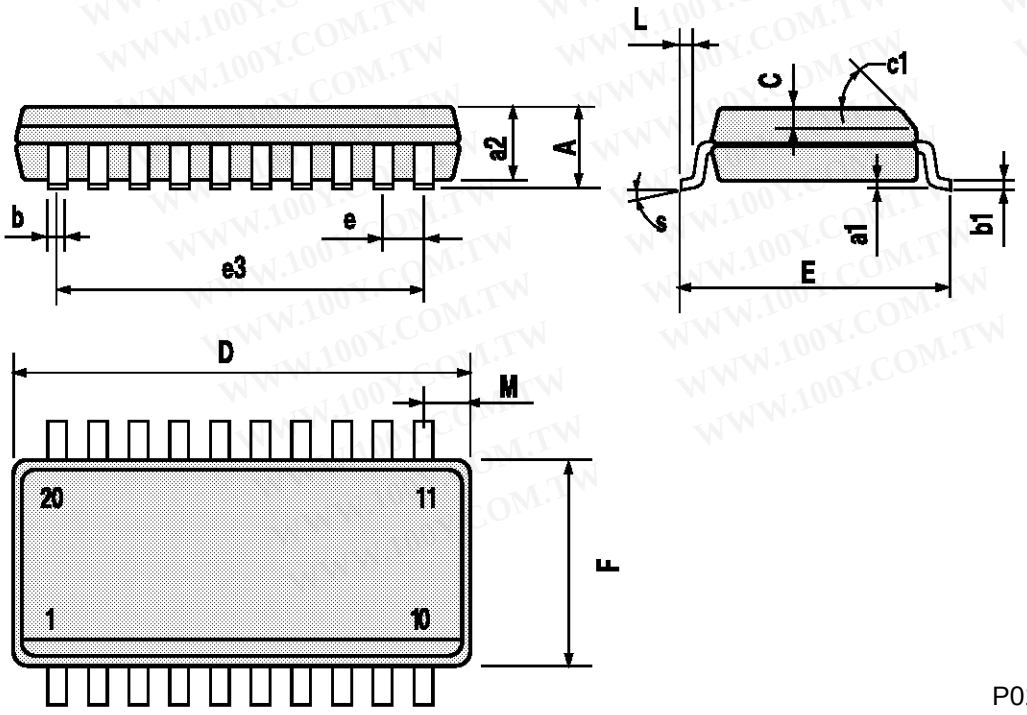
SO20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8° (max.)					



P013L

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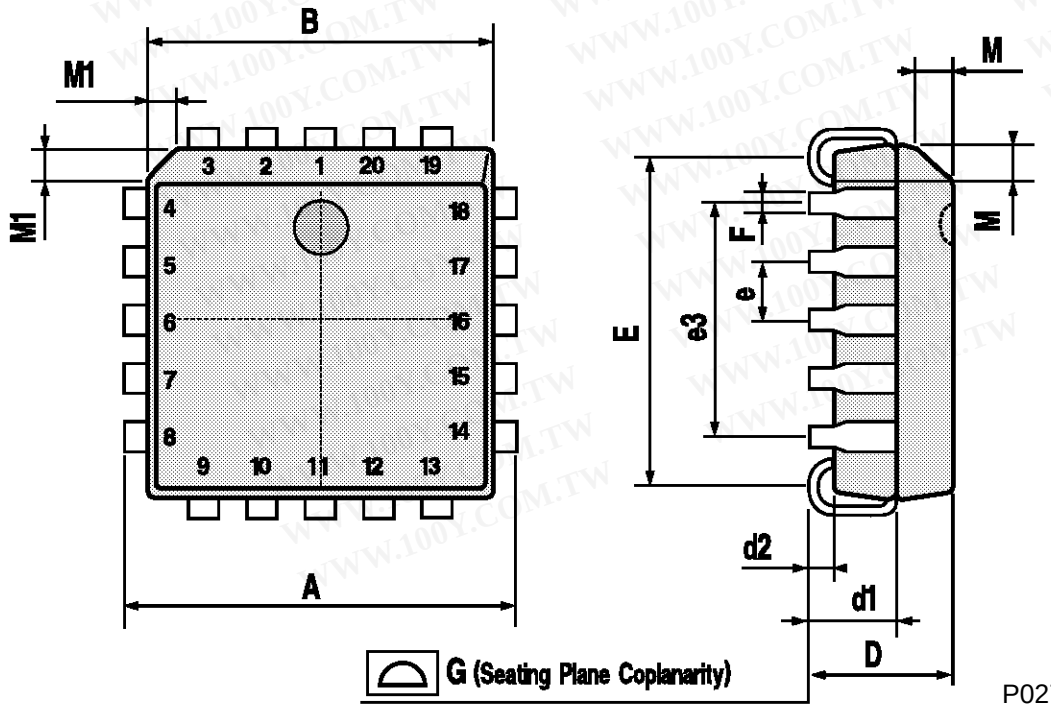
PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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