勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

8-Channel Data Selector

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Diode Protection on All Inputs
- Single Supply Operation
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range



ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS

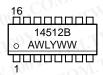


PDIP-16 P SUFFIX CASE 648



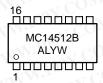


SOIC-16 D SUFFIX CASE 751B





SOEIAJ-16 F SUFFIX CASE 966



A

= Assembly Location

WL, L = Wafer Lot YY, Y = Year WW, W = Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	W. 700
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note NO TAG)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating: Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ORDERING INFORMATION

Device	Package	Shipping	
MC14512BCP	PDIP-16	2000/Box	
MC14512BD	SOIC-16	48/Rail	
MC14512BDR2	SOIC-16	2500/Tape & Reel	
MC14512BF	SOEIAJ-16	See Note 1.	
MC14512BFL1	SOEIAJ-16	See Note 1.	

 For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

© Semiconductor Components Industries, LLC, 2000

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www. 100y. com. tw

WWW.100Y.COM.TW

СВ	FAM.	UTH TABL	Disable	Z C	Http://ww
100		EM		4007.	MITW
0 0		0	0	X0 X1	WTI
0 1			0	X1 X2	COM
0 1		0 0	0	X3	COM.T.
1 0	0	0	0	X4	WI.M
1 0	-1 CC	0	0	X5	V.COM.
1 1	0.0	0	0	X6	COM
1	CON.	0	0	X7	OY. COMITY
X X	X	COA	0	0	ON COM
X X	1 X	COXI	1	High Impedance	OOX.COM.

X = Don't Care WWW.100Y.COM.TW

PIN ASSIGNMENT

Vo F	007.	10	hati
X0 [16] V _{DD}
X1 [2	15] dis
X2 [3 00	14	D Z
X3 [4	13	D C
X4 [5	12] В
X5 [6	11] A ()
X6 [7	10] INH
V _{SS} [8	9] X7
4	MAN	x 1	OOY.COM.TW

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www. 100y. com. tw

VWW.100Y.COM.TW **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V_{SS})

Y.CO. TW WW	100	V _{DD}		5°C	1	25°C	07		5°C	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ ^(4.)	Max	Min	Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V _{OL}	5.0 10 15	$\frac{CON}{N}$	0.05 0.05 0.05		0 0 0	0.05 0.05 0.05	ONETY	0.05 0.05 0.05	Vdc
$V_{in} = 0$ or V_{DD} "1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10 15	1001	4.95 9.95 14.95	EM.	Vdc
Input Voltage "0" Level $(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$ $(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$ $(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$	V _{IL}	5.0 10 15	07 <u>C</u> C	1.5 3.0 4.0	N _	2.25 4.50 6.75	1.5 3.0 4.0	V.EOM	1.5 3.0 4.0	Vdc
"1" Level $(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	V _{IH}	5.0 10 15	3.5 7.0 11	ce _M	3.5 7.0 11	2.75 5.50 8.25	MAN.	3.5 7.0 11	OM.T	Vdc
Output Drive Current $ (V_{OH} = 2.5 \text{ Vdc}) $ Source $ (V_{OH} = 4.6 \text{ Vdc}) $ $ (V_{OH} = 9.5 \text{ Vdc}) $ $ (V_{OH} = 13.5 \text{ Vdc}) $	Гон	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	° 0 <u>2</u> Y. 00 <u>Z</u> .C. 0X [°] C.O	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	- 1.7 - 0.36 - 0.9 - 2.4	.c <u>o</u> y. <u>=</u> 0)	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ Sink $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	l _{OL}	5.0 10 15	0.64 1.6 4.2	1.1 60 7	0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4	00 <u>₹</u> .C	mAdc
Input Current	l _{in}	15	N I	± 0.1	v.eo	±0.00001	± 0.1	NAM	± 1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	- I		11/10	OV.CC	5.0	7.5	NAN	V.100	pF
Quiescent Current (Per Package)	I _{DD}	5.0 10 15		5.0 10 20	10 2 7.	0.005 0.010 0.015	5.0 10 20	ZW ZW	150 300 600	μAdc
Total Supply Current ^(5.) (6.) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	OX.CO	5.0 10 15	V	MM	$I_T = (1$	0.8 μΑ/kHz) f 1.6 μΑ/kHz) f 2.4 μΑ/kHz) f	+ I _{DD}	4	MMM	μAdc
Three–State Leakage Current	OFTL.	15	N -	± 0.1	1	± 0.0001	± 0.1	_	± 3.0	μAdc

- 4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
- 5. The formulas given are for the typical characteristics only at 25°C.
- To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001. WWW.100Y.COM.TW WWW.100Y.COM.T

WW.100Y.COM.TW **SWITCHING CHARACTERISTICS** (7.) ($C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$, See Figure 1)

	1 11	MN.T.	All Types		
Characteristic	Symbol	V _{DD}	Typ (8.)	Max	Unit
Output Rise and Fall Time	t _{TLH} ,	1	001.	TW	ns
t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$	t _{THL}	5.0	100	200	
t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	01/1.7	10	50	100	
t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$,U°	15	40	80	
Propagation Delay Time (Figure 2)	t _{PLH}		1 100 at C	DIVI.	ns
Inhibit, Control, or Data to Z	TIN	5.0	330	650	
	COM	10	125	250	Ţ
100Y.C 11TN N 100	M.TW	15	85	170	
Propagation Delay Time (Figure 2)	t _{PHL}	W	A CONT	T	ns
Inhibit, Control, or Data to Z	COMP.	5.0	330	650	
	OY.CO	10	125	250	
	COMP	15	85	170	W
3–State Output Delay Times (Figure 3)	t _{PHZ} , t _{PLZ} ,	5.0	60	150	ns
"1" or "0" to High Z, and	t _{PZH} , t _{PZL}	10	35	100	
High Z to "1" or "0"	70M-7	15	30	75	17. 7

7. The formulas given are for the typical characteristics only at 25°C.

WWW.100Y.COM.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

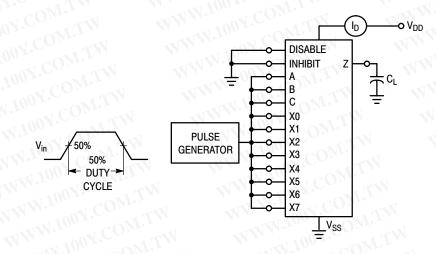


Figure 1. Power Dissipation Test Circuit and Waveform

特力材料886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

WWW.100Y.COM.TW

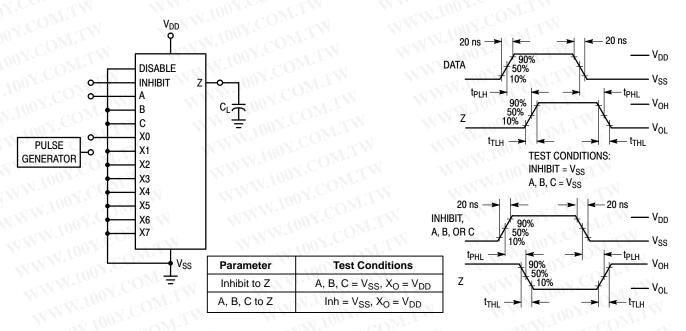


Figure 2. AC Test Circuit and Waveforms

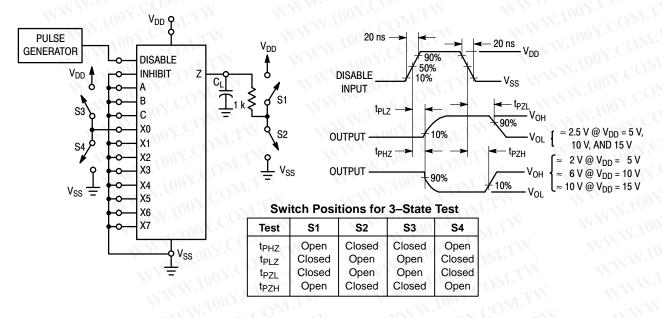


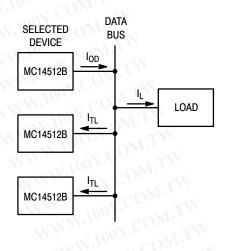
Figure 3. 3-State AC Test Circuit and Waveform

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

LOGIC DIAGRAM

В 15 DISABLE 10 INHIBIT $\rm V_{\rm DD}$ **TRANSMISSION**

特力材料886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www. 100y. com. tw



3-STATE MODE OF OPERATION

GATE

Output terminals of several MC14512B 8-Bit Data Selectors can be connected to a single date bus as shown. One MC14512B is selected by the 3-state control, and the remaining devices are disabled into a high-impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3-state or disable output leakage current, I_{TL}, and the load current, IL, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

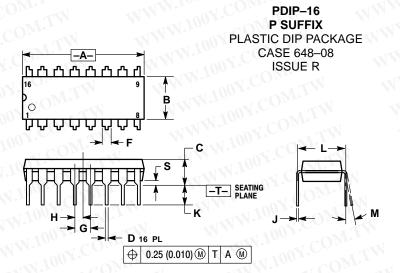
$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic state of the bus line.

PACKAGE DIMENSIONS

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787

Http://www.100y.com.tw



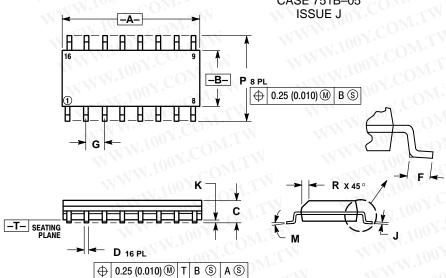
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- Y14.0M, 1992.
 CONTROLLING DIMENSION: INCH.
 DIMENSION L TO CENTER OF LEADS WHEN
 FORMED PARALLEL.
 DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 ROUNDED CORNERS OPTIONAL. 3.
- 5.

	INC	HES	MILLIM	ETERS		
DIM	MIN	MAX	MIN	MAX		
Α	0.740	0.770	18.80	19.55		
В	0.250	0.270	6.35	6.85		
С	0.145	0.175	3.69	4.44		
D	0.015	0.021	0.39	0.53		
F	0.040	0.70	1.02	1.77		
G	0.100	BSC	2.54	BSC		
Н	0.050	BSC	1.27	BSC		
J	0.008	0.015	0.21	0.38		
K	0.110	0.130	2.80	3.30		
L	0.295	0.305	7.50	7.74		
M	0°	10°	0°	10°		
S	0.020	0.040	0.51	1.01		

SOIC-16 **D SUFFIX**

PLASTIC SOIC PACKAGE CASE 751B-05



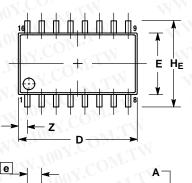
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR
- PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

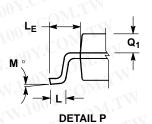
PACKAGE DIMENSIONS

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-54151736 胜特力电子(深圳) 86-755-83298787 Http://www. 100y. com. tw

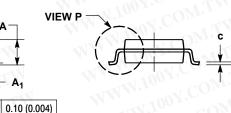
SOEIAJ-16 **F SUFFIX** PLASTIC EIAJ SOIC PACKAGE CASE 966-01



0.13 (0.005) M



ISSUE O



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14 5M 1982
- CONTROLLING DIMENSION: MILLIMETER.
- I. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 TERMINAL NUMBERS ARE SHOWN FOR

- 4. TEHMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) DAMBAR FRO INJSION STRALL BE 2008 (0.005)
 TOTAL IN EXCESS OF THE LEAD WIDTH
 DIMENSION AT MAXIMUM MATERIAL CONDITION.
 DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

11	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	<124	2.05	755	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050	BSC
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LΕ	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10 °
Q1	0.70	0.90	0.028	0.035
Z		0.78	2/2/1	0.031

are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes ON Semiconductor and without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular without further notice to any products herein. Solitate in wairanty, representation or ignarance regarding the surface of any products or any products or any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patient rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada

Email: ONlit@hibbertco.com

Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor - European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)

Email: ONlit-german@hibbertco.com

Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)

Email: ONlit-french@hibbertco.com

Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT) **English**

Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)

Email: ONlit-spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor - Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)

Toll Free from Hong Kong & Singapore: 001-800-4422-3781

Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center -32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031

Phone: 81-3-5740-2745 Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.