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Quad 2-Input NAND Gate

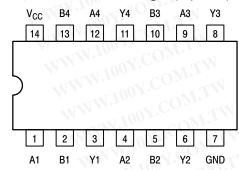
High-Performance Silicon-Gate CMOS

The MC74HC00A is identical in pinout to the LS00. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 32 FETs or 8 Equivalent Gates
- Pb–Free Packages are Available*

Pinout: 14-Lead Packages (Top View)



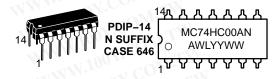
^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

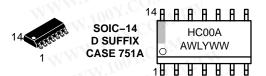


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MARKING DIAGRAMS







A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Output
Y
H
H
Н
L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	VI.	Value	Unit
V _{CC}	DC Supply Voltage (Referenced t	- 0.5 to + 7.0	V	
V _{in}	DC Input Voltage (Referenced to	-0.5 to $V_{CC} + 0.5$	٧	
V _{out}	DC Output Voltage (Referenced t	- 0.5 to V _{CC} + 0.5	V	
l _{in}	DC Input Current, per Pin	± 20	mA	
l _{out}	DC Output Current, per Pin	± 25	mA	
Icc	DC Supply Current, V _{CC} and GNI	O Pins	± 50	mA
PD	Power Dissipation in Still Air,	Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature	Tan COM.	- 65 to + 150	°C
OOY.C	Lead Temperature, 1 mm from Ca Plastic DIP, SOIC	ase for 10 Seconds or TSSOP Package	260 W	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C SOIC Package: - 7 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GN	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref	C Input Voltage, Output Voltage (Referenced to GND)			
T _A	Operating Temperature, All Package T	Operating Temperature, All Package Types			
t _r , t _f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

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ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC00AN	PDIP-14	2000 Units / Box
MC74HC00ANG	PDIP-14 (Pb-Free)	2000 Units / Box
MC74HC00AD	SOIC-14	55 Units / Rail
MC74HC00ADG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74HC00ADR2	SOIC-14	2500 Units / Reel
MC74HC00ADR2G	SOIC-14 (Pb-Free)	2500 Units / Reel
MC74HC00ADTR2	TSSOP-14*	2500 Units / Reel
MC74HC00AF	SOEIAJ-14	50 Units / Rail
MC74HC00AFG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC74HC00AFEL	SOEIAJ-14	2000 Units / Reel
MC74HC00AFELG	SOEIAJ-14 (Pb-Free)	2000 Units / Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}This package is inherently Pb-Free.

DC CHARACTERISTICS (Voltages Referenced to GND)

	MMM. CON. COM	TW WWW.100Y	CO	Guara	nteed Lin	nit							
Symbol	Parameter	Condition	V _{CC}	-55 to 25°C	≤ 85 °C	≤85°C ≤125°C							
V _{IH}	Minimum High–Level Input Voltage	I _{out} ≤ 20μΑ	nge Il _{out} ≤ 20μA 3.0 4.5	$ I_{\text{out}} \le 20\mu\text{A} $ 3.0 2.10	$ I_{out} \le 20\mu A$ 3.0 2.10 4.5 3.15	$ I_{Out} $ ≤ 20μA $\begin{vmatrix} 3.0 & 2.10 & 2.10 \\ 4.5 & 3.15 & 3.15 \end{vmatrix}$	$\begin{aligned} I_{Out} \leq 20 \mu A & 3.0 & 2.10 & 2.10 & 2.1 \\ 4.5 & 3.15 & 3.15 & 3.1 \end{aligned}$	$ I_{out} \le 20\mu A$ 3.0 2.10 2.10 2 3.15 3.15 3.15	$ I_{out} $ ≤ 20μA $\begin{vmatrix} 3.0 & 2.10 & 2.10 \\ 4.5 & 3.15 & 3.15 \end{vmatrix}$ 3.15 3.15	$ I_{out} \le 20\mu A$ 3.0 2.10 4.5 3.15	2.10 2 3.15 3	10 2.10 15 3.15	V
V _{IL} TV	Maximum Low–Level Input Voltage	$V_{out} = 0.1 V \text{ or } V_{CC} - 0.1 V$ $ I_{out} \le 20 \mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V						
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V						
	M.TW WWW.I	$\begin{split} V_{in} = & V_{IH} \text{ or } V_{IL} & I_{out} \leq 2.4 \text{mA} \\ & I_{out} \leq 4.0 \text{mA} \\ & I_{out} \leq 5.2 \text{mA} \end{split}$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20							
V _{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V						
	COM.TW WY	$\begin{split} V_{in} = V_{IH} \text{ or } V_{IL} & I_{out} \leq 2.4 \text{mA} \\ I_{out} \leq 4.0 \text{mA} \\ I_{out} \leq 5.2 \text{mA} \end{split}$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40							
lin .	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μΑ						
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	6.0	1.0	10	40	μΑ						

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

111.		V _{CC}	Guaranteed Limit			
Symbol	Parameter	V	-55 to 25°C	≤85°C	≤125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C _{in}	Maximum Input Capacitance	1007	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

	MAN, TO COME	Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V	100
C _{PD}	Power Dissipation Capacitance (Per Buffer)*	22	pF

^{*} Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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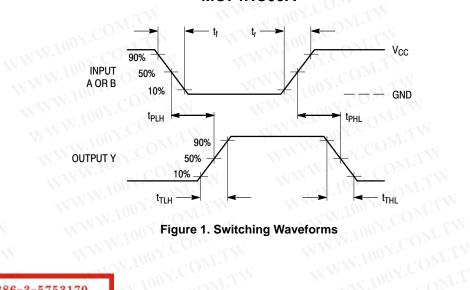
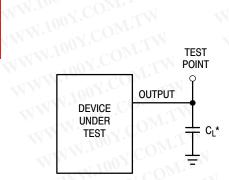


Figure 1. Switching Waveforms WWW.100Y.COM.TW

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*Includes all probe and jig capacitance

Figure 2. Test Circuit WWW.100Y.COM.TW

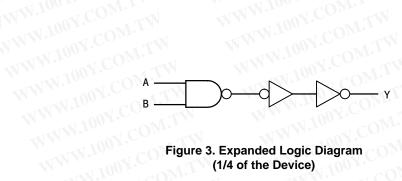


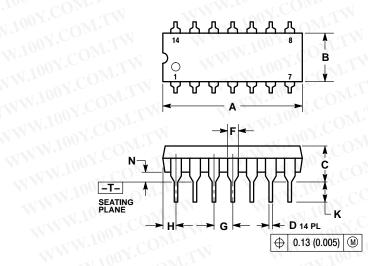
Figure 3. Expanded Logic Diagram
(1/4 of the Device) WWW.100Y.COM.TW WWW.100Y.COM.7 WWW.100Y.COM.TW WWW.100Y.COM.TW

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PACKAGE DIMENSIONS

PDIP-14 **N SUFFIX** CASE 646-06 ISSUE N





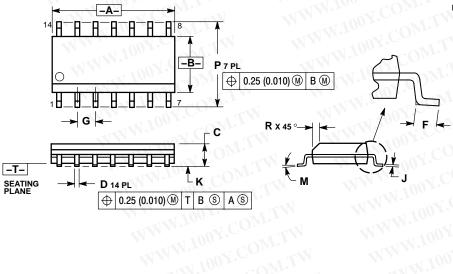
- WW.100Y.COM 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

 - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL. 3.
 - DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 - 5. ROUNDED CORNERS OPTIONAL.

- 4	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.715	0.770	18.16	18.80
В	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
. Ex	0.040	0.070	1.02	1.78
G	0.100	BSC	2.54	BSC
Н	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	To-	10 °	Mre	10 °
N	0.015	0.039	0.38	1.01

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SOIC-14 **D SUFFIX** CASE 751A-03 **ISSUE G**



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NOTES:

- ANTES.

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

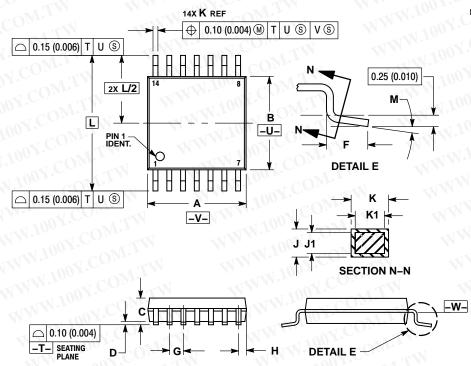
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

. 1		IETERS		HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7°	0 °	7°
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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PACKAGE DIMENSIONS

TSSOP-14 **DT SUFFIX** CASE 948G-01 **ISSUE A**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
 - 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 - NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE
 - DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 - 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

10	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20	7 =	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
.Hc	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
М	0°	8 °	0 °	8°

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