ML4812*

Power Factor Controller

GENERAL DESCRIPTION

The ML4812 is designed to optimally facilitate a peak current control boost type power factor correction system. Special care has been taken in the design of the ML4812 to increase system noise immunity. The circuit includes a precision reference, gain modulator, error amplifier, over-voltage protection, ramp compensation, as well as a high current output. In addition, start-up is simplified by an under-voltage lockout circuit with 6V hysteresis.

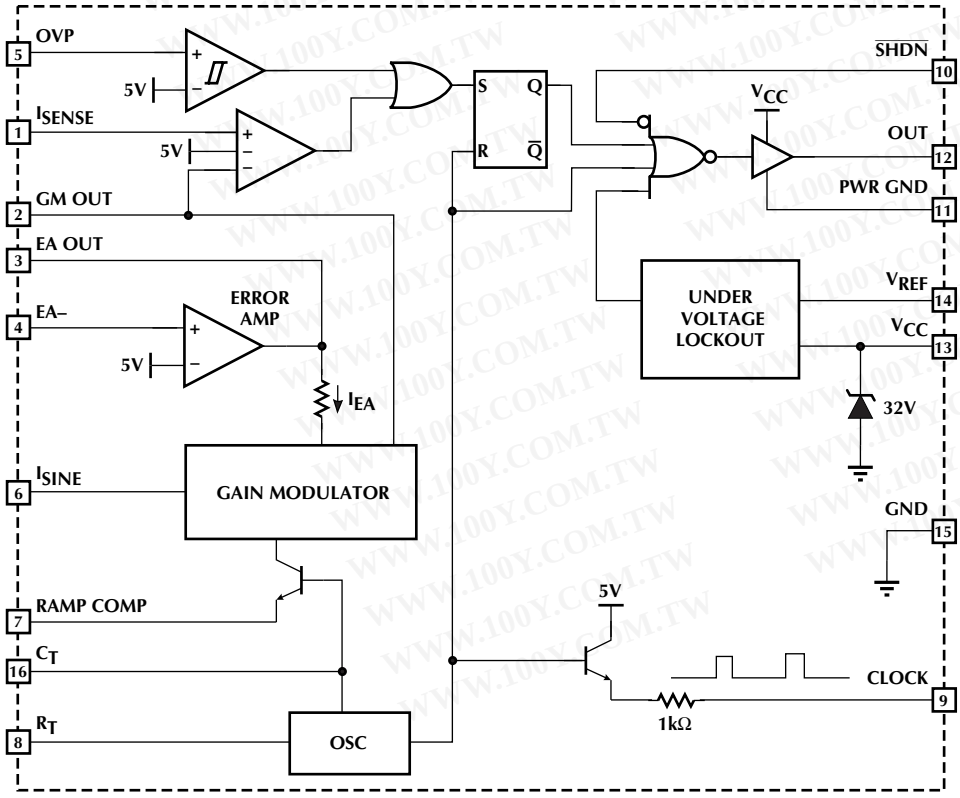
In a typical application, the ML4812 functions as a current mode regulator. The current which is necessary to terminate the cycle is a product of the sinusoidal line voltage times the output of the error amplifier which is regulating the output DC voltage. Ramp compensation is programmable with an external resistor, to provide stable operation when the duty cycle exceeds 50%.

FEATURES

- Precision buffered 5V reference (±0.5%)
- Current-input gain modulator reduces external components and improves noise immunity
- Programmable ramp compensation circuit
- 1A peak current totem-pole output drive
- Overvoltage comparator helps prevent output voltage "runaway"
- Wide common mode range in current sense comparators for better noise immunity
- Large oscillator amplitude for better noise immunity

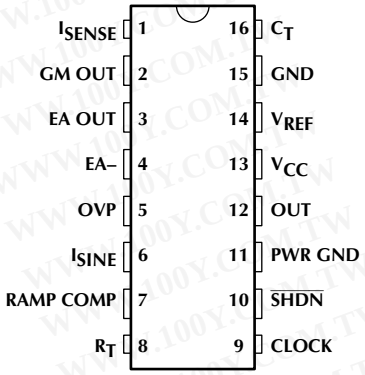
* Some Packages Are End Of Life

BLOCK DIAGRAM (Pin Configuration Shown is for DIP Version)



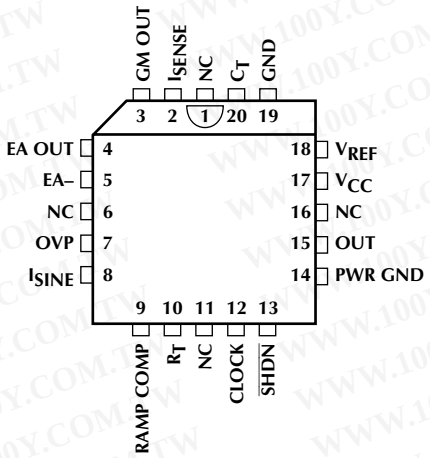
PIN CONFIGURATION

ML4812
16-Pin PDIP (P16)



TOP VIEW

ML4812
20-Pin PLCC (Q20)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	I_{SENSE}	Input from the current sense transformer to the non-inverting input of the PWM comparator.
2	GM OUT	Output of gain modulator. A resistor to ground on this pin converts the current to a voltage. This pin is clamped to 5V and tied to the inverting input of the PWM comparator.
3	EA OUT	Output of error amplifier.
4	EA–	Inverting input to error amplifier.
5	OVP	Input to over voltage comparator.
6	I_{SINE}	Current gain modulator input.
7	RAMP COMP	Buffered output from the oscillator ramp (C_T). A resistor to ground sets the current which is internally subtracted from the product of I_{SINE} and I_{EA} in the gain modulator.
8	R_T	Oscillator timing resistor pin. A 5V source sets a current in the external resistor which is mirrored to charge C_T.
9	CLOCK	Digital clock output.
10	$\overline{SHDN}$	A TTL compatible low level on this pin turns off the output.
11	PWR GND	Return for the high current totem pole output.
12	OUT	High current totem pole output.
13	V_{CC}	Positive Supply for the IC.
14	V_{REF}	Buffered output for the 5V voltage reference.
15	GND	Analog signal ground.
16	C_T	Timing capacitor for the oscillator.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 30mA
Output Current Source or Sink (OUT) DC 1.0A
Output Energy (capacitive load per cycle) 5µJ
Gain Modulator I_{SINE} Input (I_{SINE}) 1.2mA
Error Amp Sink Current (EA OUT) 10mA
Oscillator Charge Current 2mA
Analog Inputs (I_{SENSE}, EA–, OVP) ..... –0.3V to 5.5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (soldering 10 sec.) ..... 260°C
Thermal Resistance (θ_{JA})
20-Pin PLCC ..... 60°C/W
16-Pin PDIP ..... 65°C/W

OPERATING CONDITIONS

Temperature Range
ML4812CX ..... 0°C to 70°C
ML4812IX ..... –40°C to 85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 15V , R_T = 14kΩ, C_T = 1000pF, T_A = Operating Temperature Range (Notes 1, 2).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Initial Accuracy	T_J = 25°C	91	98	105	kHz
Voltage Stability	12V < V_{CC} < 18V		0.3		%
Temperature Stability			2		%
Total Variation	Line, temperature	90		108	kHz
Ramp Valley to Peak			3.3		V
R_T Voltage		4.8	5.0	5.2	V
Discharge Current (R_T open)	T_J = 25°C, V_{CT}= 2V	7.8	8.4	9.0	mA
	V_{CT} = 2V	7.3	8.4	9.3	mA
Clock Out Voltage Low	R_L = 16kΩ		0.2	0.5	V
Clock Out Voltage High	R_L = 16kΩ	3.0	3.5		V
REFERENCE					
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		2	20	mV
Load Regulation	1mA < I_O < 20mA		2	20	mV
Temperature Stability			0.4		%
Total Variation	Line, load, temp.	4.9		5.1	V
Output Noise Voltage	10Hz to 10kHz		50		µV
Long Term Stability	T_J = 125°C, 1000 hours		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
ERROR AMPLIFIER					
Input Offset Voltage				±15	mV
Input Bias Current			–0.1	–1.0	µA
Open Loop Gain	1 < $V_{EA\ OUT}$ < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	75		dB
Output Sink Current	$V_{EA\ OUT}$ = 1.1V, V_{EA-} = 6.2V	2	12		mA
Output Source Current	$V_{EA\ OUT}$ = 5.0V, V_{EA-} = 4.8V	–0.5	–1.0		mA
Output High Voltage	$I_{EA\ OUT}$ = –0.5mA, V_{EA-} = 4.8V	5.3	5.5		V
Output Low Voltage	$I_{EA\ OUT}$ = 1mA, V_{EA-} = 6.2V		0.5	1.0	V
Unity Gain Bandwidth			1.0		MHz

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN MODULATOR					
I_{SINE} Input Voltage	I_{SINE} = 500µA	0.4	0.7	0.9	V
Output Current (GM OUT)	I_{SINE} = 500µA, EA– = V_{REF} –20mV	430	470	510	µA
	I_{SINE} = 500µA, EA– = V_{REF} + 20mV		3	10	µA
	I_{SINE} = 1mA, EA– = V_{REF} – 20mV	860	940	1020	µA
	I_{SINE} = 500µA, EA– = V_{REF} – 20mV, $I_{RAMP\ COMP}$ = 50µA		455		µA
Bandwidth			200		kHz
PSRR	12V < V_{CC} < 25V		70		dB
OVP COMPARATOR					
Input Offset Voltage	Output Off	–25		+5	mV
Hysteresis	Output On	95	105	115	mV
Input Bias Current			–0.3	–3	µA
Propagation Delay			150		ns
PWM COMPARATOR: I_{SENSE}					
Input Offset Voltage				±15	mV
Input Offset Current				±1	µA
Input Common Mode Range		–0.2		5.5	V
Input Bias Current			–2	–10	µA
Propagation Delay			150		ns
I_{LIMIT} Trip Point	$V_{GM\ OUT}$ = 5.5V	4.8	5	5.2	V
OUTPUT					
Output Voltage Low	I_{OUT} = –20mA		0.1	0.4	V
	I_{OUT} = –200mA		1.6	2.2	V
Output Voltage High	I_{OUT} = 20mA	13	13.5		V
	I_{OUT} = 200mA	12	13.4		V
Output Voltage Low in UVLO	I_{OUT} = –5mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		ns
Shutdown	V_{IH}	2.0			V
	V_{IL}			0.8	V
	I_{IL}, $V_{\overline{SHDN}}$ = 0V			–1.5	mA
	I_{IH}, $V_{\overline{SHDN}}$ = 5V			10	µA
UNDER-VOLTAGE LOCKOUT					
Startup Threshold		15	16	17	V
Shutdown Threshold		9	10	11	V
V_{REF} Good Threshold			4.4		V
SUPPLY					
Supply Current	Start-Up, V_{CC} = 14V, T_J = 25°C		0.8	1.2	mA
	Operating, T_J = 25°C		20	25	mA
Internal Shunt Zener Voltage	I_{CC} = 30mA	25	30	34	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: V_{CC} is raised above the Startup Threshold first to activate the IC, then returned to 15V.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4812 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where:

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}}$$

and:

$$T_{DEADTIME} = \frac{C_T \times V_{RAMP\ VALLEY\ TO\ PEAK}}{8.4mA - I_{SET}}$$

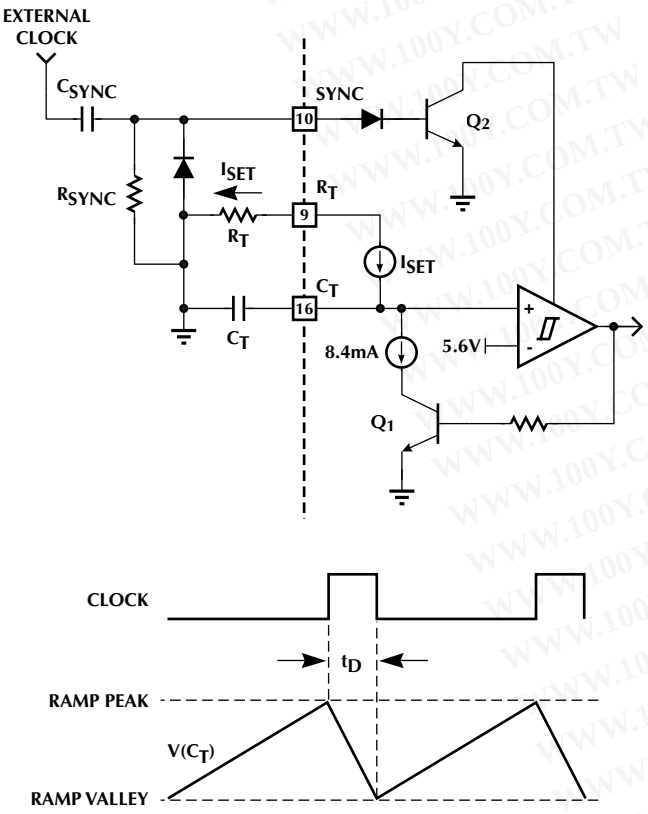


Figure 1. Oscillator Block Diagram

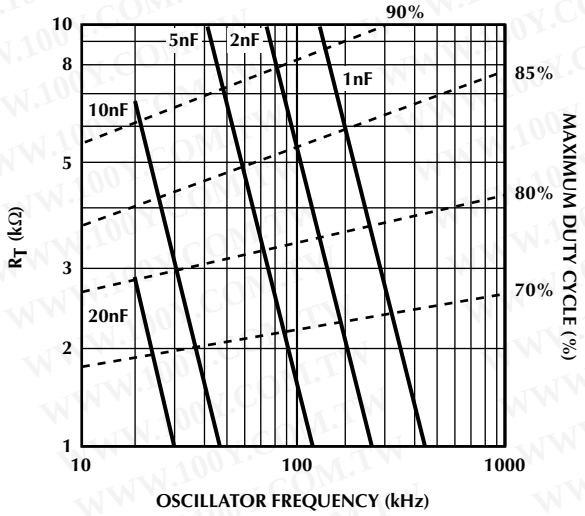


Figure 2. Oscillator Timing Resistance vs. Frequency

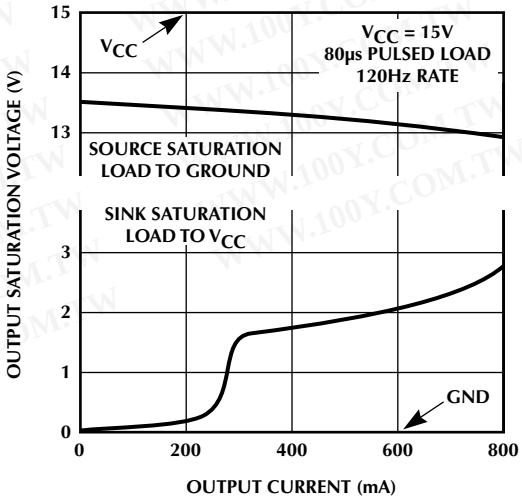


Figure 3. Output Saturation Voltage vs. Output Current

FUNCTIONAL DESCRIPTION (Continued)

OUTPUT DRIVER STAGE

The ML4812 output driver is a 1A peak output high speed totem pole circuit designed to quickly drive capacitive loads, such as power MOSFET gates. (Figure 3)

ERROR AMPLIFIER

The ML4812 error amplifier is a high open loop gain, wide bandwidth, amplifier.(Figures 4-5)

GAIN MODULATOR

The ML4812 gain modulator is of the current-input type to provide high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator. The output of the gain modulator is a current of the form: I_{OUT} is proportional to $I_{SINE} \times I_{EA}$, where I_{SINE} is the current in the dropping resistor, and I_{EA} is a current proportional to the output of the error amplifier. When the error amplifier is saturated high, the output of the gain modulator is approximately equal to the I_{SINE} input current. The gain modulator output current is converted into the reference voltage for the PWM comparator through a resistor to ground on the gain modulator output. The gain modulator output is clamped to 5V to provide current limiting.

Ramp compensation is accomplished by subtracting 1/2 of the current flowing out of RAMP COMP through a buffer transistor driven by C_T which is set by an external resistor.

UNDER VOLTAGE LOCKOUT

On power-up the ML4812 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is imposed. During the UVLO condition, the 5V V_{REF} pin is "off", making it usable as a "flag" for starting up a downstream PWM converter.

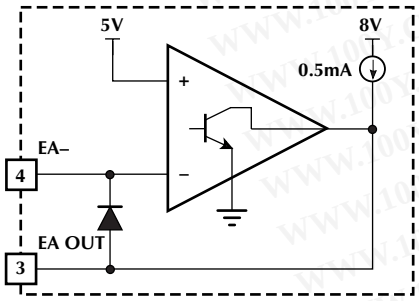


Figure 4. Error Amplifier Configuration

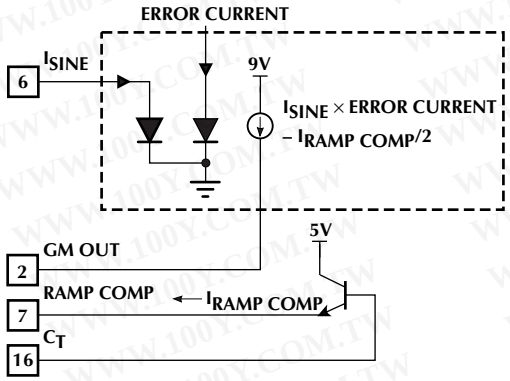


Figure 6. Gain Modulator Block Diagram

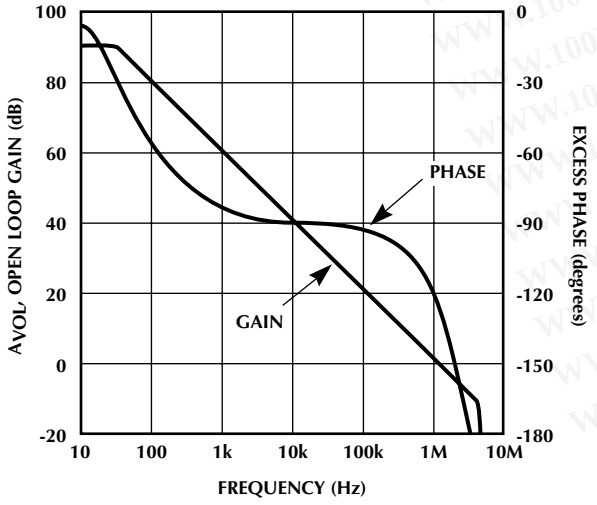


Figure 5. Error Amplifier Open-Loop Gain and Phase vs Frequency

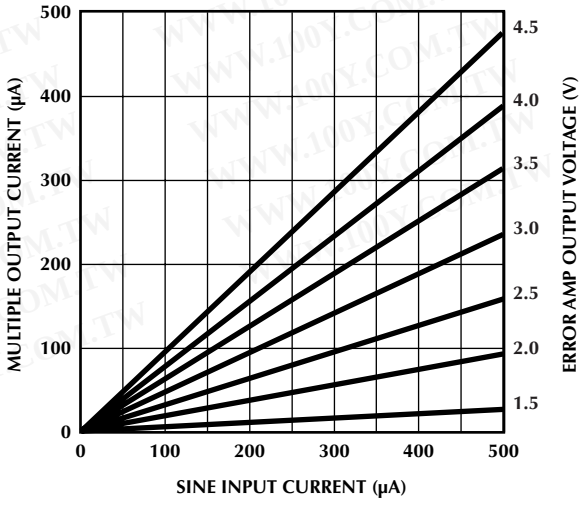


Figure 7. Gain Modulator Linearity

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4812CP	0°C to 70°C	Molded PDIP (P16)
ML4812CQ	0°C to 70°C	Molded PLCC (Q20) (End Of Life)
ML4812IP	–40°C to 85°C	Molded PDIP (P16) (End Of Life)
ML4812IQ	–40°C to 85°C	Molded PLCC (Q20) (End Of Life)

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