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September 1983 Revised February 1999

MM74HC165 Parallel-in/Serial-out 8-Bit Shift Register

General Description

The MM74HC165 high speed PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This 8-bit serial shift register shifts data from ${\bf Q}_{\bf A}$ to ${\bf Q}_{\bf H}$ when clocked. Parallel inputs to each stage are enabled by a low level at the SHIFT/LOAD input. Also included is a gated CLOCK input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a CLOCK INHIBIT function. Holding either of the CLOCK inputs high inhibits clocking, and holding either CLOCK input low with the SHIFT/LOAD input high enables the other CLOCK input. Data transfer occurs on the positive going edge of the clock. Parallel

loading is inhibited as long as the SHIFT/LOAD input is HIGH. When taken LOW, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 µA maximum
- Low quiescent supply current: 80 µA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

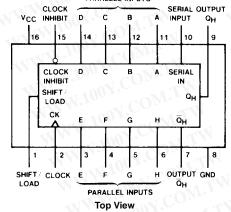
Ordering Code:

Order Number	Package Number	Package Description
MM74HC165M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC165SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC165MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC165	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP PARALLEL INPUTS



Function Table

10-		Inte	rnal	Output			
Shift/	Clock	Clock	Serial	Parallel	Output		Q _H
Load Inhibit		117	АН	Q_A	QB	N.	
NEW	Х	X	Χ	ah	а	b	h
H	100	L	X	X	Q_{A0}	Q_{B0}	Q _{H0}
Н	L	1	Н	X	Н	Q_{AN}	Q_{GN}
H	L	1	L	X	L	Q_AN	
Н	H 4	X	X	X	Q_{A0}	Q_{B0}	Q _{H0}

H = HIGH Level (steady state), L = LOW Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from LOW-to-HIGH level

 Q_{A0} , Q_{B0} , Q_{H0} = The level of Q_A , Q_B , or Q_H , respectively, before the indicated steady-state input conditions were established.

 Q_{AN} , Q_{GN} = The level of Q_A or Q_G before the most recent \uparrow transition of the clock; indicates a one-bit shift.

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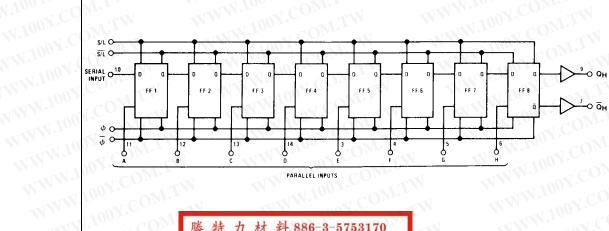
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Absolute Maximum Rati	ngs(Note 1)
(Note 2)	
Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input Voltage (V _{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V _{OUT})	-0.5 to V_{CC} +0.5V
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V _{CC} or GND Current, per pin (I _{CC})	±50 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T _L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V _{CC}	V
Operating Temperature Range (T	₄) –40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns
Note 1: Absolute Maximum Patings are th	oce values	heyond whi	ich dom

age to the device may occur. Note 2: Unless otherwise specified all voltages are referenced to ground.

 $\textbf{Note 3:} \ \ \textbf{Power Dissipation temperature derating} - \ \ \textbf{plastic "N" package:}$ 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Conditions V _{CC}	T _A =	25°C	$T_A = -40 \text{ to } 85^{\circ}\text{C}$	T _A = -55 to 125°C	Units
Symbol	Parameter	Conditions	Тур		Guaranteed L	imits	Ullits	
V _{IH}	Minimum HIGH Level	1/1/1	2.0V	17	1.5	1.5	1.5	V
	Input Voltage	W.IO.	4.5V		3.15	3.15	3.15	V
ONY.	WITT	11 11 100	6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level	-11/1/1/1	2.0V	Oba	0.5	0.5	0.5	V
	Input Voltage	W 10	4.5V		1.35	1.35	1.35	V
	COM	WWW.	6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}	00	CON	L. F.		TAIN . IO	. 7
	Output Voltage	$ I_{OUT} \le 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
	COM	W	4.5V	4.5	4.4	4.4	4.4	V
	OY.CO TW	M. M.	6.0V	6.0	5.9	5.9	5.9	V
	COM	$V_{IN} = V_{IH}$ or V_{IL}	1.7	- ×7 C) IA P.	×XI	-X W W.	- 03
	001.0 -11 IV	$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
	COM	I _{OUT} ≤ 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}	- t ()	00 -			TIV.	To.
	Output Voltage	I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	0.1	V
	1.100 . COM.	7	4.5V	0	0.1	0.1	0.1	V
WW	W.Co.	W W	6.0V	0	0.1	0.1	0.1	V
	M.Ing. CON	$V_{IN} = V_{IH}$ or V_{IL}		1.10	57 C) Name	VIV	MA
	1007.0	$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
-11	MM. IO	$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input	$V_{IN} = V_{CC}$ or GND	6.0V	-xxi 11	±0.1	±1.0	±1.0	μΑ
- 1	Current	V _{CC} = 2-6V		144.	anv.	UU.	17	M
I _{CC}	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	6.0V	TIN.	8.0	80	160	μΑ
4	Supply Current	$I_{OUT} = 0 \mu A$	1		4005	T		M.A.
	1 100 E	$V_{CC} = 2-6V$			Too	COMP	-4	

Note 4: For a power supply of 5V ±10% the worst case output voltages (VOH, and VOL) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage curvature of the V_{IH} value at 5.5V is 3.85V.) rent (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used. WWW.100Y.COM

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AC Electrical Characteristics

 $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 15$ pF, $t_r = t_{\ell} = 6$ ns

Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
f _{MAX}	Maximum Operating Frequency	T.V.	50	30	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay H to Q _H or \overline{Q}_H	MM	15	25	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q _H	MMA	13	25	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Clock to Output	N WW	15	25	ns
ts	Minimum Setup Time Serial Input to Clock, Parallel or Data to Shift/Load	M MN	10	20	ns
t _S	Minimum Setup Time Shift/Load to Clock	W W	11	20	ns
t _S	Minimum Setup Time Clock Inhibit to Clock		10	20	ns
t _H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load	T.TW	MMM.T	0	ns
t _W	Minimum Pulse Width Clock	N	TIM W.	16	ns

AC Electrical Characteristics

tpHL tpLH Maxim Delay t ts Minimu Serial t or Para ts Minimu Shift/Lo	Parameter um Operating um Operating um Propagation H to Q _H or Q H um Propagation Serial Shift/ I Load to Q _H um Propagation Clock to Output um Setup Time Input to Clock, allel Data to Shift/Load um Setup Time poad to Clock	Conditions	2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V	Typ 10 45 50 70 21 18 70 21 18 70 21 18 35 11 9	5 27 32 150 30 26 175 35 30 150 30 26	Guaranteed L 4 21 25 189 38 33 220 44 37 189 38 33 125 25	4 18 21 225 45 39 260 52 44 225 45 39	MHz MHz MHz ns ns ns ns ns ns ns
Frequence Freque	um Propagation H to Q _H or Q̄ _H um Propagation Serial Shift/ I Load to Q _H um Propagation Clock to Output um Setup Time Input to Clock, allel Data to Shift/Load um Setup Time	MMM.1007. MMM.1007. MMM.1007. MMM.1007.	4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V	45 50 70 21 18 70 21 18 70 21 18 35 11	27 32 150 30 26 175 35 30 150 30 26	21 25 189 38 33 220 44 37 189 38 33	18 21 225 45 39 260 52 44 225 45 39	MHz MHz ns ns ns ns ns ns ns
tpHL, tpLH Maxim Delay I tpHL, tpLH Maxim Delay I tpHL, tpLH Maxim Delay I ts Minimu Serial I or Para ts Minimu Shift/Lot	um Propagation H to Q _H or Q H um Propagation Serial Shift/ Il Load to Q _H um Propagation Clock to Output um Setup Time Input to Clock, allel Data to Shift/Load um Setup Time	WWW.100Y WWW.100 WWW.100 WWW.100 WWW.100 WWW.100 WWW.100 WWW.100 WWW.100 WWW.100 WWW.100 WWW.100	6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V	50 70 21 18 70 21 18 70 21 18 70 21 18 35 11	32 150 30 26 175 35 30 150 30 26	25 189 38 33 220 44 37 189 38 33 125	21 225 45 39 260 52 44 225 45 39	ns
Delay I IphL, IphH Maxim Delay I Paralle IphL, IphH Maxim Delay I Is Minimu Serial I or Para Is Minimu Shift/Lo	H to Q _H or Q _H um Propagation Serial Shift/ I Load to Q _H um Propagation Clock to Output um Setup Time Input to Clock, allel Data to Shift/Load um Setup Time	WWW.1003 WWW.100 WWW.100 WWW.100	2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V	70 21 18 70 21 18 70 21 18 35 11	150 30 26 175 35 30 150 30 26	189 38 33 220 44 37 189 38 33 125	225 45 39 260 52 44 225 45 39	ns ns ns ns ns ns ns
Delay I tphL, tpLH Maxim Delay S Paralle tphL, tpLH Maxim Delay S ts Minimu Serial I or Para ts Minimu Shift/Lo	H to Q _H or Q _H um Propagation Serial Shift/ I Load to Q _H um Propagation Clock to Output um Setup Time Input to Clock, allel Data to Shift/Load um Setup Time	WWW.TOO. WWW.TO WWW.TO	4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V	21 18 70 21 18 70 21 18 35 11	30 26 175 35 30 150 30 26	38 33 220 44 37 189 38 33	45 39 260 52 44 225 45 39	ns ns ns ns ns ns
tpHL, tpLH Maxim Delay sparalle tpHL, tpLH Maxim Delay start series or Para start shift series Minimu Shift/Lot ts Minimu Shift/Lot ts Minimu Shift/Lot ts Minimu	um Propagation Serial Shift/ Il Load to Q _H um Propagation Clock to Output um Setup Time Input to Clock, allel Data to Shift/Load um Setup Time	WWW.100 WWW.10 WWW.10 WWW.10	6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V	18 70 21 18 70 21 18 35 11	26 175 35 30 150 30 26 100	33 220 44 37 189 38 33 125	39 260 52 44 225 45 39	ns ns ns ns ns
tpHL, tpLH Maxim Delay sparalle tpHL, tpLH Maxim Delay start series or Para ts Minimu Shift/Lot ts Minimu Shift/Lot ts Minimu Shift/Lot ts Minimu	um Propagation Serial Shift/ Il Load to Q _H um Propagation Clock to Output um Setup Time Input to Clock, allel Data to Shift/Load um Setup Time	WWW.IO	2.0V 4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V	70 21 18 70 21 18 35 11	175 35 30 150 30 26 100	220 44 37 189 38 33 125	260 52 44 225 45 39 150	ns ns ns ns ns
Delay to Paralle tent, tent Delay to Paralle tent, tent Delay to Paralle tent Delay tent Delay to Paralle tent Delay tent	Serial Shift/ Isl Load to Q _H um Propagation Clock to Output um Setup Time Input to Clock, allel Data to Shift/Load um Setup Time	WWW.I	4.5V 6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V	21 18 70 21 18 35 11	35 30 150 30 26	44 37 189 38 33 125	52 44 225 45 39 150	ns ns ns ns ns
Paralle tphL, tpLH Maxim Delay t ts Minimu Serial I or Para ts Minimu Shift/Lo ts Minimu	In Load to Q _H um Propagation Clock to Output um Setup Time Input to Clock, allel Data to Shift/Load um Setup Time	WWW.I	6.0V 2.0V 4.5V 6.0V 2.0V 4.5V 6.0V	18 70 21 18 35 11	30 150 30 26 100	37 189 38 33 125	44 225 45 39 150	ns ns ns ns
ts Minimu Shift/Lot ts Minimu Serial I or Para ts Minimu Shift/Lot ts Minimu Shift/Lot	um Propagation Clock to Output Im Setup Time Input to Clock, allel Data to Shift/Load Im Setup Time	MAM. MAM.	2.0V 4.5V 6.0V 2.0V 4.5V 6.0V	70 21 18 35 11	150 30 26 100	189 38 33 125	225 45 39 150	ns ns ns
Delay (ts Minimu Serial I or Para ts Minimu Shift/Lo	clock to Output Im Setup Time Input to Clock, allel Data to Shift/Load Im Setup Time	MM. MMM.	4.5V 6.0V 2.0V 4.5V 6.0V	21 18 35 11	30 26 100	38 33 125	45 39 150	ns ns
Delay 6 ts Minimu Serial I or Para ts Minimu Shift/L6 ts Minimu	im Setup Time Input to Clock, allel Data to Shift/Load im Setup Time	MM. MMM.	6.0V 2.0V 4.5V 6.0V	18 35 11	26 100	33 125	39 150	ns
Serial I or Para ts Minimu Shift/Lo	Input to Clock, allel Data to Shift/Load um Setup Time	MM. MM.	2.0V 4.5V 6.0V	35 11	100	125	150	
Serial I or Para ts Minimu Shift/Lo	Input to Clock, allel Data to Shift/Load um Setup Time	MM. MM.	4.5V 6.0V	11	- 1	W .	-11	ne
or Para ts Minimu Shift/Lo ts Minimu	um Setup Time	WW	6.0V		20	25		113
ts Minimu Shift/Lo	ım Setup Time	WN	- 4				30	ns
Shift/Lo	_7 1 10 -	WY	2.0V	3	17	21	25	ns
Shift/Lo	oad to Clock			38	100	125	150	ns
	COM		4.5V	12	20	25	30	ns
			6.0V	9	17	21	25	ns
	ım Setup Time	N 1N	2.0V	35	100	125	150	ns
Clock I	nhibit to Clock		4.5V	11	20	25	30	ns
111	00^{10} $M.$		6.0V	9	17	21	25	ns
t _H Minimu	ım Hold Time Serial		2.0V	. 0	0	0	0	ns
Input to	Clock or		4.5V		0	0	0	ns
Paralle	l Data to Shift/Load		6.0V		0	0	0	ns
t _W Minimu	ım Pulse Width,	1	2.0V	30	80	100	120	ns
Clock	1007.0		4.5V	9	16	20	24	ns
-71	M.100		6.0V	8	14	18	20	ns
t _{THL} , t _{TLH} Maxim	um Output	11.77	2.0V	30	75	95	110	ns
Rise ar	nd Fall Time		4.5V	9	15	19	22	ns
N	100 1.		6.0V	8	13	16	19	ns
t _r , t _f Maxim	um Input Rise and	TIN	2.0V	AN W	1000	1000	1000	ns
Fall Tin	- 41111		4.5V		500	500	500	ns
4	WWW LOOK		6.0V		400	400	400	ns
	TIMM:	COM	I	11	WW	· CO	W.	

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AC E	lectrical Charact	eristics (Contin	nued)					
Symbol	Parameter	Conditions	V _{CC}	$T_A = 25^{\circ}C$ $T_A = -40 \text{ to } 85^{\circ}C$ $T_A = -55 \text{ to } 1$		T _A = -55 to 125°C	Units	
		Conditions	•cc	Тур		Guaranteed L	imits	Ullits
C _{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100	MM	1001.CO	MITW	pF
C _{IN}	Maximum Input Capacitance	ST CONT		5	10	10	10	pF

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Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, WWW.100Y.COM.TW WWW.100Y. $I_S = C_{PD} \ V_{CC} \ f + I_{CC}.$

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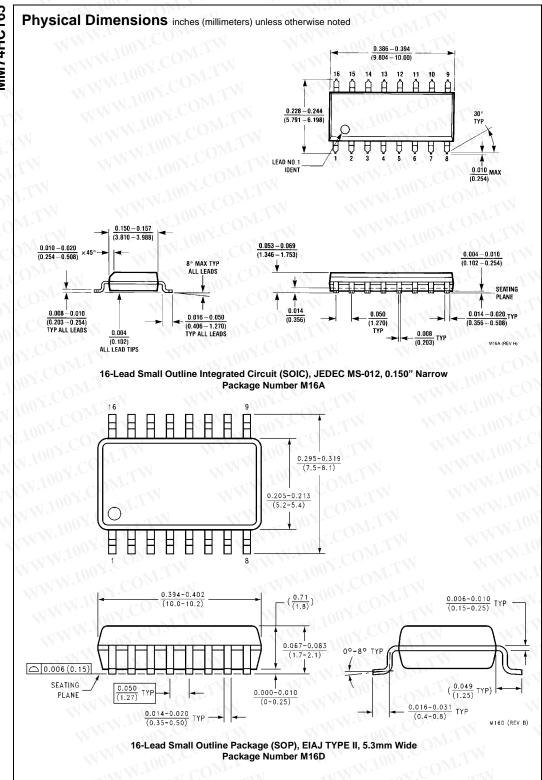
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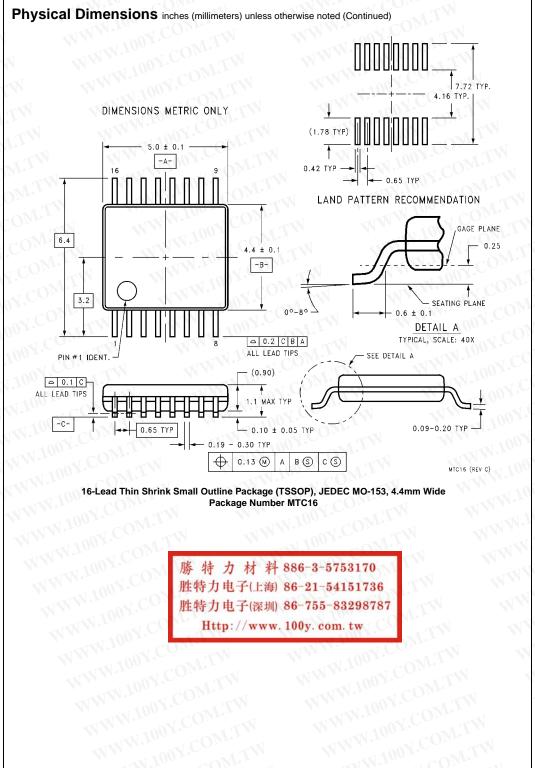
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Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.090 (18.80 - 19.81)(2.286)**16 15 14 13 12 11 10 9** 16 15 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 8 1 2 IDENT OPTION 01 OPTION 02 0.065 0.130 ± 0.005 4° TYP 0.060 (1.524) TYP (1.651)0.300 - 0.320(3.302 ± 0.127) OPTIONAL (7.620 - 8.128)0.145 - 0.200(3.683 - 5.080)95°±5° $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 90° ± 4° TYP MIN $\frac{0.280}{(7.112)}$ (0.508)0.125 - 0.150 (3.175 - 3.810) 0.030 ± 0.015 MIN (0.762 ± 0.381) 0.014 = 0.023 (0.356 = 0.584) 0.100 ± 0.010 (0.325 +0.040 -0.015 (2.540 ± 0.254) 0.050 ± 0.010 N16E (REV F) TYP (8.255 +1.016) -0.381 (1.270 ± 0.254)

16-Lead Plastic Dual-In-Line Package (PDIP), MS-001, 0.300" Wide Package N16E

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