勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

19-1788; Rev 0; 10/00

EVALUATION KIT AVAILABLE

MAXIM

Triple Charge-Pump TFT LCD DC-DC Converter

MAX1747

General Description

The MAX1747 triple charge-pump DC-DC converter provides the regulated voltages required by active matrix thin-film transistor (TFT) liquid-crystal displays (LCDs) in a low-profile TSSOP package. One high-power and two low-power charge pumps convert the +2.7V to +4.5V input supply voltage into three independent output voltages.

The primary high-power charge pump generates an output voltage (V_{OUT}) between 4.5V and 5.5V that is regulated within ±1%. The low-power BiCMOS control circuitry and the low on-resistance (R_{ON}) power MOSFETs maximize efficiency. The adjustable switching frequency (200kHz to 2MHz) provides fast transient response and allows the use of small low-profile ceramic capacitors.

The dual low-power charge pumps independently regulate one positive output (V_{POS}) and one negative output (V_{NEG}). These additional outputs use external diode and capacitor multiplier stages (as many stages as required) to regulate output voltages up to +35V and -35V.

The constant switching frequency and a proprietary regulation algorithm minimize output ripple and capacitor sizes for all three charge pumps. The MAX1747 is available in the ultra-thin TSSOP package (1.1mm max height).

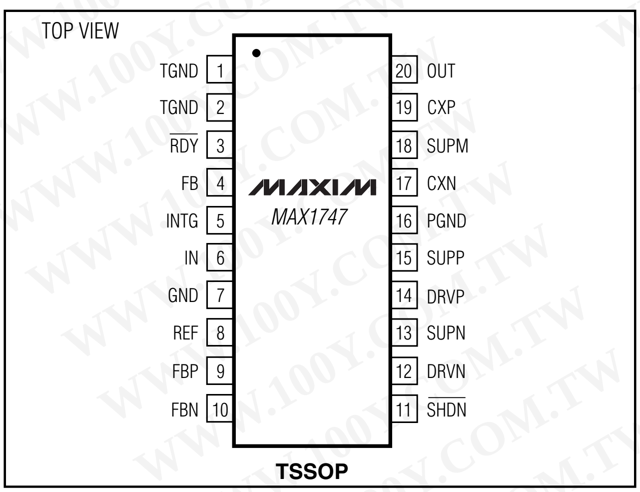
Applications

TFT Active-Matrix LCDs

Passive-Matrix Displays

Personal Digital Assistants (PDAs)

Pin Configuration



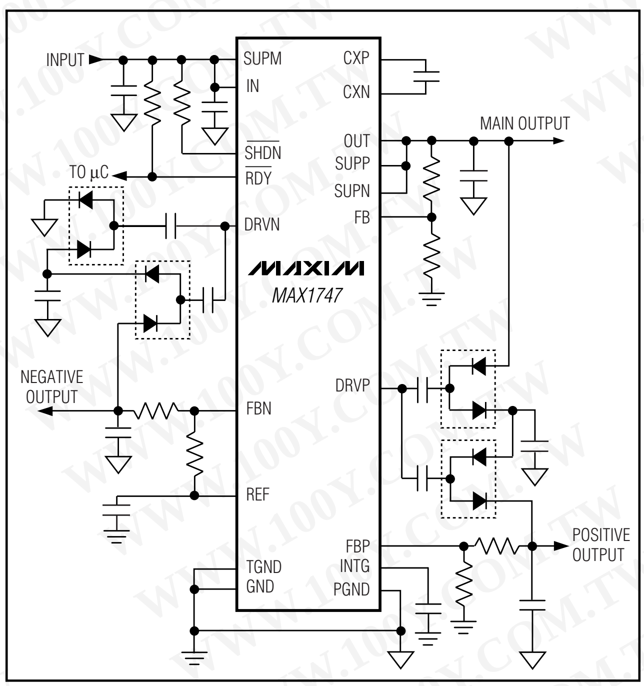
Features

- ♦ Adjustable Outputs
  - Up to +5.5V Main High-Power Output
  - Up to +35V Positive Charge-Pump Output
  - Down to -35V Negative Charge-Pump Output
- ♦ 200kHz to 2MHz Adjustable Switching Frequency
- ♦ +2.7V to +4.5V Input Supply
- ♦ Internal Power MOSFETs
- ♦ 0.1µA Shutdown Current
- ♦ Internal Soft-Start
- ♦ Power-Ready Output
- ♦ Internal Supply Sequencing
- ♦ Fast Transient Response
- ♦ Ultra-Thin Solution (No Inductors)
- ♦ Thin TSSOP Package (1.1mm max)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1747EUP	-40°C to +85°C	20 TSSOP

Typical Operating Circuit



For price, delivery, and to place orders, please contact Maxim Distribution at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Triple Charge-Pump TFT LCD DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

IN, SUPM, OUT, TGND to GND .... -0.3V to +6V
$\overline{SHDN}$ .... -0.3V to +1V
PGND to GND .... ±0.3V
SUPM to IN .... ±0.3V
CXN to PGND .... -0.3V to (V_{SUPM} + 0.3V)
CXP to PGND .... (V_{SUPM} - 0.3V) to (V_{OUT} + 0.3V)
DRVN to GND .... -0.3V to (V_{SUPN} + 0.3V)
DRVP to GND .... -0.3V to (V_{SUPP} + 0.3V)
$\overline{RDY}$ to GND .... -0.3V to +14V
SUPP, SUPN to GND .... -0.3V to +14V
INTG, REF, FB, FBN, FBP to GND .... -0.3V to (V_{IN} + 0.3V)

Continuous Current into:
SUPM, CXN, CXP, OUT .... ±800mA
SUPP, SUPN, DRVN, DRVP .... ±200mA
$\overline{SHDN}$ .... +100µA
All Other Pins .... ±10mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 10.9mW/°C above +70°C) 879mW
Operating Temperature Range .... -40°C to +85°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{SUPM} = +3.0V, V_{SUPP} = V_{SUPN} = +5V, TGND = PGND = GND, $I_{\overline{SHDN}}$ = 22µA, C_{OUT} = 2 × 4.7µF, C_{REF} = 0.22µF, C_{INTG} = 1500pF, V_{OUT} = +5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V_{IN}		2.7		4.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} falling, 40mV hysteresis (typ)	2.2	2.4	2.6	V
Input Quiescent Supply Current	I_{IN} + I_{SUPM}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V, V_{OUT} = 5V, no load on DRVN and DRVP; CXN and CXP open		0.9	1.0	mA
Output Quiescent Supply Current	$I_{Q(OUT)}$	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V, V_{OUT} = 5V, no load on DRVN and DRVP; CXN and CXP open		2.5	4.0	mA
Shutdown Supply Current		$V_{\overline{SHDN}}$ = 0, V_{SUPM} = 5V		0.1	20	µA
Operating Frequency	f_{OSC}	$I_{\overline{SHDN}}$ = 22µA	0.65	1	1.2	MHz
MAIN CHARGE PUMP						
Output Voltage Range	V_{OUT}		4.5		5.5	V
Maximum Output Current	$I_{OUT(MAX)}$	C_X = 0.47µF	200			mA
FB Regulation Voltage	V_{FB}		1.237	1.248	1.263	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V	-50		+50	nA
Integrator Transconductance				530		µS
FB Power-Ready Trip Level		Rising edge	1.09	1.125	1.16	V
FB Fault Trip Level		Falling edge		1.100		V
Main Soft-Start Period				4.096 / F_{OSC}		s
NEGATIVE LOW-POWER CHARGE PUMP						
SUPN Input Supply Range	V_{SUPN}		2.7		13	V
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.2V, no load on DRVN		0.6	0.8	mA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = 13V		0.1	10	µA
FBN Regulation Voltage	V_{FBN}		-50	0	+50	mV

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{SUPM} = +3.0V, V_{SUPP} = V_{SUPN} = +5V, TGND = PGND = GND, $I_{\overline{SHDN}}$ = 22µA, C_{OUT} = 2 × 4.7µF, C_{REF} = 0.22µF, C_{INTG} = 1500pF, V_{OUT} = +5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FBN Input Bias Current	I_{FBN}	V_{FBN} = -50mV	-50		+50	nA
DRVN PCH On-Resistance				3	6	Ω
DRVN NCH On-Resistance		V_{FBN} = 50mV		1	5	Ω
		V_{FBN} = -50mV	20			kΩ
FBN Power-Ready Trip Level		Falling edge	80	125	165	mV
FBN Fault Trip Level		Rising edge		140		mV
Negative Soft-Start Period				2.048/ F_{OSC}		s
POSITIVE LOW-POWER CHARGE PUMP						
SUPP Input Supply Range	V_{SUPP}		2.7		13	V
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V, no load on DRVP		0.6	0.8	mA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = 13V		0.1	10	µA
FBP Regulation Voltage	V_{FBP}		1.20	1.25	1.30	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.5V	-50		+50	nA
DRVP PCH On-Resistance				3	6	Ω
DRVP NCH On-Resistance		V_{FBP} = 1.20V		1.5	5	Ω
		V_{FBP} = 1.30V		20		kΩ
FBP Power-Ready Trip Level		Rising edge	1.090	1.125	1.160	V
FBP Fault Trip Level		Falling edge		1.100		V
Positive Soft-Start Period				2.048/ F_{OSC}		s
REFERENCE						
Reference Voltage	V_{REF}	-2µA < I_{REF} < 50µA	1.231	1.25	1.269	V
Reference Undervoltage Threshold		V_{REF} rising	0.95	1.05	1.18	V
LOGIC SIGNALS						
$\overline{SHDN}$ Input Low Voltage					0.4	V
$\overline{SHDN}$ Bias Voltage		$I_{\overline{SHDN}}$ = 22µA	580	724	830	mV
$\overline{SHDN}$ Bias Voltage Tempco				2		mV/°C
$\overline{SHDN}$ Input Current Range	$I_{\overline{SHDN}}$	For 200kHz to 2MHz operation	3		65	µA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA		0.25	0.5	V
$\overline{RDY}$ Output High Leakage		$V_{\overline{RDY}}$ = 13V		0.01	1	µA

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Triple Charge-Pump TFT LCD DC-DC Converter

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{SUPM} = +3.0V, V_{SUPP} = V_{SUPN} = +5V, TGND = PGND = GND, $I_{\overline{SHDN}}$ = 22µA, C_{OUT} = 2 × 4.7µF, C_{REF} = 0.22µF, C_{INTG} = 1500pF, V_{OUT} = +5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Supply Range	V_{IN}		2.7	4.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} falling, 40mV hysteresis (typ)	2.2	2.6	V
Input Quiescent Supply Current	I_{IN} + I_{SUPM}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V, V_{OUT} = 5V, no load on DRVN and DRVP; CXN and CXP open		1.0	mA
Output Quiescent Supply Current	$I_{Q(OUT)}$	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V, V_{OUT} = 5V, no load on DRVN and DRVP; CXN and CXP open		4.0	mA
Input Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPM} = 5V		20	µA
Operating Frequency	f_{OSC}	$I_{\overline{SHDN}}$ = 22µA	0.65	1.2	MHz
MAIN CHARGE PUMP					
Output Voltage Range	V_{OUT}		4.5	5.5	V
Output Current	$I_{OUT(MAX)}$	C_X = 0.47µF	200		mA
FB Regulation Voltage	V_{FB}		1.222	1.271	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V	-50	+50	nA
FB Power-Ready Trip Level		Rising edge	1.09	1.16	V
NEGATIVE LOW-POWER CHARGE PUMP					
SUPN Input Supply Range	V_{SUPN}		2.7	13	V
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.2V, no load on DRVN		0.8	mA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = 13V		10	µA
FBN Regulation Voltage	V_{FBN}		-50	+50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = 0	-50	+50	nA
DRVN PCH On-Resistance				6	Ω
DRVN NCH On-Resistance		V_{FBN} = 50mV		5	Ω
		V_{FBN} = -50mV	20		kΩ
FBN Power-Ready Trip Level		Falling edge	80	165	mV
POSITIVE LOW-POWER CHARGE PUMP					
SUPP Input Supply Range	V_{SUPP}		2.7	13	V
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V, no load on DRVP		0.8	mA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = 13V		10	µA
FBP Regulation Voltage	V_{FBP}		1.20	1.30	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.5V	-50	+50	nA
DRVP PCH On-Resistance				6	Ω
DRVP NCH On-Resistance		V_{FBP} = 1.20V		5	Ω
		V_{FBP} = 1.30V	20		kΩ
FBP Power-Ready Trip Level		Rising edge	1.09	1.16	V

WWW.100Y.COM.TW

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{SUPM} = +3.0V, V_{SUPP} = V_{SUPM} = +5V, TGND = PGND = GND, $I_{\overline{SHDN}}$ = 22µA, C_{OUT} = 2 × 4.7µF, C_{REF} = 0.22µF, C_{INTG} = 1500pF, V_{OUT} = +5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

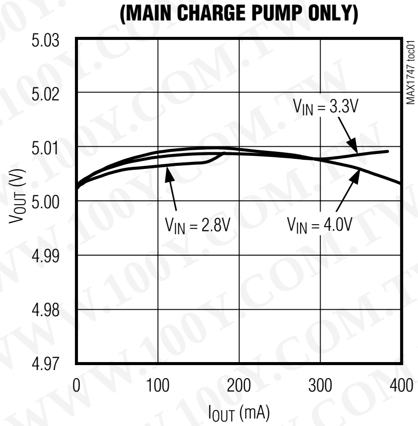
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
REFERENCE					
Reference Voltage	V_{REF}	-2µA < I_{REF} < 50µA	1.222	1.269	V
Reference Undervoltage Threshold		V_{REF} rising	0.95	1.18	V
LOGIC SIGNALS					
$\overline{SHDN}$ Input Low Voltage				0.4	V
$\overline{SHDN}$ Bias Voltage		$I_{\overline{SHDN}}$ = 22µA	580	900	mV
$\overline{SHDN}$ Input Current Range	$I_{\overline{SHDN}}$	For 200kHz to 2MHz operation	3	65	µA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA		0.5	V
$\overline{RDY}$ Output High Leakage		$V_{\overline{RDY}}$ = 13V		1	µA

Note 1: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

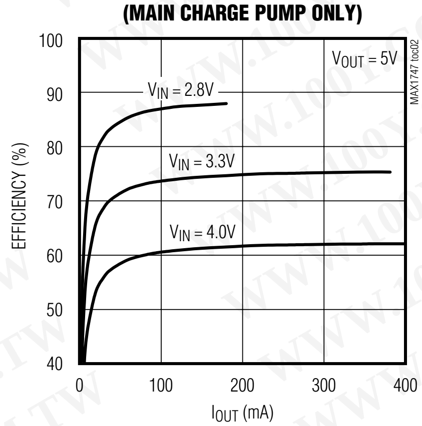
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = V_{SUPM} = +3.3V, T_A = +25°C, unless otherwise noted.)

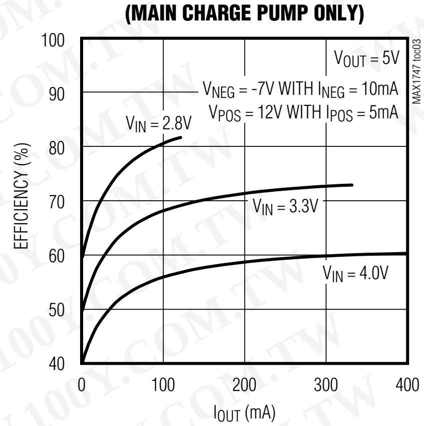
MAIN OUTPUT EFFICIENCY vs. LOAD CURRENT (MAIN CHARGE PUMP ONLY)



MAIN OUTPUT EFFICIENCY vs. LOAD CURRENT (MAIN CHARGE PUMP ONLY)



MAIN OUTPUT EFFICIENCY vs. LOAD CURRENT (MAIN CHARGE PUMP ONLY)

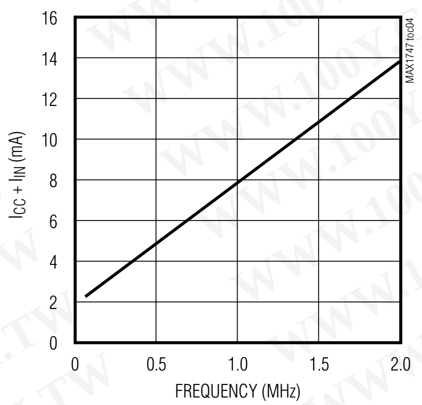


勝特力材料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

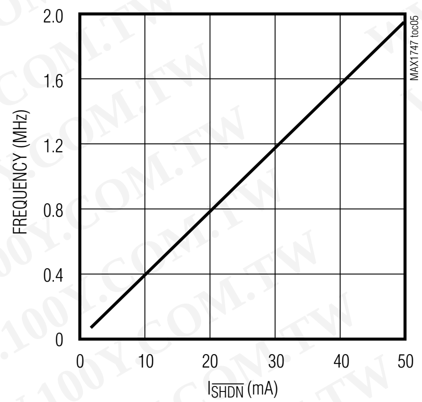
Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{IN} = V_{SUPM} = +3.3V$, $T_A = +25°C$, unless otherwise noted.)

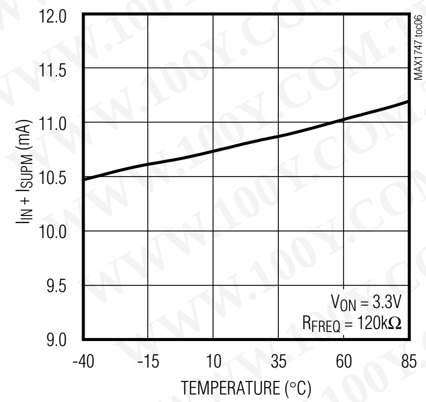
NO-LOAD SUPPLY CURRENT vs. SWITCHING FREQUENCY



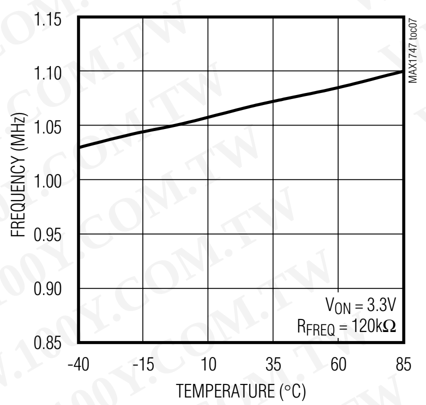
SWITCHING FREQUENCY vs. ISHDN



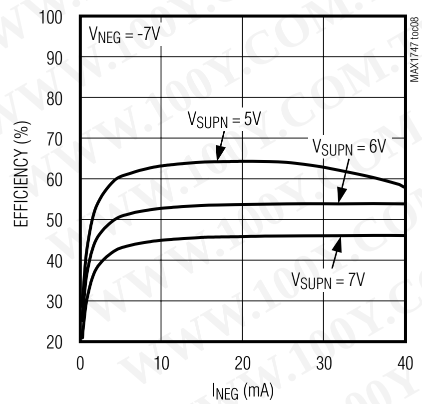
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



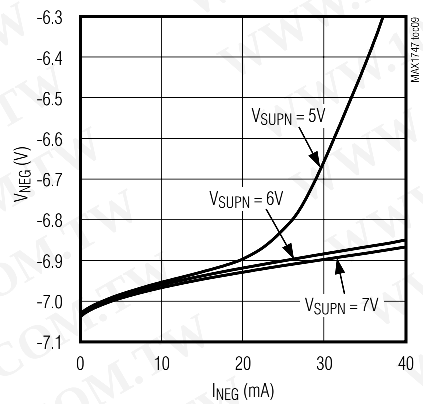
SWITCHING FREQUENCY vs. TEMPERATURE



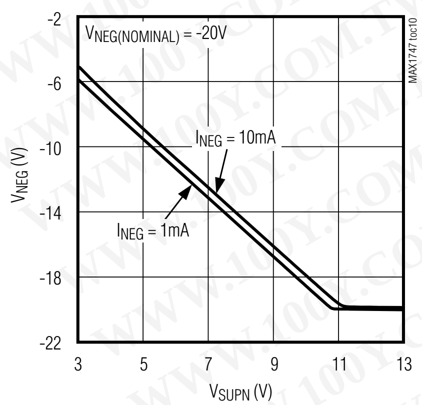
NEGATIVE LOW-POWER CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT



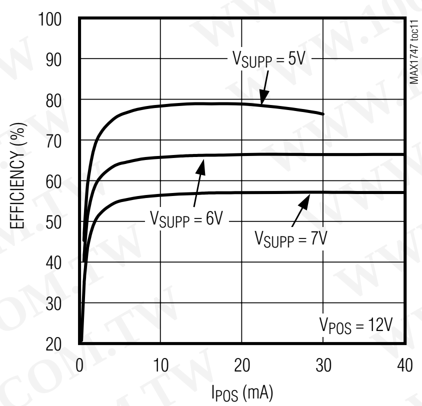
NEGATIVE LOW-POWER CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT



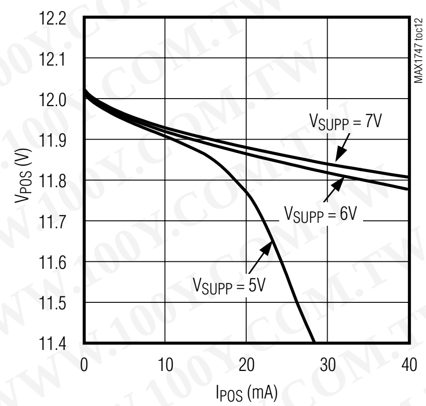
MAXIMUM NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



POSITIVE LOW-POWER CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT



POSITIVE LOW-POWER CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT

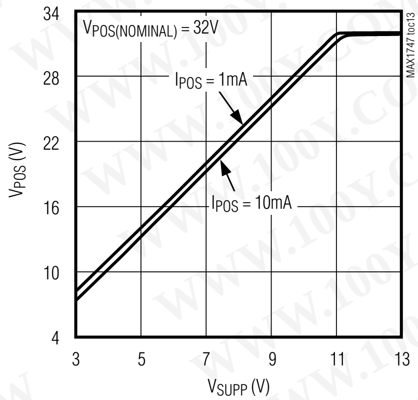


勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

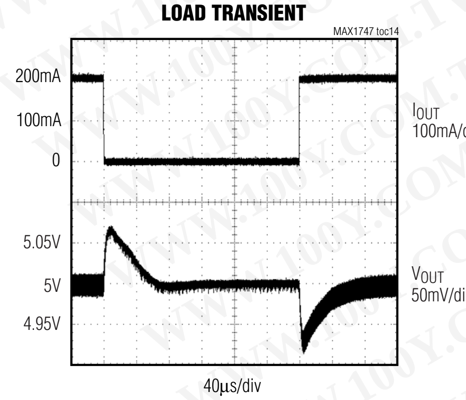
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = V_{SUPM} = +3.3V, T_A = +25°C, unless otherwise noted.)

MAXIMUM POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. SUPPLY VOLTAGE

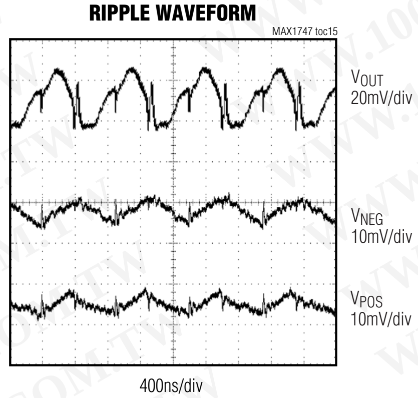


LOAD TRANSIENT



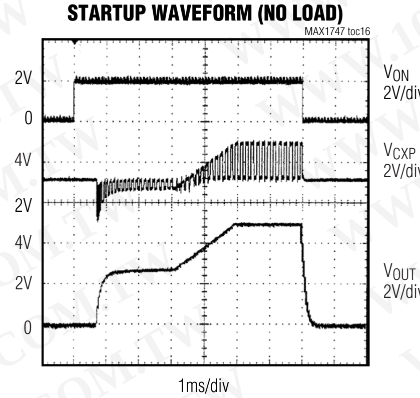
V_{IN} = 3.3V, V_{OUT} = 5.0V
R_{OUT} = 500Ω TO 25Ω
C_{INTG} = 1500pF

RIPPLE WAVEFORM



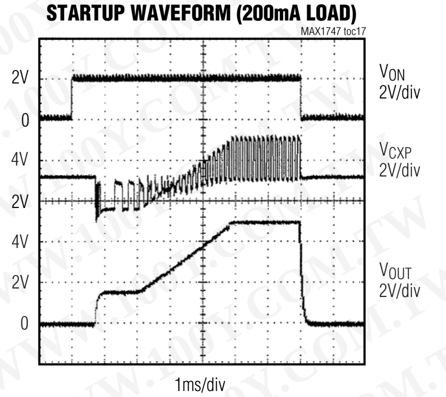
V_{OUT} = +5.0V, I_{OUT} = 200mA
V_{NEG} = -7V, I_{NEG} = 10mA
V_{POS} = +12V, I_{POS} = 5mA

STARTUP WAVEFORM (NO LOAD)



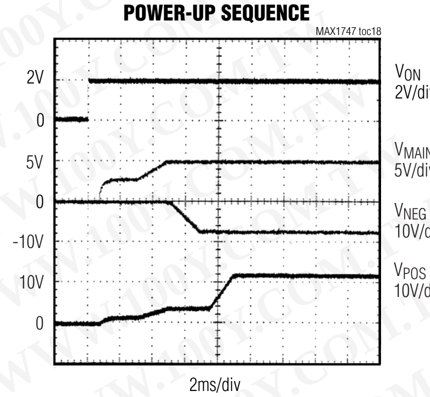
V_{OUT} = 5V, NO LOAD
ON CONNECTED TO $\overline{SHDN}$ THROUGH
A 58kΩ RESISTOR

STARTUP WAVEFORM (200mA LOAD)



V_{OUT} = 5V, R_{OUT} = 25Ω (200mA)
ON CONNECTED TO $\overline{SHDN}$ THROUGH
A 58kΩ RESISTOR

POWER-UP SEQUENCE



V_{MAIN} = 5V, V_{NEG} = -7V, V_{POS} = 12V
ON CONNECTED TO $\overline{SHDN}$ THROUGH
A 58kΩ RESISTOR

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Pin Description

PIN	NAME	FUNCTION
1, 2	TGND	Must be connected to ground.
3	$\overline{RDY}$	Active-Low Open-Drain Output. Indicates all outputs are ready. The R_{ON} is 125Ω (typ).
4	FB	Main Charge-Pump Feedback Input. Regulates to 1.25V nominal. Connect to the center of a feedback resistive divider between the main output (OUT) and analog ground (GND).
5	INTG	Main Charge-Pump Integrator Output. If used, connect 1500pF to analog ground (GND). To disable the integrator, connect to GND.
6	IN	Supply Input. +2.7V to +4.5V input range. Powers only the logic and reference. Bypass to analog ground (GND) with a 0.1µF capacitor as close to the pin as possible.
7	GND	Analog Ground. Connect to power ground (PGND) underneath the IC.
8	REF	Internal Reference Bypass Terminal. Connect a 0.22µF capacitor from this terminal to analog ground (GND). External load capability to 50µA. REF is disabled in shutdown.
9	FBP	Positive Charge-Pump Feedback Input. Regulates to 1.25V nominal. Connect feedback resistive divider to analog ground (GND).
10	FBN	Negative Charge-Pump Regulator Feedback Input. Regulates to 0V nominal. Connect feedback resistive divider to the reference (REF).
11	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ through an external resistor. When $\overline{SHDN}$ is pulled low, the device turns off and draws only 0.1µA. OUT is also pulled low through an internal 10Ω resistor in shutdown mode. When current is sourced into $\overline{SHDN}$ through R_{FREQ}, the device activates, and the $\overline{SHDN}$ input current sets the oscillator's switching frequency: R_{FREQ} (kΩ) = 45.5 (MHz / mA) × (V_{ON} - 0.7V) / f_{OSC} (MHz)
12	DRVN	Negative Charge-Pump Driver Output. Output high level is V_{SUPN}, and low level is PGND.
13	SUPN	Negative Charge-Pump Driver Supply Voltage. Bypass to power ground (PGND) with a 0.1µF capacitor.
14	DRVP	Positive Charge-Pump Driver Output. Output high level is V_{SUPP} and low level is PGND.
15	SUPP	Positive Charge-Pump Driver Supply Voltage. Bypass to power ground (PGND) with a 0.1µF capacitor.
16	PGND	Power Ground. Connect to analog ground (GND) underneath the IC.
17	CXN	Negative Terminal of the Main Charge-Pump Flying Capacitor
18	SUPM	Main Charge-Pump Supply Voltage Input
19	CXP	Positive Terminal of the Main Charge-Pump Flying Capacitor
20	OUT	Main Charge-Pump Output. Bypass to power ground (PGND) with 10µF for a 1MHz application (see *Output Capacitor Selection*). An internal 10Ω resistor discharges the output when the device is shut down.

Detailed Description

The MAX1747 is an efficient triple-output power supply for TFT LCD applications. The device contains one high-power charge pump and two low-power charge pumps. The MAX1747 charge pumps switch continuously at a constant frequency, so the output noise contains well-defined frequency components, and the circuit requires much smaller external capacitors for a given output ripple. The adjustable switching frequency is set by the current into the shutdown pin (see *Frequency Selection and Shutdown*).

The main charge pump uses internal MOSFETs with low R_{ON} to provide high output current. The adjustable output voltage of the main charge pump can be set up to 5.5V with external resistors. The dual low-power charge pumps independently regulate a positive output

勝特力材料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

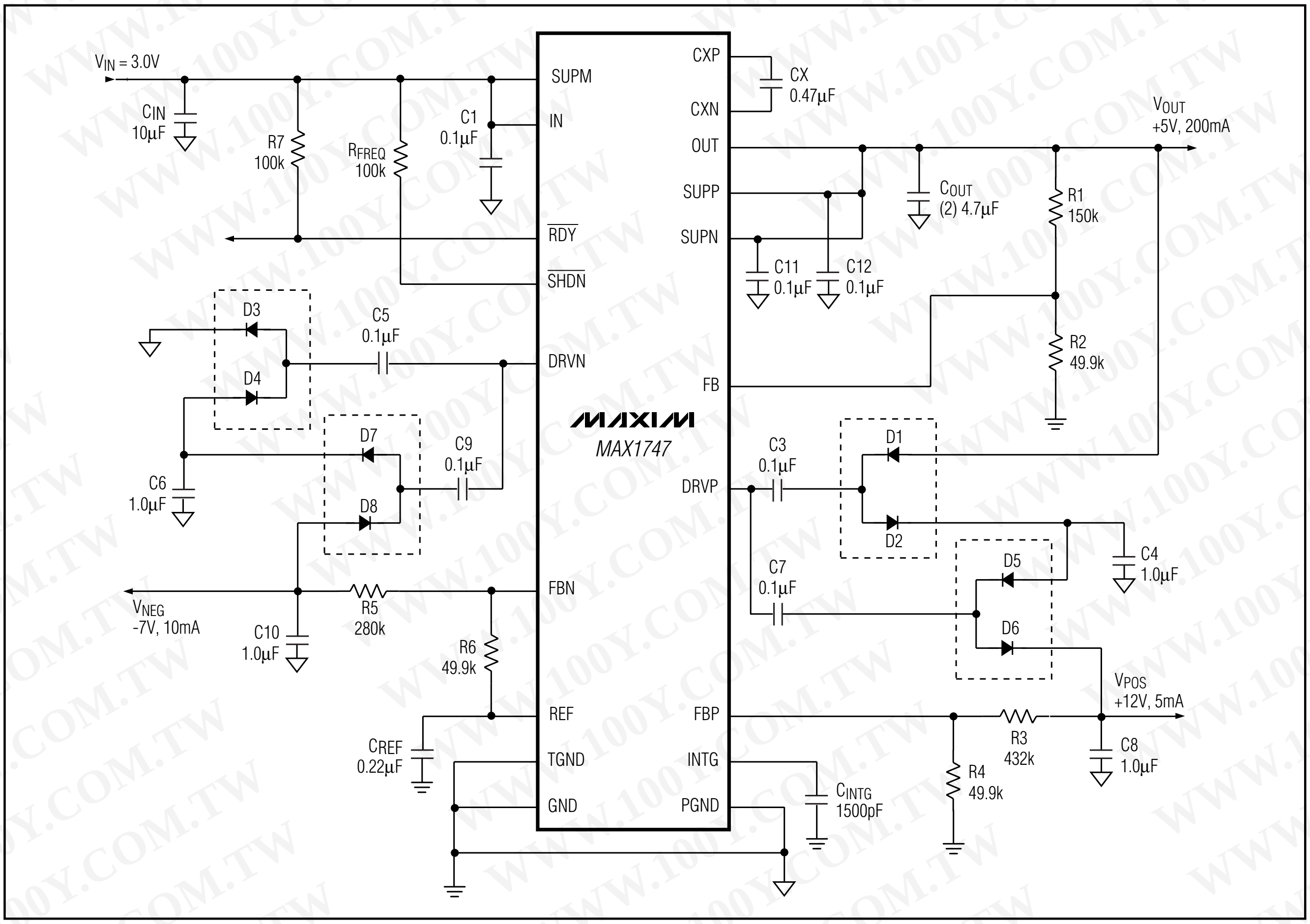


Figure 1. Typical Application Circuit

(V_{POS}) and a negative output (V_{NEG}). These two outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages above +35V and under -35V.

A proprietary regulation algorithm minimizes output ripple as well as capacitor sizes for all three charge pumps. Also included in the MAX1747 are a precision 1.25V reference that sources up to 50µA, shutdown, power-up sequencing, fault detection, and an active-low open-drain ready output.

Main Charge Pump

During the first half-cycle, the MAX1747 charges the flying capacitor (CX) by connecting it between the supply voltage (V_{SUPM}) and ground (Figure 2). This initial charge is controlled by the variable N-channel on-resistance. During the second half-cycle, the MAX1747 level shifts the flying capacitor by stacking the voltage across CX on top of the supply voltage. This transfers the sum of the two voltages to the output capacitor (C_{OUT}).

Dual Charge-Pump Regulators

The MAX1747 contains two individual low-power charge pumps. Using a single stage, the first charge pump inverts the supply voltage (V_{SUPN}) and provides a regulated negative output voltage. The second charge pump doubles the supply voltage (V_{SUPP}) and provides a regulated positive output voltage. The MAX1747 contains internal P-channel and N-channel MOSFETs to control the power transfer. The internal MOSFETs switch at a constant frequency set by the current into the shutdown pin (see *Frequency Selection and Shutdown*).

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Triple Charge-Pump TFT LCD DC-DC Converter

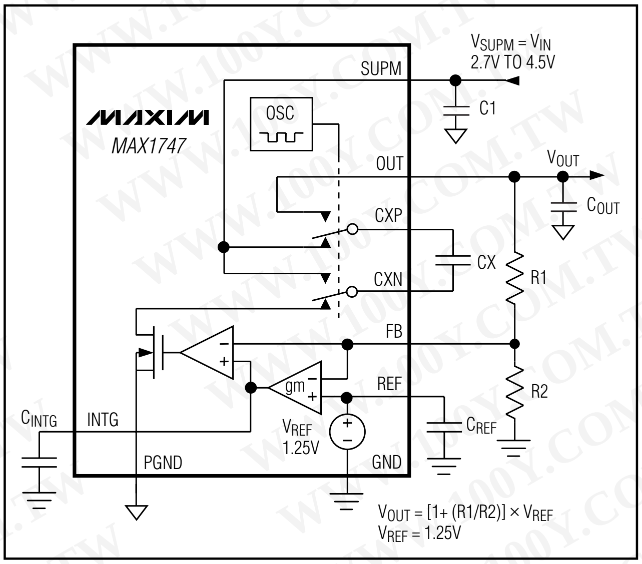


Figure 2. Main Charge-Pump Block Diagram

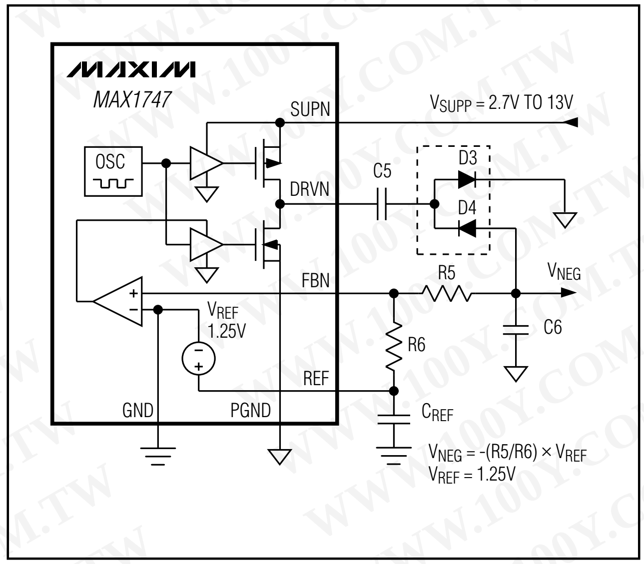


Figure 3. Negative Charge-Pump Block Diagram

Negative Charge Pump

During the first half-cycle, the P-channel MOSFET turns on, and flying capacitor C5 charges to V_{SUPN} minus a diode drop (Figure 3). During the second half-cycle, the P-channel MOSFET turns off, and the N-channel MOSFET turns on, level shifting C5. This connects C5 in parallel with the reservoir capacitor, C6. If the voltage across C6 minus a diode drop is lower than the voltage across C5, current flows from C5 to C6 until the diode (D4) turns off. The amount of charge transferred to the output is controlled by the variable N-channel R_{ON}.

Positive Charge Pump

During the first half-cycle, the N-channel MOSFET turns on and charges the flying capacitor, C3 (Figure 4). This initial charge is controlled by the variable N-channel R_{ON}. During the second half-cycle, the N-channel MOSFET turns off, and the P-channel MOSFET turns on, level shifting C3 by V_{SUPP} volts. This connects C3 in parallel with the reservoir capacitor, C4. If the voltage across C4 plus a diode drop ($V_{POS} + V_{DIODE}$) is smaller than the level-shifted flying capacitor voltage ($V_{C3} + V_{SUPP}$), charge flows from C3 to C4 until the diode (D2) turns off.

Frequency Selection and Shutdown

The shutdown pin ($\overline{SHDN}$) on the MAX1747 performs a dual function: it shuts down the device and determines the oscillator frequency. The $\overline{SHDN}$ input looks like a diode to ground and should be driven through a resistor (Figure 5).

Driving $\overline{SHDN}$ low forces all three MAX1747 converters into shutdown mode. When disabled, the supply current drops to 20µA (max) to maximize battery life, and OUT is pulled to ground through an internal 10Ω resistor. For the low-power charge pumps, the output capacitance and load current determine the rate at which each output voltage will decay. The device activates (see *Power-up Sequencing*) once $\overline{SHDN}$ is forward biased (minimum of 3µA of current). Do not leave $\overline{SHDN}$ floating. For a typical application where shutdown is used only to set the switching frequency, connect $\overline{SHDN}$ to the input (V_{IN} = 3.3V) with a 120kΩ resistor for a 1MHz switching frequency.

The bias current into $\overline{SHDN}$, programmed with an external resistor, determines the oscillator frequency (see *Typical Operating Characteristics*). To select the frequency, calculate the external resistor value, R_{FREQ}, using the following formula:

$$R_{FREQ} = 45.5\ (\text{MHz / mA}) \times (V_{ON} - 0.7V) / f_{OSC}$$

where R_{FREQ} is in kΩ and f_{OSC} is in MHz. Program the frequency in the 200kHz to 2MHz range. This frequency range corresponds to $\overline{SHDN}$ input currents between 3µA to 65µA. Proper operation of the oscillator is not guaranteed beyond these limits. Forcing $\overline{SHDN}$ below 400mV disables the device.

Soft-Start

For the MAX1747, soft-start is achieved by controlling the rise rate of the output voltage, regardless of output capacitance or output load, and limited only by the output impedance of the regulator (see Startup Waveforms

勝特力材料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

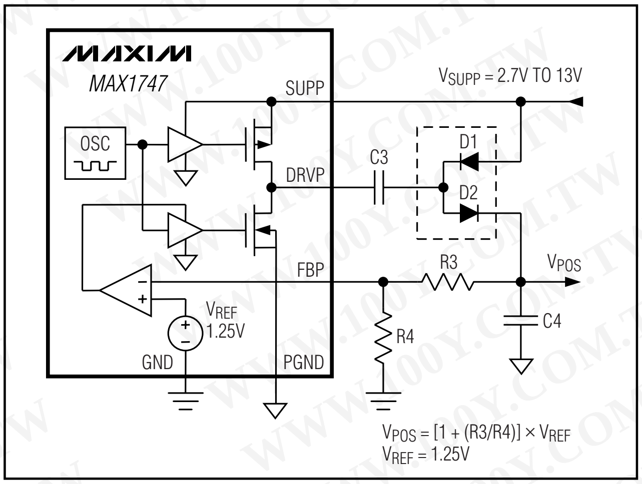


Figure 4. Positive Charge-Pump Block Diagram

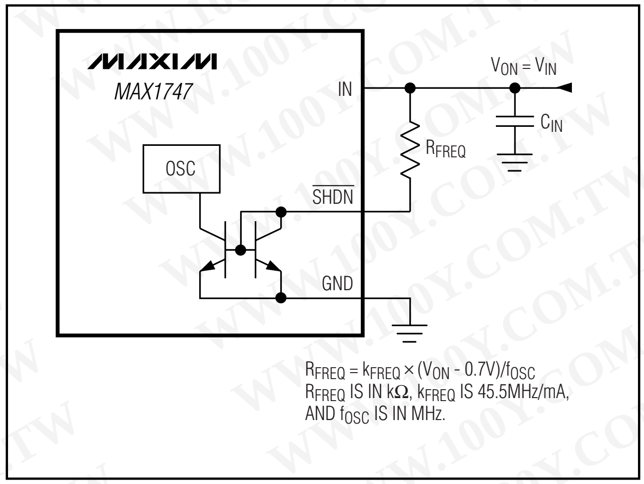


Figure 5. Frequency Adjustment

in the *Typical Operating Characteristics*). The main output voltage is controlled to be in regulation within 4096 clock cycles ($1/f_{OSC}$). The negative and positive low-power charge pumps are controlled to be in regulation within 2048 clock cycles.

Power-Up Sequencing

Upon power-up or exiting shutdown, the MAX1747 starts a power-up sequence. First, the reference powers up. Then the primary charge pump powers up with soft-start enabled. Once the main charge pump reaches 90% of its nominal value (V_{FB} > 1.125V), the negative charge pump turns on. When the negative output voltage reaches approximately 90% of its nominal value (V_{FBN} < 125mV), the positive charge pump starts up. Finally, when the positive output voltage reaches 90% of its nominal value (V_{FBP} > 1.125V), the active-low ready signal ($\overline{RDY}$) goes low (see *Power Ready*).

Fault Detection

Once $\overline{RDY}$ is low, and if any output falls below its fault detection threshold, $\overline{RDY}$ goes high impedance.

For the reference, the fault threshold is 1.05V. For the main charge pump, the fault threshold is 88% of its nominal value (V_{FB} < 1.1V). For the negative charge pump, the fault threshold is approximately 88% of its nominal value (V_{FBN} > 140mV). For the positive charge pump, the fault threshold is 88% of its nominal value (V_{FBP} < 1.1V).

Once an output faults, all outputs later in the power sequence shut down until the faulted output rises above its power-up threshold. For example, if the negative charge-pump output voltage falls below the fault-detection threshold, the main charge pump remains active while the positive charge pump stops switching and its output voltage decays, depending on output capacitance and load. The positive charge-pump output will not power up until the negative charge-pump output voltage rises above its power-up threshold (see *Power-Up Sequencing*).

Power Ready

Power ready is an open-drain output. When the power-up sequence is properly completed, the MOSFET turns on and pulls $\overline{RDY}$ low with a typical 125Ω R_{ON}. If a fault is detected, the internal open-drain MOSFET appears as a high impedance. Connect a 100kΩ pullup resistor between $\overline{RDY}$ and IN for a logic level output.

Voltage Reference

The voltage at REF is nominally 1.25V. The reference can source up to 50mA with excellent load regulation (see *Typical Operating Characteristics*). Connect a 0.22µF bypass capacitor between REF and GND. During shutdown, the reference is disabled.

Design Procedure

Efficiency Considerations

The efficiency characteristics of the MAX1747 regulated charge pumps are similar to a linear regulator. They are dominated by quiescent current at low output currents and by the input voltage at higher output currents (see *Typical Operating Characteristics*). Therefore, the maximum efficiency may be approximated by:

Efficiency $\cong V_{OUT} / (2 \times V_{SUPM})$ for the main charge pump

Efficiency $\cong - V_{NEG} / (V_{SUPN} \times N)$ for the negative low-power charge pump

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Efficiency $\cong V_{POS} / [V_{SUPP} \times (N+1)]$ for the positive low-power charge pump

where N is the number of charge-pump stages.

Output Voltage Selection

Adjust the main output voltage by connecting a voltage-divider from the output (V_{OUT}) to FB and GND (see *Typical Operating Circuit*). Adjust the negative low-power output voltage by connecting a voltage-divider from the output (V_{NEG}) to FBN to REF. Adjust the positive low-power output voltage by connecting a voltage-divider from the output (V_{POS}) to FBP to GND. Select R2, R4, and R6 in the 10kΩ to 200kΩ range. Calculate the remaining resistors with the following equations:

$$R1 = R2\,[(V_{OUT} / V_{REF}) - 1]$$

$$R3 = R4\,[(V_{POS} / V_{REF}) - 1]$$

$$R5 = R6\,|V_{NEG} / V_{REF}|$$

where V_{REF} = 1.25V. V_{OUT} may range from 4.5V to 5.5V, V_{POS} may range from V_{SUPP} to +35V, and V_{NEG} may range from 0 to -35V.

Flying Capacitors

Increasing the flying capacitor's value increases the output-current capability. Above a certain point, larger capacitor values lower the secondary pole formed by the transfer capacitor and switch R_{ON}, which destabilizes the output. For the main charge pump, use a ceramic capacitor based on the following equation:

$$C_X \le \frac{0.47\mu F \times MHz}{f_{OSC}}$$

For the low-power charge pumps, a 0.1µF ceramic capacitor works well in most applications. Smaller values may be used for lower current applications. Component suppliers are listed in Table 1.

Output Capacitors

For the main charge pump, use a ceramic capacitor based on the following equation:

$$C_{OUT} \ge \left[\left(\frac{20}{MHz} \times C_X \times f_{OSC}\right) \text{AND} \left(\frac{2\mu F \times MHz}{f_{OSC}}\right)\right]$$

For low-frequency applications (close to 200kHz), selection of the output capacitor is limited solely by the switching frequency. However, for high-frequency applications (close to 2MHz), selection of the output capacitor is limited by the secondary pole formed by the flying capacitor and switch on-resistance.

For the low-power charge pumps, the output capacitor should be anywhere from 5-times to 20-times larger than the flying capacitor, depending on the ripple tolerance. Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage.

Input Capacitors

Using an input capacitor with a value equal to or greater than the output capacitor is recommended. Place the capacitor as close to the IC as possible. If the source impedance or inductance of the input supply is large, additional input bypassing may be required.

For the low-power charge-pump inputs (SUPN and SUPP), using bypass capacitors with values equal to or greater than the flying capacitors is recommended. Place these capacitors as close to the supply voltage inputs as possible.

Rectifier Diodes

Use Schottky diodes with a current rating greater than 4 times the average output current, and with a voltage rating of 1.5 times V_{SUPP} for the positive charge pump and V_{SUPN} for the negative charge pump.

Integrator Capacitor

The MAX1747 contains an internal current integrator that improves the DC load regulation but increases the peak-to-peak transient voltage (see Load-Transient Waveform in the *Typical Operating Characteristics*). Connect a ceramic capacitor between INTG and GND based on the following equation:

$$C_{INTG} \ge \frac{150Hz \times C_{OUT}}{f_{OSC}}$$

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX
CAPACITORS		
AVX	803-946-0690	803-626-3123
Kemet	408-986-0424	408-986-1442
Sanyo	619-661-6835	619-661-1055
Taiyo Yuden	408-573-4150	408-573-4159
DIODES		
Central	516-435-1110	516-435-1824
International Rectifier	310-322-3331	310-322-3332
Motorola	602-303-5454	602-994-6430
Nihon	847-843-7500	847-843-2798

勝特力材料 886-3-5753170
胜特力电子(上海) 86-21-54151736
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

PC Board Layout and Grounding

Careful printed circuit layout is important to minimize ground bounce and noise. First, place the main charge-pump flying capacitor less than 0.2in (5mm) from the CXP and CXN pins with wide traces and no vias. Then place 0.1µF ceramic bypass capacitors near the charge-pump input pins (SUPP and SUPN) to the PGND pin. Keep the charge-pump circuitry as close to the IC as possible, using wide traces and avoiding vias when possible. Locate all feedback resistive dividers as close to their respective feedback pins as possible. The PC board should feature separate analog and power ground areas connected at only one point under the IC. To maximize output power and efficiency, and minimize output power ripple voltage, use extra-wide power ground traces, and solder the IC's power ground pin directly to it. Avoid having sensitive traces near the switching nodes and high-current lines.

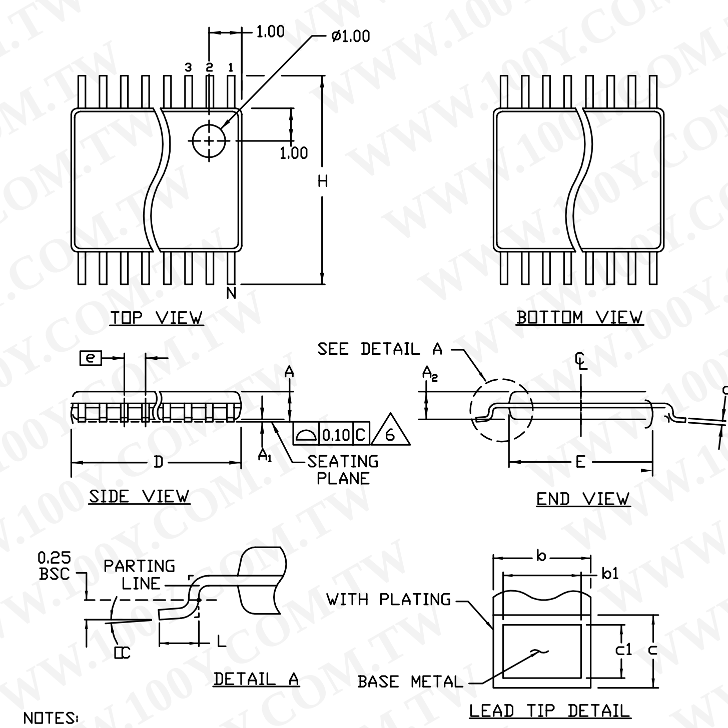
Refer to the MAX1747 evaluation kit for an example of proper board layout.

Chip Information

TRANSISTOR COUNT: 2534

Package Information

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AD	20	D	6.40	6.60	.252	.260
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS- AB, AC, AD, AE, AF
5. 'N' REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV D | 1/1

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

© 2000 Maxim Integrated Products Printed USA MAXIM is a registered trademark of Maxim Integrated Products.