Microsemi
LAWRENCE

TECHNICAL DATA

SILICON CONTROLLED RECTIFIER
Qualified per MIL-PRF-19500/276

Devices

2N2323	2N2324	2N2326	2N2328	
2N2323S	2N2324S	2N2326S	2N2328S	2N2329
2N2323A	2N2324A	2N2326A	2N2328A	2N2329S
2N2323AS	2N2324AS	2N2326AS	2N2328AS	

Qualified Level

JAN
JANTX
JANTXV

MAXIMUM RATINGS

Ratings	Sym	2N2323,S/ 2N2323A,S	2N2324,S/ 2N2324A,S	2N2326,S/ 2N2326A,S	2N2328,S/ 2N2328A,S	2N2329,S	Unit
Reverse Voltage	V_{RM}	50	100	200	300	400	Vdc
Working Peak Reverse Voltage	V_{RM}	75	150	300	400	500	Vpk
Forward Blocking Voltage	V_{FBXM}	$50^{(3/4)}$	$100^{(3/4)}$	$200^{(3/4)}$	$300^{(3/4)}$	$400^{(3)}$	Vpk
Average Forward Current [1]	I_O			0.22			Adc
Forward Current Surge Peak[2]	I_{FSM}			15			Adc
Cathode-Gate Current	V_{KGM}			6			Vpk
Operating Temperature	T_{op}			-65 to +125			^{0}C
Storage Junction Temp	T_{stg}			-65 to +150			^{0}C

1) This average forward current is for an ambient temperature of 80^0C and 180 electrical degrees of conduction.
2) Surge current is non-recurrent. The rate of rise of peak surge current shall not exceed 40 A during the first 5 µs after switching from the 'off' (blocking) to the 'on' (conducting) state. This is measured from the point where the thyristor voltage has decayed to 90% of its initial blocking value.
3) Gate connected to cathode through 1,000 ohm resistor.
4) Gate connected to cathode through 2,000 ohm resistor.

TO-5
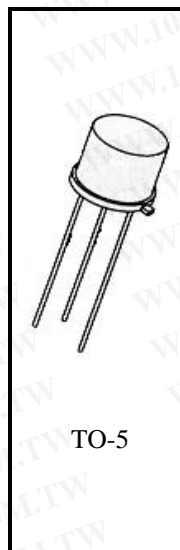
*See appendix A for package outline

ELECTRICAL CHARACTERISTICS

Characteristics		Symbol	Min.	Max.	Unit
SUBGROUP 2 TESTING					
Reverse Blocking Current					
R_2 = 1 kµ	2N2323 thru 2N2329				
	2N2323S thru 2N2329S				
R_2 = 2 kµ	2N2323A thru 2N2328A				
	2N2323AS thru 2N2328AS	I_{RBX1}		10	µAdc
V_R = 50 Vdc	2N2323, S, A, AS				
V_R = 100 Vdc	2N2324, S, A, AS				
V_R = 200 Vdc	2N2326, S, A, AS				
V_R = 300 Vdc	2N2328, S, A, AS				
V_R = 400 Vdc	2N2329, S,				

2N2323, A, AS, S; 2N2324, A, AS, S; 2N2326, A, AS, S; 2N2328, A, AS, S; 2N232, S JAN SERIES

ELECTRICAL CHARACTERISTICS (con't)

Characteristics		Symbol	Min.	Max.	Unit
Forward Blocking Current					
$R_2 = 1$ kΩ 2N2323 thru 2N2329					
2N2323S thru 2N2329S					
$R_2 = 2$ kΩ 2N2323A thru 2N2328A					
2N2323AS thru 2N2328AS		I_{FBX1}		10	μAdc
$V_R = 50$ Vdc 2N2323, S, A, AS					
$V_R = 100$ Vdc 2N2324, S, A, AS					
$V_R = 200$ Vdc 2N2326, S, A, AS					
$V_R = 300$ Vdc 2N2328, S, A, AS					
$V_R = 400$ Vdc 2N2329, S					
Reverse Gate Current					
$V_{KG} = 6$ Vdc		I_{KG}		200	μAdc
Gate Trigger Voltage and Current					
$V_2 = V_{FBX} = 6$ Vdc; $R_L = 100$ Ω					
$R_e = 1$ kΩ 2N2323 thru 2N2329 and		V_{GT1}	0.35	0.80	Vdc
2N2323S thru 2N2329S		I_{GT1}		200	μAdc
$R_e = 2$ kΩ 2N2323A thru 2N2328A and		V_{GT1}	0.35	0.60	Vdc
2N2323AS thru 2N2328AS		I_{GT1}		20	μAdc

SUBGROUP 4 TESTING

		Symbol	Min.	Max.	Unit
Exponential Rate of Voltage Rise $T_A = 125^0$C					
50 Ω $\leq R_L \leq 400$ Ω, C = 0.1 to 1.0 μF, repetition rate = 60 pps,					
test duration = 15 seconds					
dv/dt = 1.8 v/μs, $R_3 = 1$ kΩ 2N2323 thru 2N2329 and					
2N2323S thru 2N2329S					
dv/dt = 0.7 v/μs, $R_3 = 2$ kΩ 2N2323A thru 2N2328A and		V_{FBX}			Vdc
2N2323AS thru 2N2328AS					
$V_{AA} = 50$ Vdc 2N2323, S, A, AS			47		
$V_{AA} = 100$ Vdc 2N2324, S, A, AS			95		
$V_{AA} = 200$ Vdc 2N2326, S, A, AS			190		
$V_{AA} = 300$ Vdc 2N2328, S, A, AS			285		
$V_{AA} = 400$ Vdc 2N2329, S			380		
Forward "on" Voltage					
$i_{FM} = 4$a (pk) (pulse), pulse width = 8.5 ms, max; duty cycle = 2% max		V_{FM}		2.2	V(pk)
Holding Current					
$V_{AA} = 24$ Vdc max, $I_{F1} = 100$ mAdc, $I_{F2} = 10$ mAdc					
Gate trigger source voltage = 6 Vdc,					
trigger pulse width = 25 μs min., $R_2 = 330$ Ω					
$R_3 = 1$ kΩ 2N2323 thru 2N2329 and		I_{HOX}		2.0	mAdc
2N2323S thru 2N2329S					
$R_3 = 2$ kΩ 2N2323A thru 2N2328A and					
2N2323AS thru 2N2328AS					