

5 VOLT BULK ERASE FLASH MEMORY

28F010 and 28F020 (x8)

- Flash Electrical Chip-Erase
 - 1-Mbit: 1 Second Typical Chip-Erase
 - 2-Mbit: 2 Second Typical Chip-Erase
- Quick-Pulse Programming Algorithm
 - 10 μs Typical Byte-Program
 - 1-Mbit: 1 Second Chip-Program
 Nhit: 2 Second Chip Brogram
- 2-Mbit: 2 Second Chip-Program
- 100,000 Erase/Program Cycles
- 12.0 V ±5% V_{PP}
- High-Performance Read
 - 90 ns Maximum Access Time
- CMOS Low Power Consumption
 - 10 mA Typical Active Current
 - 50 μA Typical Standby Current
 0 Watts Data Retention Power
- Integrated Program/Erase Stop Timer

- Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- Noise Immunity Features
 - ±10% V_{CC} Tolerance
 - Maximum Latch-Up Immunity through EPI Processing
- ETOX™ Nonvolatile Flash Technology
 - EPROM-Compatible Process Base
 - High-Volume Manufacturing Experience
- JEDEC-Standard Pinouts
 - 32-Pin Plastic Dip
 - 32-Lead PLCC
 - 32-Lead TSOP

(See Packaging Spec., Order #231369)

■ Extended Temperature Options

The Intel® 5 Volt Bulk Erase CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F010 and 28F020 add electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after sale. The 28F010 and 28F020 increase memory flexibility, while contributing to time and cost savings.

The 28F010 is a 1024 kilobit nonvolatile memory organized as 131,072 bytes of eight bits. Similarly, the 28F020 is a 2048 kilobit nonvolatile memory organized as 262,144 bytes of eight bits. Both devices are offered in 32-pin plastic dip or 32-lead PLCC and TSOP packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Extended erase and program cycling capability is designed into Intel® ETOX™ (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0 V V_{PP} supply, the 28F010 and 28F020 perform 100,000 erase and program cycles—well within the time limits of the quick-pulse programming and quick-erase algorithms.

The Intel 28F010 and 28F020 employ advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 90 ns access time provides zero wait-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 μ A translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from -1 V to V_{CC} + 1 V.

With Intel ETOX process technology base, the 28F010 and 28F020 build on years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

December 1998

Order Number: 290663-001

28F010/28F020

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REVISION HISTORY

Number	Description
-001	This document combines datasheets for the 28F010 (order 290207) and 28F020 (order 290245), bulk erase devices.

28F010/28F020

1.0 **APPLICATIONS**

The Intel 28F010 and 28F020 flash memories provide nonvolatility along with the capability to perform over 100,000 electrical chip-erasure/ reprogram cycles. These features make the 28F010 and 28F020 an innovative alternative to disk, EEPROM, and battery-backed static RAM. Where periodic updates of code and data tables are the 28F010 and required. reprogrammability and nonvolatility make them the obvious and ideal replacements for EPROM.

Primary applications and operating systems stored in flash eliminate the slow disk-to-DRAM download process. This results in dramatic enhancement of performance and substantial reduction of power consumption—a consideration particularly important in portable equipment. Flash memory increases flexibility with electrical chip erasure and in-system update capability of operating systems and application code. With updatable code, system manufacturers can easily accommodate last-minute changes as revisions are made.

In diskless workstations and terminals, network traffic reduces to a minimum and systems are instant-on. Reliability exceeds that of electro-mechanical media. Often in these environments, power interruptions force extended re-boot periods for all networked terminals. This mishap is no longer an issue if boot code, operating systems, communication protocols and primary applications are flash resident in each terminal.

For embedded systems that rely on dynamic RAM/disk for main system memory or nonvolatile backup storage, the 28F010 and 28F020 flash memories offer a solid state alternative in a minimal form factor. The 28F010 and 28F020 provide higher performance, lower power consumption, instant-on capability, and allows an "eXecute in place" (XIP) memory hierarchy for code and data table reading. Additionally, the flash memory is more rugged and reliable in harsh environments where extreme temperatures and shock can cause disk-based systems to fail.

The need for code updates pervades all phases of a system's life—from prototyping to system manufacture to after sale service. The electrical chip-erasure and reprogramming ability of the 28F010 and 28F020 allow in-circuit alterability; this eliminates unnecessary handling and less reliable

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socketed connections, while adding greater test, manufacture, and update flexibility.

Material and labor costs associated with code changes increases at higher levels of system integration—the most costly being code updates after sale. Code "bugs," or the desire to augment system functionality, prompt after sale code updates. Field revisions to EPROM-based code requires the removal of EPROM components or entire boards. With the 28F010 and 28F020, code updates are implemented locally via an edge connector, or remotely over a communication link.

For systems currently using a high-density static RAM/battery configuration for data accumulation, flash memory's inherent nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable equipment and medical instruments, both requiring continuous performance. In addition, flash memory offers a considerable cost advantage over static RAM.

Flash memory's electrical chip erasure, byte programmability and complete nonvolatility fit well with data accumulation and recording needs. Electrical chip-erasure gives the designer a "blank slate" in which to log or record data. Data can be periodically off-loaded for analysis and the flash memory erased producing a new "blank slate."

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 depicts two 28F020s tied to the 80C186 system The 228F010 and 28F020 architecture minimize interface circuitry needed for complete incircuit updates of memory contents.

The outstanding feature of the TSOP (Thin Small Outline Package) is the 1.2 mm thickness. TSOP is particularly suited for portable equipment and applications requiring large amounts of flash memory.

With cost-effective in-system reprogramming, extended cycling capability, and true nonvolatility, the 28F010 and 28F020 offer advantages to the alternatives: EPROMs, EEPROMs, battery backed static RAM, or disk. EPROM-compatible read specifications, straightforward interfacing, and incircuit alterability offers designers unlimited flexibility to meet the high standards of today's designs.

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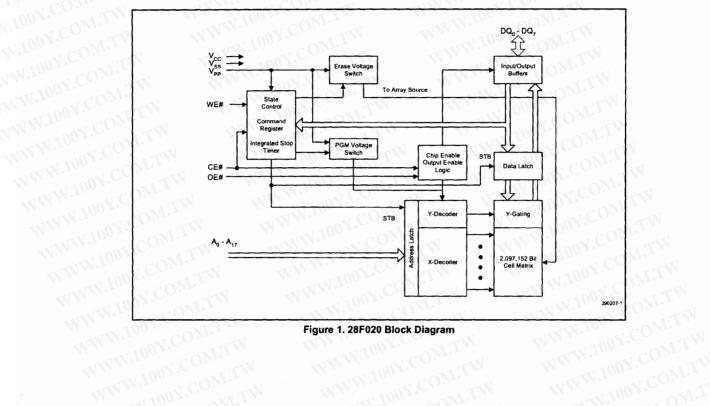


Figure 1. 28F020 Block Diagram WWW.100Y WWW.100Y.COM.T

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28F010/28F020

Table 1. Pin Description

Symbol A ₀ -A ₁₆	Type INPUT	Name and Function ADDRESS INPUTS for memory addresses. Addresses are internally
-1	, M.10	latched during a write cycle. 28F010: A[0-16], 28F020: A[0-17]
DQ ₀ –DQ ₇	INPUT/OUTPUT	DATA INPUT/OUTPUT: Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state off when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low; CE# high deselects the memory device and reduces power consumption to standby levels.
OE#	INPUT	OUTPUT ENABLE: Gates the devices output through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	WRITE ENABLE: Controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the WE# pulse.
-oM		Note: With V _{PP} ≤ 6.5 V, memory contents cannot be altered.
V _{PP}	TW	ERASE/PROGRAM POWER SUPPLY for writing the command register, erasing the entire array, or programming bytes in the array.
Vcc	V.I.A.	DEVICE POWER SUPPLY (5 V ±10%)
Vss	M.TW	GROUND
NC S	WTIE	NO INTERNAL CONNECTION to device. Pin may be driven or left floating.

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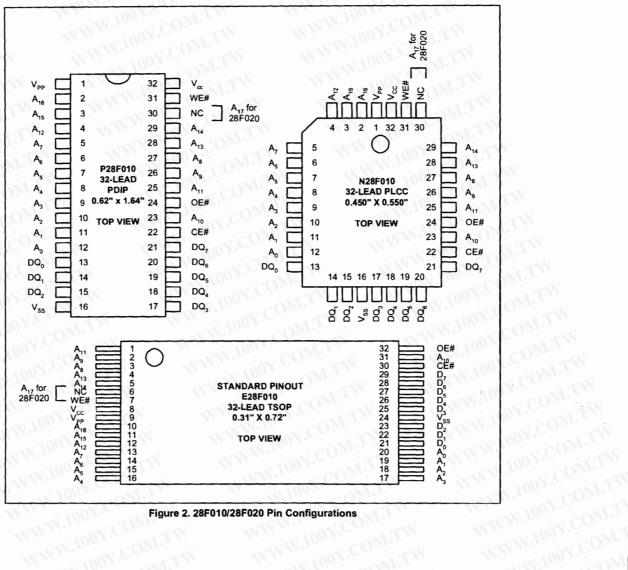


Figure 2. 28F010/28F020 Pin Configurations WWW.100Y.COM.TW

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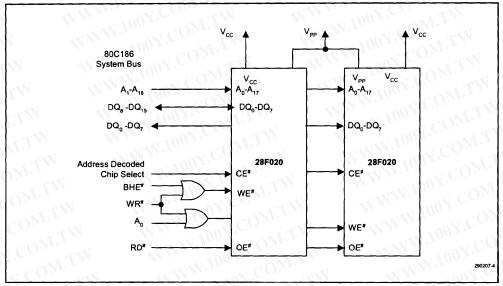


Figure 3. 28F020 in a 80C186 System

2.0 PRINCIPLES OF OPERATION

Flash memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 5 Volt Bulk Erase introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supplies during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 5 Volt Bulk Erase is a read-only memory. Manipulation of the external memory control pins yields the standard EPROM read, standby, output disable, and intelligent identifier operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the VPP pin. In addition, high voltage on VPP enables erasure and programming of the device. All functions associated with altening memory contents—intelligent identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the intelligent identifier codes, or output data for erase and program verification.

2.1 Integrated Stop Timer

Successive command write cycles define the durations of program and erase operations; specifically, the program or erase time durations are normally terminated by associated Program or Erase Verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer-terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate Verify or Reset command.

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Table 2. 28F010/28F020 Bus Operations

W	Mode	V _{PP} (1)	A ₀	Ag	CE#	OE#	WE#	DQ ₀ -DQ ₇
	Read	V _{PPL}	A ₀	A ₉	VIL	VIL	VIH	Data Out
	Output Disable	V _{PPL}	Х	X	VIL	VIH	V _{IH}	Tri-State
READ-ONLY	Standby	V _{PPL}	Х	X	VIH	Х	X	Tri-State
	Intelligent Identifier (Mfr)(2)	V _{PPL}	V _{IL}	V _{ID} (3)	VIL	VIL	ViH	Data = 89H
	Intelligent Identifier (Device)(2)	V _{PPL}	VIH	V _{ID} (3)	VIL	VIL	ViH	Data = B4H
LTW	Read	VPPH	Ao	A ₉	VIL	VIL	ViH	Data Out(4)
READ/WRITE	Output Disable	V _{PPH}	X	Х	VIL	ViH	VIH	Tri-State
	Standby ⁽⁵⁾	V _{PPH}	X	Νx	V _{IH} ¬	X	Х	Tri-State
	Write	VPPH	Ao	A ₉	VIL	ViH	VIL	Data In(6)

NOTES:

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- Refer to DC Characteristics. When V_{PP} = V_{PPL} memory contents can be read but not written or erased. 1.
- Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
- VID is the intelligent identifier high voltage. Refer to DC Characteristics.
- Read operations with VPP = VPPH may access array data or the intelligent identifier codes
- With VPP at high voltage, the standby current equals Icc + IPP (standby).
- Refer to Table 3 for valid data-in during a write operation.
- X can be VIL or VIH.

2.2 **Write Protection**

The command register is only active when VPP is at high voltage. Depending upon the application, the system designer may choose to make the VPP power supply switchable—available only when memory updates are desired. When VPP = VPPL, the contents of the register default to the Read command, making the 28F010 and 28F020 readonly memories. In this mode, the memory contents cannot be altered.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this case, all command register functions are inhibited whenever V_{CC} is below the write lockout voltage V_{LKO}. (See Section 3.4, Power-Up/Down Protection.) The 28F010 and 28F020 are designed to accommodate either design practice, and to encourage optimization of the processor memory interface.

The two-step program/erase write sequence to the command register provides additional software write protections. WWW.100Y.COM.TW

BUS OPERATIONS 2.2.1

2.2.1.1 Read

The 28F010 and 28F020 have two control functions, both of which must be logically active, to obtain data at the outputs. Chip Enable (CE#) is the power control and should be used for device selection. Output Enable (OE#) is the output control and should be used to gate data from the output pins, independent of device selection. Refer to the AC read timing waveforms.

When VPP is high (VPPH), the read operation can be used to access array data, to output the intelligent identifier codes, and to access data for program/erase verification. When Vpp is low (VppL), the read operation can only access the array data.

2.2.1.2 **Output Disable**

With OE# at a logic-high level (VIH), output from the device is disabled. Output pins are placed in a highimpedance state.



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2.2.1.3 Standby

With CE# at a logic-high level, the standby operation disables most of the 28F010 and 28F020's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the OE# signal. If the 28F010 and 28F020 are deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

2.2.1.4 Intelligent Identifier Operation

The intelligent identifier operation outputs the manufacturer code (89H) and device code (B4H for 28F010, BDH for 28F020). Programming equipment automatically matches the device with its proper erase and programming algorithms.

With CE# and OE# at a logic low level, raising A9 to high voltage VID (see DC Characteristics) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer and device codes can also be read via the command register, for instances where the 28F010 and 28F020 are erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (B4H for 28F010, BDH for 28F020).

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2.2.1.5 Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the VPP pin. The contents of the register serve as input to the internal state machine. The state machine outputs dictate the function of the

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing WE# to a logic-low level (VIL), while CE# is low. Addresses are latched on the falling edge of WE#, while data is latched on the rising edge of the WE# pulse. Standard microprocessor write timings are used.

Refer to AC Characteristics-Write/Erase/Program Operations and the erase/programming waveforms for specific timing parameters.

2.2.2 **COMMAND DEFINITIONS**

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When low voltage is applied to the VPP pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are operations are selected by writing specific data patterns into the command register. Table 3 defines WW.100Y.COM.TW 28F010/28F020 register commands.

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Table 3. Command Definitions

WW	400	Firs	t Bus Cycle	W	Seco	nd Bus Cycle	N
Command	Bus Cycles Req'd	Operation(1)	Address(2)	Data(3)	Operation ⁽¹⁾	Address ⁽²⁾	Data(3)
Read Memory	11.1	Write	Х	00H	W.100	COM	. Y
Read Intelligent Identifier Codes(4)	3	Write	IA	90H	Read	IA	ID
Set-Up Erase/Erase ⁽⁵⁾	2	Write) X	20H	Write	X.CO	20H
Erase Verify ⁽⁵⁾	2	Write	EA	(A0H	Read	x C	EVD
Set-Up Program/ Program(6)	2	Write	COX	40H	Write	PA	PD
Program Verify ⁽⁶⁾	2	Write	. X	C0H	Read	X	PVD
Reset(7)	2	Write	< xO [™]	FFH	Write	X	FFH

NOTES:

- 1. Bus operations are defined in Table 2.
- 2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
 - EA ≈ Erase Address: Address of memory location to be read during erase verify PA ≈ Program Address: Address of memory location to be programmed.
 - PA ≈ Program Address: Address of memory location to be programmed Addresses are latched on the falling edge of the WE# pulse.
- ID = Identifier Data: Data read from location IA during device identification (Mfr = 89H, Device = (B4H for 28F010, BDH for 28F020).
 - EVD = Erase Verify Data: Data read from location EA during erase verify.

 PD = Program Data: Data to be programmed at location PA. Data is latched on the rising edge of WE#
 - PD = Program Data: Data to be programmed at location PA. Data is latched on the rising edge of WE#.

 PVD = Program Verify Data: Data read from location PA during program verify. PA is latched on the Program command.
- 4. Following the Read Intelligent ID command, two read operations access manufacturer and device codes.
- 5. Figure 5 illustrates the 28F010/28F020 Quick-Erase Algorithm flowchart.
- 6. Figure 4 illustrates the 28F010/28F020 Quick-Pulse Programming Algorithm flowchart.
- 7. The second bus cycle must be followed by the desired command register write.

2.2.2.1 Read Command

While VPP is high, for erasure and programming, memory contents can be accessed via the Read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hardwired to the 28F010 or the 28F020, the device powers-up and remains enabled for reads until the command register contents are changed.

Refer to the *AC Characteristics—Read-Only Operations* and waveforms for specific timing parameters.

2.2.2.2 Intelligent Identifier Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically accessignature codes by raising A₉ to a high voltage. However, multiplexing high voltage onto address lines is not a desired system design practice.

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The 28F010 and 28F020 contain an intelligent identifier operation to supplement traditional PROMprogramming methodology. The operation is initiated by writing 90H into the command register. Following the command Write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of (B4H for 28F010, BDH for 28F020). To terminate the operation, it is necessary to write another valid command into the register.

2.2.2.3 Set-Up Erase/Erase Commands

Set-Up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the Erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the WE# pulse and terminates with the rising edge of the next WE# pulse (i.e., Erase Verify command)

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the pin. In the absence of this high voltage, memory contents are against erasure. Refer Characteristics-Write/Erase/Program Only Opertiming ations and waveforms for specific parameters.

2.2.2.4 **Erase Verify Command**

The Erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the WE# pulse. The register write terminates the erase operation with the rising edge of its WE# pulse.

The 5 Volt Bulk Erase applies an internallygenerated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The Erase Verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer Section 2.2.2.3. Set-Up Erase/Erase Commands. Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g., Program Set-Up) to the command register. 28F010/28F020 Figure 5. the Quick-Erase Algorithm flowchart, illustrates how commands and bus operations are combined to perform electrical erasure of the 28F010 and 28F020. Refer to AC Characteristics—Write/Erase/Program Only Operwaveforms for specific timing ations and parameters.

2.2.2.5 Set-Up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up

Once the program set-up operation is performed, the next WE# pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the WE# pulse. Data is internally latched on the rising edge of the WE# pulse. The rising edge of WE# also begins the programming operation. The programming operation terminates with the next rising edge of WE#, used to write the Program Verify command. Refer to AC Characteristics—Write/Erase/Program Only Operations and Waveforms for specific timing parameters

2.2.2.6 **Program Verify Command**

The 5 Volt Bulk Erase is programmed on a byte-by-Byte programming may or at random. Following byte basis. sequentially programming operation, the byte just programmed must be verified

The program verify operation is initiated by writing COH into the command register. The register write terminates the programming operation with the rising edge of its WE# pulse. The program verify operation stages the device for verification of the byte last programmed. No new address information is latched.

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The 5 Volt Bulk Erase applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 5, the 28F010/28F020 Quick-Pulse Programming Algorithm flowchart, illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Characteristics—Write/Erase/Program Only Operations and waveforms for specific timing parameters.

2.2.2.7 Reset Command

A Reset command is provided as a means to safely abort the Erase or Program command sequences. Following either Set-Up command (Erase or Program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

2.2.3 EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure.

The 5 Volt Bulk Erase is capable or 100,000 program/erase cycles. The device is programmed and erased using Intel's quick-pulse programming

and quick- erase algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

2.2.4 QUICK-PULSE PROGRAMMING ALGORITHM

The quick-pulse programming algorithm uses programming operations of 10 µs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage Figure 4 illustrates the 28F010/28F020 Quick-Pulse Programming Algorithm flowchart.

2.2.5 QUICK-ERASE ALGORITHM

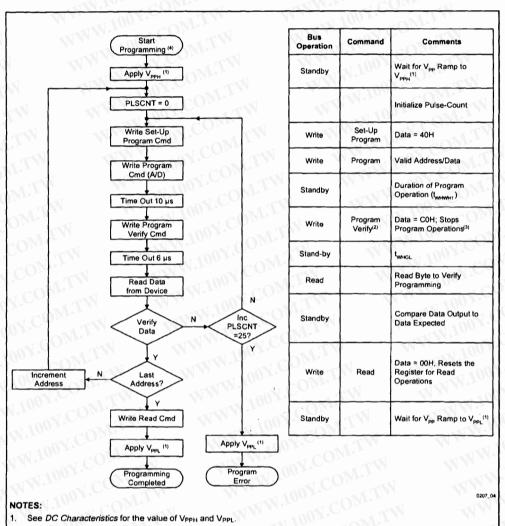
Intel's quick-erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the quick-pulse programming algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The 5 Volt Bulk Erase is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the quick-pulse programming algorithm, in approximately two seconds.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 5 illustrates the 28F010/28F020 Quick-Erase Algorithm flowchart.

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- 2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
- Refer to Principles of Operation.
- CAUTION: The algorithm must be followed to ensure proper and reliable operation of the device.

Figure 4. 28F010/28F020 Quick-Pulse Programming Algorithm

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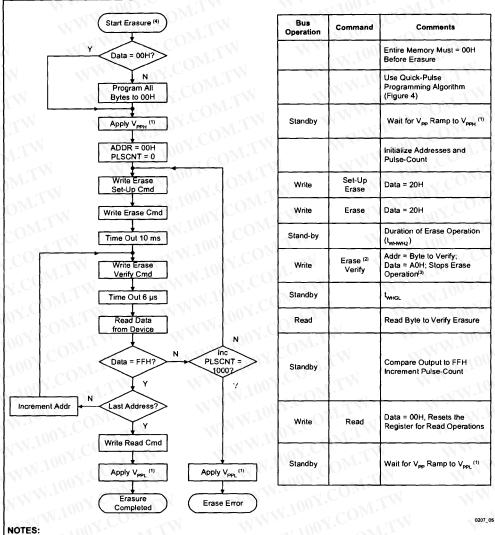
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- 1. See DC Characteristics for the value of VPPH and VPPI.
- Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the Read command.
- Refer to Principles of Operation.
- CAUTION: The algorithm must be followed to ensure proper and reliable operation of the device.

Figure 5. 28F010/28F020 Quick-Erase Algorithm WWW.100Y.COM.T



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3.0 DESIGN CONSIDERATIONS

3.1 Two-Line Output Control

Flash memories are often used in larger memory arrays. Intel provides two read control inputs to accommodate multiple memory connections. Two-line control provides for:

- a. the lowest possible memory power dissipation and.
- complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address decoder output should drive chip-enable, while the system's read signal controls all flash memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

3.2 Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chipenable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μ F ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection, between Vcc and Vss. The bulk capacitor will overcome voltage slumps caused by printed circuit board trace inductance, and will supply charge to the smaller capacitors as needed.

3.3 V_{PP} Trace on Printed Circuit Boards

Programming flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

3.4 Power-Up/Down Protection

The 5 Volt Bulk Erase is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, the 5 Volt Bulk Erase is indifferent as to which power supply, VPP or VCC, powers up first. Power supply sequencing is not required. Internal circuitry in the 5 Volt Bulk Erase ensures that the command register is reset to the read mode on power-up.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The control register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

3.5 5 Volt Bulk Erase Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases the usable battery life of your system because the usable battery life of your system because the Usable battery life of your system because the retain code or data when the system is off. Table 4 illustrates the power dissipated when updating the 5 Volt Bulk Erase.

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Table 4. 5 Volt Bulk Erase Typical Update Power Dissipation(4)

Operation	Notes	Power Dissipation (Watt-Seconds				
WWW.LOOV.C		28F010	28F020			
Array Program/Program Verify	ON IN	0.171	0.34			
Array Erase/Erase Verify	CON 2	0.136	0.37			
One Complete Cycle	3	0.478	1.05			

NOTES:

- Formula to calculate typical Program/Program Verify Power = [V_{PP} × # Bytes × typical # Prog Pulses (twhwht × I_{PP2} typical + twhGL × I_{PP4} typical)] + [V_{CC} × # Bytes × typical # Prog Pulses (twhwht × I_{CC2} typical + twhGL × I_{CC4} typical)].
- Formula to calculate typical Erase/Erase Verify Power = [V_{PP} (V_{PP3} typical × t_{ERASE} typical + 1_{PP5} typical × t_{WHGL} × # Bytes)] + [V_{CC} (I_{CC3} typical × t_{ERASE} typical + I_{CC5} typical × t_{WHGL} × # Bytes)].
- 3. One Complete Cycle = Array Preprogram + Array Erase + Program.
- 4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.



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4.0 **ELECTRICAL SPECIFICATIONS**

4.1 Absolute Maximum Ratings*

Operating Temperature	
During Read	0 °C to +70 °C(1)
During Erase/Program	0 °C to +70 °C(1)
Operating Temperature	
During Read	40 °C to +85 °C(2)
During Erase/Program	40 °C to +85 °C(2)
Temperature Under Bias	10 °C to +80 °C(1)
Temperature Under Bias	50 °C to +95 °C(2)
Storage Temperature	65 °C to +125 °C
Voltage on Any Pin with	
Respect to Ground	2.0 V to +7.0 V(3)
Voltage on Pin A ₉ with	
Respect to Ground	2.0 V to +13.5 V(3, 4)
V _{PP} Supply Voltage with	
Respect to Ground	
During Erase/Program	2.0 V to +14.0 V(3, 4)
V _{CC} Supply Voltage with	
Respect to Ground	
Output Short Circuit Current.	100 mA(5)
4.2 Operating Con	ditions
10 1 - COM-2	

NOTICE: This is a production datasheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the Operating Conditions is not recommended and extended exposure beyond the Operating Conditions may affect device reliability.

NOTES:

- Operating Temperature is for commercial product as defined by this specification.
- Operating Temperature is for extended temperature products as defined by this specification.
- Minimum DC input voltage is -0.5 V. During transitions, inputs may undershoot to -2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is Vcc 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
- Maximum DC voltage on $A_{\mbox{\scriptsize 9}}$ or $V_{\mbox{\scriptsize PP}}$ may overshoot to +14.0 V for periods less than 20 ns.
- Output shorted for no more than one second. No more than one output shorted at a time.
- See AC Testing Input/Output Waveform (Figure 6) and AC Testing Load Circuit (Figure 7) for testing WWW.100Y.C characteristics.

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V.CU	TW WWW	Lin	nits	100
Symbol	Parameter	Min	Max	Unit
TA	Operating Temperature(1)	0,0	70	°C
TA	Operating Temperature(2)	-40	+85	°C
Vcc	V _{CC} Supply Voltage (10%) ⁽⁶⁾	4.50	5.50	V
Vcc	V _{CC} Supply Voltage (5%) ⁽⁷⁾	4.75	5.25	V

4.3 Capacitance

Maria	100X.CO		Limits		W	1/1/4
Symbol	Parameter	Notes	Min	Max	Unit	Conditions
Cin	Address/Control Capacitance	1	Wire	4 (8)	pF	V _{IN} = 0 V
Cout	Output Capacitance	1	M.Iud	12	pF	V _{OUT} = 0 V

NOTE:

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DC Characteristics—28F010—TTL/NMOS Compatible 4.4 **Commercial Products**

	WWW.LOOX.C	O_{Mr}	TXV	Limits		1111	1007.COM
Symbol	Parameter Input Leakage Current	Notes 1	Min	Typ(3)	Max ±1.0	Unit μA	Vcc = Vcc Max
I _{LO}	Output Leakage Current	10	M.T	N KN	±10	μА	V _{IN} = V _{CC} or V _{SS} V _{CC} = V _{CC} Max V _{OUT} = V _{CC} or V _{SS}
Iccs	V _{CC} Standby Current	VIC	2 <u>141-7</u>	0.3	1.0	mA	V _{CC} = V _{CC} Max CE# = V _{IH}
lcc1	Vcc Active Read Current	001/.	COD	10	30	mA	V _{CC} = V _{CC} Max, CE# = V f = 6 MHz, I _{OUT} = 0 mA
lcc2	V _{CC} Programming Current	1, 2	60	1.0	10	mA	Programming in Progress
I _{CC3}	V _{CC} Erase Current	1,2	N.O.	5.0	15	mA	Erasure in Progress
Icc4	V _{CC} Program Verify Current	1, 2	2 5.0 15		15	mA	V _{PP} ≈ V _{PPH} Program Verify in Progres
I _{CC5}	V _{CC} Erase Verify Current	1, 2	001 00 x .	5.0	15	mA	V _{PP} ≈ V _{PPH} Erase Verify in Progress
IPPS	V _{PP} Leakage Current	111	100		±10	μΑ	V _{PP} ≤ V _{CC}
I _{PP1}	V _{PP} Read Current or Standby Current	111	100	90	200	μА	VPP > VCC
)U - s1.(OM	al W	11.10	ov.C	±10.0		V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Programming Current	1, 2	W.I	8.0	30	mA	V _{PP} = V _{PPH} Programming in Progress
Іррз	V _{PP} Erase Current	1, 2	NW:	6.0	30	mA	V _{PP} = V _{PPH} Erasure in Progress
I _{PP4}	V _{PP} Program Verify Current	1, 2		2.0	5.0	mA	V _{PP} = V _{PPH} Program Verify in Progre
I _{PP5}	V _{PP} Erase Verify Current	1, 2	WV	2.0	5.0	mA	V _{PP} = V _{PPH} Erase Verify in Progress
VIL	Input Low Voltage		-0.5		0.8	V	NI.
V _{IH}	Input High Voltage	I .	2.0	WW	V _{CC} + 0.5	V	OM.
V _{OL}	Output Low Voltage	N		NW	0.45	V	V _{CC} = V _{CC} Min I _{OL} = 5.8 mA
V _{OH1}	Output High Voltage	LM.	2.4	WV	NW.	0 A 3	V _{CC} = V _{CC} Min I _{OH} = -2.5 mA
V _{ID}	A ₉ Intelligent Identifier Voltage	TV	11.50	V	13.00	V	N.COM.I



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28F010/28F020

DC Characteristics—28F010—TTL/NMOS Compatible 4.4 Commercial Products (Continued)

	W.IV	JOM.	- 1	Limits		M.	COM
Symbol	Parameter	Notes	Min	Typ(3)	Max	Unit	Test Conditions
liD	A ₉ Intelligent Identifier Current	1, 2	LTV	90	200	μA	$A_9 = V_{ID}$
V _{PPL}	V _{PP} during Read-Only Operations	N.CO	0.00	W	6.5	V	NOTE: Erase/Program are Inhibited when V _{PP} = V _{PPL}
V _{PPH}	V _{PP} during Read/Write Operations	007.C	11.40	IW	12.60	٧	MM: 100X.COM
V _{LKO}	V _{CC} Erase/Write Lock Voltage	1001.	2.5	LTW	-1	٧Ń	WW.1007.CO

NOTES:

Sampled, not 100% tested.

All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, V_{PP} = 12.0 V, T = 25 °C. These currents are WWW.100Y.COM.TW valid for all product versions (packages and speeds).

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"Typicals" are not guaranteed, but based on a limited number of samples from production lots. WWW.100Y.COM WWW.100Y.COM

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28F010/28F020



DC Characteristics—28F020—TTL/NMOS Compatible 4.5 **Commercial Products**

Symbol	Parameter	Notes	Min	Limits Typ ⁽³⁾	Max	Unit	Test Conditions
ILI	Input Leakage Current	COM	TW	170	±1.0	μA	V _{CC} = V _{CC} Max V _{IN} = V _{CC} or V _{SS}
ILO	Output Leakage Current	.c ⁰	1.1	N	±10	μА	V _{CC} = V _{CC} Max V _{OUT} = V _{CC} or V _{SS}
Iccs	V _{CC} Standby Current	N.CC	WI.	0.3	1.0	mA	V _{CC} = V _{CC} Max CE# = V _{IH}
lcc1	V _{CC} Active Read Current	ovi.C	COM	10	30	mA	V _{CC} = V _{CC} Max CE# = V _{IL} f = 6 MHz l _{OUT} = 0 mA
lcc2	V _{CC} Programming Current	1, 2	CO	1.0	10	mA	Programming in Progress
Іссз	V _{CC} Erase Current	1, 2	of CS	5.0	15	mA	Erasure in Progress
Icc4	V _{CC} Program Verify Current	1, 2	oy.C	5.0	15	mA	V _{PP} = V _{PPH} Program Verify in Progress
I _{CC5}	V _{CC} Erase Verify Current	1, 2	001	5.0	15	mA	V _{PP} = V _{PPH} Erase Verify in Progress
IPPS	V _{PP} Leakage Current	NT	100	.Co	±10	μA	V _{PP} ≤ V _{CC}
I _{PP1}	V _{PP} Read Current, ID Current	11	v.100	90	200	μА	V _{PP} > V _{CC}
OOY.C	or Standby Current	M.M.	. 11	01.0	±10	LIN	V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Programming Current	1, 2	TVI.	8/.	30	mA	V _{PP} = V _{PPH} Programming in Progress
I _{PP3}	V _{PP} Erase Current	1, 2	N N	10	30	mA	V _{PP} = V _{PPH}
I _{PP4}	V _{PP} Program Verify Current	1, 2	N Y	2.0	5.0	mA	V _{PP} = V _{PPH} Program Verify ir Progress
I _{PP5}	V _{PP} Erase- Verify Current	1, 2	N	2.0	5.0	mA	V _{PP} = V _{PPH} Erase Verify in Progress



28F010/28F020

4.5 DC Characteristics—29F020—TTL/NMOS Compatible Commercial Products (Continued)

	I Mila	0_{M} ,		Limits		W.	Test Conditions
Symbol	Parameter	Notes	Min	Typ(3)	Max	Unit	
VIL	Input Low Voltage	.0	-0.5		0.8	V	1001. WITH
Viн	Input High Voltage	COL	2.0	N	V _{CC} + 0.5	V	W.100Y.COM.TW
Vol	Output Low Voltage		N1.T	W	0.45	V	V _{CC} = V _{CC} Min I _{OL} = 5.8 mA
V _{OH1}	Output High Voltage	V.C.	2.4	W		V	V _{CC} = V _{CC} Min I _{OH} = -2.5 m ²
V _{ID}	A ₉ Intelligent Identifier Voltage	NOY.C	11.50	TW	13.00	V	MM. TOOX.COM
I _{ID}	A ₉ Intelligent Identifier Current	1, 2	CO	90	200	μА	$A_9 = V_{ID}$
VPPL	V _{PP} during Read-Only Operations	V 100	0.00	M.T	6.5	V	NOTE: Erase/Program are Inhibited when V _{PP} = V _{PPL}
V _{PPH}	V _{PP} during Read/Write Operations	1N.10	11.40	OM.	12.60	٧	MMM.100X.C
V _{LKO}	V _{CC} Erase/Write Lock Voltage	$M_{T_{I}}$	2.5	CO_{M}	TV	٧	M.M. TOOX.

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... are COM.TW 1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, V_{PP} = 12.0 V, T = 25 °C. These currents are valid for all product versions (packages and speeds).

2. Not 100% tested: Characterization WWW.100Y.COM.TW

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3. "Typicals" are not guaranteed, but based on a limited number of samples from production lots. WWW.100 WWW.100Y.COM WWW.100Y.COM.

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DC Characteristics—28F010—CMOS Compatible Commercial Products 4.6

	WWW.100V.C	O_{Mr} .	- Kro-	Limits	- 411	M.	ON COM TW
Symbol		Notes	Min	Typ(3)	Max	Unit	Test Conditions
ILI	Input Leakage Current	COJ	V. T.	N	±1.0	μΑ	V _{CC} = V _{CC} Max V _{IN} ≈ V _{CC} or V _{SS}
ILO	Output Leakage Current	y.20	M.	V	±10	μА	V _{CC} = V _{CC} Max V _{OUT} = V _{CC} or V _{SS}
Iccs	V _{CC} Standby Current	01.C	OME.	50	100	μА	V _{CC} = V _{CC} Max CE# = V _{CC} ±0.2 V
lcc1	V _{CC} Active Read Current	0014	COJ	10	30	mA	V _{CC} = V _{CC} Max, CE# = V _{IL} f = 6 MHz, I _{OUT} = 0 mA
I _{CC2}	V _{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I _{CC3}	V _{CC} Erase Current	1, 2	Y.O.	5.0	15	mA	Erasure in Progress
Icc4	V _{CC} Program Verify Current	1, 2	OY.C	5.0	15	mA	V _{PP} = V _{PPH} Program Verify in Progress
ICC5	V _{CC} Erase Verify Current	1, 2	00 x ·	5.0	15	mA	V _{PP} = V _{PPH} Erase Verify in Progress
IPPS	V _{PP} Leakage Current	111	100	7 CO	±10	μA	V _{PP} ≤ V _{CC}
IPP1	V _{PP} Read Current, ID Current or Standby Current	MN	N.10	90	200	μА	V _{PP} > V _{CC}
	WIL	MAN	1	001.	±10	TV	V _{PP} ≤ V _{CC}
IPP2	V _{PP} Programming Current	1, 2		8.0	30	mA	V _{PP} > = V _{PPh} Programming in Progress
I _{PP3}	V _{PP} Erase Current	1, 2		6.0	30	mA	V _{PP} = V _{PPH} Erasure in Progress
IPP4	V _{PP} Program Verify Current	1, 2	WW	2.0	5.0	mA	V _{PP} = V _{PPH} Program Verify in Progress
I _{PP5}	V _{PP} Erase Verify Current	1, 2		2.0	5.0	mA	V _{PP} = V _{PPH} Erase Verify in Progress
VIL	Input Low Voltage		-0.5	M. L.	0.8	V	MIN N
ViH	Input High Voltage	V	0.7 V _{CC}		V _{CC} + 0.5	V	OM.TW
Vol	Output Low Voltage	N			0.45	V	V _{CC} = V _{CC} Min I _{OL} = 5.8 mA
V _{OH1}	Output High Voltage	LM.	0.85 V _{CC}	W	NW.	V	V _{CC} = V _{CC} Min I _{OH} = -2.5 mA
V _{OH2}	WW.IOV.CON		V _{CC} - 0.4			1.10°	V _{CC} = V _{CC} Min I _{OH} = -100 μA



28F010/28F020

DC Characteristics—28F010—CMOS Compatible 4.6 Commercial Products (Continued)

	TWW.In	CO_{MT} .		Limits	411	W.	CON CONTRACTOR
Symbol	Parameter	Notes	Min	Typ(3)	Max	Unit	Test Conditions
V _{ID}	A ₉ Intelligent Identifier Voltage		11.50	X	13.00	٧	N.1001.COM.TV
liD	A ₉ Intelligent Identifier Current	1, 2	M.I	90	200	μА	A ₉ = V _{ID}
VPPL	V _{PP} during Read-Only Operations	OOY.C	0.00	IVI	6.5	V	NOTE: Erase/Programs are Inhibited when V _{PP} = V _{PPL}
VPPH	V _{PP} during Read/Write Operations	100X.	11.40	T.T.	12.60	V	M. 1007.CO
V _{LKO}	V _{CC} Erase/Write Lock Voltage	1700.7	2.5	W		٧	MMM.100 F.CC

NUTES: Refer to Section 4.4. WWW.10074.7 DC Characteristics—28F020—CMOS Compatible **Commercial Products**

	M. P.	Wire	$In_{n_{-}}$	Limits	Mir	1	M.Inc.
Symbol	Parameter	Notes	Min	Typ(3)	Max	Unit	Test Conditions
עע	Input Leakage Current		N.10	JY.C	±1.0	μΑ	V _{CC} = V _{CC} Max V _{IN} = V _{CC} or V _{SS}
LO	Output Leakage Current	1	VW.1	001/ 001	±10	μА	V _{CC} = V _{CC} Max V _{OUT} = V _{CC} or V _{SS}
ccs	V _{CC} Standby Current	1 W	WW	50	100	μА	V _{CC} = V _{CC} Max CE# = V _{CC} ±0.2 V
lcc ₁	V _{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$ Max CE# = V_{IL} f = 6 MHz, $I_{OUT} = 0$ mA
lcc2	V _{CC} Programming Current	1, 2	W	1.0	10	mA	Programming in Progress
lcc3	V _{CC} Erase Current	1, 2	W	5.0	15	mA	Erasure in Progress
CC4	V _{CC} Program Verify Current	1, 2		5.0	15	mA	V _{PP} = V _{PPH} Program Verify in Progress
CC5	V _{CC} Erase Verify Current	1, 2		5.0	15	mA	V _{PP} = V _{PPH} Erase Verify in Progress
IPPS -	V _{PP} Leakage Current = -	1			±10_	μΑ	V _{PP} ≤ V _{CC}

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28F010/28F020

DC Characteristics—28F020—CMOS Compatible 4.7 Commercial Products (Continued)

ı	W. Too	OD_{IV}	-8.8	Limits		W.	COM
Symbol	Parameter	Notes	Min	Typ(3)	Max	Unit	Test Conditions
IPP1	V _{PP} Read Current, ID Current or Standby Current	COV	T.T.	90 N	200	μА	V _{PP} > V _{CC}
-XXI	MW.In	J.CO	Mr.	N	±10	WW	V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Programming Current	1, 2	$\mathcal{D}_{\mathbf{M}}$	8	30	mA	V _{PP} = V _{PPH} Programming in Progress
l _{PP3}	V _{PP} Erase Current	1, 2	$\hat{O}_{D_{A}}$	10	30	mA	V _{PP} = V _{PPH} Erasure in Progress
I _{PP4}	V _{PP} Program Verify Current	1, 2	, CO	2.0	5.0	mA	V _{PP} = V _{PPH} Program Verify ir Progress
I _{PP5}	V _{PP} Erase Verify Current	1, 2	Y.C	2.0	5.0	mA	V _{PP} = V _{PPH} Erase Verify in Progress
VIL	Input Low Voltage	11.10	-0.5	O_{Mr}	0.8	V	WWW. TOW.C
ViH	Input High Voltage	W.1	0.7 V _C C	$CO_{\overline{D}}$	V _{CC} + 0.5	V	WWW.100Y.
V _{OL}	Output Low Voltage	WW.	100	I.CO	0.45	V	V _{CC} = V _{CC} Min I _{OL} = 5.8 mA
Vон1	Output High Voltage		0.85 V _{CC}	Y.C	OM:	٧	V _{CC} = V _{CC} Min I _{OH} = -2.5 mA
V _{OH2}	CON.TW		V _C C - 0.4	001.	$CO_{\overline{N}}$	TV	V _{CC} = V _{CC} Min I _{OH} = -100 µA
ViD	A ₉ Intelligent Identifier Voltage	W	11.5 0	100	13.00	٧	M MMM.
liD	A ₉ Intelligent Identifier Current	1, 2		90	200	μА	A ₉ = V _{ID}
V _{PPL}	V _{PP} during Read-Only Operations		0.00	W.1	6.5	VO	NOTE: Erase/Programs are Inhibited when V _{PP} = V _{PPL}
V _{PPH}	V _{PP} during Read/Write Operations		11.4 0	WW.	12.60	.Vo	M. TW WY
VLKO	V _{CC} Erase/Write Lock Voltage	1	2.5	W	.100	V	ON TW

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4.8 DC Characteristics—28F010—TTL/NMOS Compatible **Extended Temperature Products**

	MW.100 C	$O_{J/J}$.	-	Limits		W	TOON.COM.
Symbol		Notes	Min	Typ(3)	Max	Unit	Test Conditions
ll:	Input Leakage Current	CO	T.T.	MI.	±1.0	μA	V _{CC} = V _{CC} Max V _{IN} = V _{CC} or V _{SS}
lo	Output Leakage Current	1.00	$M_{i,I}$		±10	μΑ	V _{CC} = V _{CC} Max V _{OUT} = V _{CC} or V _{SS}
lccs	V _{CC} Standby Current	01.C	O_{MT}	0.3	1.0	mA	V _{CC} = V _{CC} Max CE# = V _{IH}
lcc1	V _{CC} Active Read Current	00N.		10	30	mA	V _{CC} = V _{CC} Max, CE# ≈ V _{II} f = 6 MHz, I _{OUT} ≈ 0 mA
lcc2	V _{CC} Programming Current	1, 2		1.0	30	mA	Programming in Progress
Іссз	V _{CC} Erase Current	1, 2	N.C.	5.0	30	mA	Erasure in Progress
Icc4	Vcc Program Verify Current	1, 2	OY.C	5.0	30	mA	V _{PP} = V _{PPH} Program Verify in Progres
I _{CC5}	V _{CC} Erase Verify Current	1, 2	007	5.0	30	mA	V _{PP} = V _{PPH} Erase Verify in Progress
I _{PPS}	V _{PP} Leakage Current	10	700.	, c0	±10	μА	V _{PP} ≤ V _{CC}
I _{PP1}	V _{PP} Read Current or Standby Current	1	1.100	90	200	μА	V _{PP} > V _{CC}
00 7.	OM.I.	1 N	N.10	3 7 (±10.0		V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Programming Current	1, 2	W.	8.0	30	mA	V _{PP} = V _{PPH} Programming in Progress
I _{PP3}	V _{PP} Erase Current	1, 2	7	6.0	30	mA	V _{PP} = V _{PPH} Erasure in Progress
I _{PP4}	V _{PP} Program Verify Current	1, 2		2.0	5.0	mA	V _{PP} = V _{PPH} Program Verify in Progres
I _{PP5}	V _{PP} Erase Verify Current	1, 2		2.0	5.0	mA	V _{PP} = V _{PPH} Erase Verify in Progress
VIL	Input Low Voltage	L	-0.5	WW	0.8	V	M
V _{IH}	Input High Voltage	N	2.0	UWV	V _{CC} + 0.5	٧	OW.I.A.
VoL	Output Low Voltage	N		WW	0.45	Ŋ.	Vcc ≈ Vcc Min I _{OL} = 5.8 mA
V _{OH1}	Output High Voltage	TM	2.4 	W	144. 144.	0/2	V _{CC} ≈ V _{CC} Min I _{OH} = –2.5 mA
V _{ID}	A ₉ Intelligent Identifier Voltage	T	11.50	N.	13.00	JV)(J.COM.TW

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4.8 DC Characteristics—28F010—TTL/NMOS Compatible Extended Temperature Products (Continued)

	1111.100	$0M_{TT}$		Limits		M.7	COM
Symbol	Parameter	Notes	Min	Typ(3)	Max	Unit	Test Conditions
lio	A ₉ Intelligent Identifier Current	1, 2	TW	90	500	μА	$A_9 = V_{ID}$
V _{PPL}	V _{PP} during Read-Only Operations	CO	0.00	Z	6.5	V	NOTE: Erase/Program are Inhibited when V _{PP} = V _{PPL}
V _{PPH}	V _{PP} during Read/Write Operations	OY.CC	11.40	V	12.60	٧	W. 100Y. CONT.
V _{LKO}	V _{CC} Erase/Write Lock Voltage	gov.C	2.5	TW		٧	WANTOON COM

NOTES:

Refer to Section 4.4.





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4.9 DC Characteristics—28F020—TTL/NMOS Compatible **Extended Temperature Products**

Symbol	Parameter	Notes	Min	Limits Typ ⁽³⁾	Max	Unit	Test Conditions
I _{LI}	Input Leakage Current	1	(TV	k1	±1.0	μА	V _{CC} = V _{CC} Max V _{IN} = V _{CC} or V _{SS}
I _{LO}	Output Leakage Current	, <u>c</u> o	W.I	W.	±10	μА	V _{CC} = V _{CC} Max V _{OUT} = V _{CC} or V _{SS}
lccs	V _{CC} Standby Current	N.C		0.3	1.0	mA	V _{CC} = V _{CC} Max CE# = V _{IH}
lcc1	V _{CC} Active Read Current	01.4 001	CO_J	10	30	mA	V _{CC} = V _{CC} Max CE# = V _{IL} f = 6 MHz I _{OUT} = 0 mA
I _{CC2}	V _{CC} Programming Current	1, 2	1.CO	1.0	30	mA	Programming in Progress
I _{CC3}	V _{CC} Erase Current	1, 2	-7 C	5.0	30	mA	Erasure in Progress
Icc4	V _{CC} Program Verify Current	1, 2	V. (5.0	30	mA	V _{PP} = V _{PPH} Program Verify in Progress
Iccs	V _{CC} Erase Verify Current	1, 2	OON	5.0	30	mA	V _{PP} = V _{PPH} Erase Verify in Progress
IPPS	V _{PP} Leakage Current	NA.	400	('Co	±10	μА	V _{PP} ≤ V _{CC}
I _{PP1}	V _{PP} Read Current, ID Current or Standby Current		N.10	90	200	μА	VPP > VCC
100x	COMITY	7.7	W.1	JU -	±10		V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Programming Current	1, 2	NW.	8	30	mA	V _{PP} = V _{PPH} Programming in Progress
I _{PP3}	V _{PP} Erase Current	1, 2	WV	10	30	mA	V _{PP} = V _{PPH}
IPP4	V _{PP} Program Verify Current	1, 2	WW	2.0	5.0	mA	V _{PP} = V _{PPH} Program Verify ir Progress

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DC Characteristics—TTL/NMOS Compatible 4.9 **Extended Temperature Products (Continued)**

Symbol	Parameter	Notes	Min	Limits Typ ⁽³⁾	Max	Unit	Test Conditions
I _{PP5}	V _{PP} Erase Verify Current	1, 2	LTV	2.0	5.0	mA	V _{PP} = V _{PPH} Erase Verify in Progress
VIL	Input Low Voltage		-0.5	1	0.8	V	W.100 COM
V _{IH}	Input High Voltage	y.C	2.0		V _{CC} + 0.5	٧	MM.1007.COJ
V _{OL}	Output Low Voltage	ooy.	COM	VT	0.45	٧	$V_{CC} = V_{CC}$ Min $I_{OH} = -2.5$ mA
V _{OH1}	Output High Voltage	1007	2.4	M.T	N	٧	$V_{CC} = V_{CC}$ Min $I_{OL} \approx 5.8$ mA
V _{ID}	A _g Intelligent Identifier Voltage	V.100	11.50	JM.	13.00	٧	WW.100x.
الم الم	A ₉ Intelligent Identifier Current	1, 2	ooy.	90	500	μA	$A_9 = V_{ID}$
V _{PPL}	V _{PP} during Read-Only Operations	NW.	0.00	$CO_{\bar{b}}$	6.5	V	NOTE: Erase/Program a Inhibited when V _{PP} = V _P
V _{PPH}	V _{PP} during Read/Write Operations	WY	11.40	I.C	12.60	V	MW.T
V _{LKO}	V _{CC} Erase/Write Lock Voltage	NY	2.5		MO	V	WWW.

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DC Characteristics—28F010—CMOS Compatible 4.10 **Extended Temperature Products**

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	MAM. Jook. C	O_{MT} .	- - 11	Limits	_ 4	VV	TOOX.COM.
Symbol	Parameter	Notes	Min	Typ(3)	Max	Unit	Test Conditions Vcc = Vcc Max
lu	Input Leakage Current	c0	1.1	XI	±1.0	μА	V _{IN} = V _{CC} or V _{SS}
ILO	Output Leakage Current	y.20	M		±10	μА	V _{CC} = V _{CC} Max V _{OUT} = V _{CC} or V _{SS}
Iccs	V _{CC} Standby Current	01.C		50	100	μА	Vcc = Vcc Max CE# = Vcc ±0.2 V
lcc1	V _{CC} Active Read Current	001	CO^{3}	10	30	mA	V _{CC} = V _{CC} Max, CE# = V _{IL} f = 10 MHz, I _{OUT} = 0 mA
lcc2	V _{CC} Programming Current	1, 2	. (1.0	10	mA	Programming in Progress
Іссз	V _{CC} Erase Current	1, 2	Y.C.	5.0	30	mA	Erasure in Progress
lcc4	Vcc Program Verify Current	1, 2	O.Y.C	5.0	30	mA	V _{PP} = V _{PPH} Program Verify in Progress
lccs	V _{CC} Erase Verify Current	1, 2	001	5.0	30	mA	V _{PP} = V _{PPH} Erase Verify in Progress
IPPS	V _{PP} Leakage Current	111	700	a CC	±10	μА	V _{PP} ≤ V _{CC}
IPP1	V _{PP} Read Current, ID Current or Standby Current	NN	V.100	90	200	μА	VPP > VCC
MON!	CONTRACTOR	WW	11	001	±10		V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Programming Current	1, 2		8.0	30	mA	V _{PP} = V _{PPH} Programming in Progress
Іррз	V _{PP} Erase Current	1, 2		6.0	30	mA	V _{PP} = V _{PPH} Erasure in Progress
I _{PP4}	V _{PP} Program Verify Current	1, 2	W	2.0	5.0	mA	V _{PP} = V _{PPH} Program Verify in Progress
I _{PP5}	V _{PP} Erase Verify Current	1, 2	V	2.0	5.0	mA	V _{PP} ≈ V _{PPH} Erase Verify in Progress
VIL	Input Low Voltage		-0.5		0.8	V	WIN.
ViH	Input High Voltage	N	0.7 V _{CC}	WW	V _{CC} + 0.5	٧	OM.TW
Vol	Output Low Voltage			WW.	0.45	V	Vcc = Vcc Min I _{OL} = 5.8 mA
V _{OH1}	Output High Voltage	IN	0.85 V _{CC}	1/1	WW	V	V _{CC} = V _{CC} Min I _{OH} = -2.5 mA
V _{OH2}	AMM:100X'COV	1. 1. Y	Vcc - 0.4		WW	41 10	V _{CC} = V _{CC} Min I _{OH} = -100 μA

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DC Characteristics—28F010—CMOS Compatible 4.10 **Extended Temperature Products (Continued)**

	W. Ju	Q_{N_I}	1	Limits	لتيب	NW	COM
Symbol	Parameter	Notes	Min	Typ(3)	Max	Unit	Test Conditions
V _{ID}	A ₉ Intelligent Identifier Voltage	Y CO	11.50	\ .ss1	13.00	V	W.100X.COM.TV
liD	A ₉ Intelligent Identifier Current	1, 2	MI	90	500	μА	$A_9 = V_{ID}$
V _{PPL}	V _{PP} during Read-Only Operations	NOY.C	0.00	TW	6.5	٧	NOTE: Erase/Programs are Inhibited when V _{PP} = V _{PPL}
V _{PPH}	V _{PP} during Read/Write Operations	TOON	11.40	T.IV	12.60	V	NAM TOOK COL
VLKO	V _{CC} Erase/Write Lock Voltage	100	2.5	M.T	W	٧	MANN TOO T. CC

WWW.100 4.11 DC Characteristics—28F020—CMOS Compatible **Extended Temperature Products**

N.C	W. A.	MV		Limits):	W	WWW
Symbol	Parameter	Notes	Min	Typ ⁽³⁾	Max	Unit	Test Conditions
lu .	Input Leakage Current	1	W.1	00X	±1.0	μА	V _{CC} = V _{CC} Max V _{IN} = V _{CC} or V _{SS}
ILO	Output Leakage Current	1 _W	NN.	1001	±10	μА	V _{CC} = V _{CC} Max V _{OUT} = V _{CC} or V _{SS}
lccs	V _{CC} Standby Current	1		50	100	μА	V _{CC} = V _{CC} Max CE# = V _{CC} ±0.2 V
lcc1	V _{CC} Active Read Current	1	WA	10	50	mA	V _{CC} = V _{CC} Max CE# = V _{IL} f = 6 MHz I _{OUT} = 0 mA
lcc2	V _{CC} Programming Current	1, 2	W	1.0	10	mA	Programming in Progress
Іссз	V _{CC} Erase Current	1, 2		5.0	30	mA	Erasure in Progress
Icc4	V _{CC} Program- Verify Current	1, 2		5.0	30	mA	V _{PP} = V _{PPH} Program Verify ir Progress



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DC Characteristics—28F020—CMOS Compatible Extended Temperature Products (Continued) 4.11

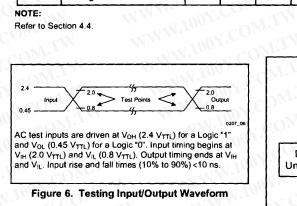
Symbol	Parameter	Notes	Min	Limits Typ ⁽³⁾	Max	Unit	Test Conditions
lccs	V _{CC} Erase Verify Current	1, 2	1.TV	5.0	30	mA	V _{PP} = V _{PPH} Erase Verify in Progress
IPPS	V _{PP} Leakage Current	1	MI	N	±10	μA	V _{PP} ≤ V _{CC}
l _{PP1}	V _{PP} Read Current, ID Current or Standby Current	07.C	OM:	90	200	μА	VPP > VCC
T	MMM	OOY.	Co_{k_0}	VT	±10		V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Programming Current	1, 2	CO	8	30	mA	V _{PP} = V _{PPH} Programming in Progress
I _{PP3}	V _{PP} Erase Current	1, 2	N.C	10	30	mA	V _{PP} = V _{PPH} Erasure in Progress
I _{PP4}	V _{PP} Program Verify Current	1, 2	01.	2.0	5.0	mA	V _{PP} = V _{PPH} Program Verify in Progress
I _{PP5}	V _{PP} Erase Verify Current	1, 2	1002	2.0	5.0	mA	V _{PP} = V _{PPH} Erase Verify in Progress
VIL	Input Low Voltage	MA	-0.5	Y.CC	0.8	V	100
ViH	Input High Voltage	NW	0.7 Vcc	OY.C	V _{CC} + 0.5	V	WWW.10
V _{OL}	Output Low Voltage	WW	VVI.	001	0.45	٧	V _{CC} = V _{CC} Min I _{OL} = 5.8 mA
V _{OH1}	Output High Voltage	W	0.85 Vcc	700 s	V.CO	V	V _{CC} = V _{CC} Min I _{OH} = -2.5 mA
V _{OH2}	oy.com.tv		V _{CC} - 0.4	V.100	oy.C	DIV	V _{CC} = V _{CC} Min I _{OH} = -100 µA
V _{ID}	A ₉ Intelligent Identifier Voltage		11.50	W.	13.00	٧	TIN WW
I _{ID}	A ₉ Intelligent Identifier Current	1, 2	W	90	500	μА	A ₉ = V _{ID}

28F010/28F020

DC Characteristics—28F020—CMOS Compatible 4.11 **Extended Temperature Products (Continued)**

]	W.100	COM.	A	Limits		VW	In COMP.
Symbol	Parameter	Notes	Min	Typ ⁽³⁾	Max	Unit	Test Conditions
V _{PPL}	V _{PP} during Read-Only Operations	1 CO	0.00		6.5	٧	NOTE: Erase/Programs are Inhibited when V _{PP} = V _{PPL}
V _{PPH}	V _{PP} during Read/Write Operations	o V.C	11.40		12.60	٧	1M.100 Y.COM.1
VLKO	V _{CC} Erase/Write Lock Voltage	OY.C	2.5	WT		V	M.M. T. 100 Y. COM

NOTE:



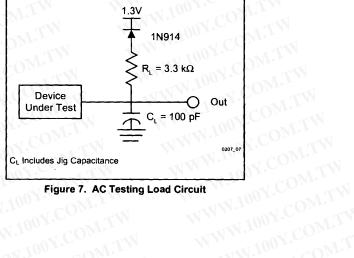


Figure 7. AC Testing Load Circuit



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4.12 AC Characteristics—28F010—Read-Only Operations Commercial and Extended Temperature Products

	Versions		28F01	0-90(1)	28F01	0-120(1)	28F01	0-150(1)	
Symbol	Characteristic	Notes	Min	Max	Min	Max	Min	Max	Un
tavav/tRC	Read Cycle Time	LIT	90		120	- 10	150		ns
tELQV/tCE	CE# Access Time	DIA.	W	90	WW	120	ov.	150	ns
tavav/tacc	Address Access Time	O_{Mr}	-NN	90		120	V	150	ns
tGLQV/tOE	OE# Access Time	MON	. 1	35		50	Inc	55	ns
tELOX/tLZ	CE# to Low Z	2, 3	0		0	-111	0	- c(ns
t _{EHQZ}	Chip Disable to Output in High Z	2	M.T	45		55	N.10	55	ns
tGLQX/tOLZ	OE# to Output in Low Z	2, 3	0		0	V1	0	JV -	ns
tghqz/tdf	Output Disable to Output in High Z	2	MOS	30		30	WW	35	ns
toн	Output Hold from Address, CE#, or OE# Change	2, 4	.C0)	1.1 11 T	0		0	1100	ns
twhGL	Write Recovery Time before Read	100	6	M.	6		6	W	μs

NOTES:

- 1. See AC Input/Output Waveform and AC Testing Load Circuit for testing characteristics.
- 2. Sampled, not 100% tested.

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- 3. Guaranteed by design.
- 4. Whichever occurs first.

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AC Characteristics—28F020—Read Only Operations 4.13 Commercial and Extended Temperature Products

	Versions	7	28F02	(0-90(4)	28F02	0-120(4)	28F02	0-150(4)	
Symbol	Characteristics	Notes	Min	Max	Min	Max	Min	Max	U
t _{AVAV} /t _{RC}	Read Cycle Time	1	90		120	-311	150		n
t _{ELQV} /t _{CE} >	Chip Enable Access Time	Ω_{h_2}	TW	90	W	120	Your	150	n
tavov/tacc	Address Access Time	CO_{N_2}	-	90	41	120	7001	150	n
tGLQV/tOE	Output Enable Access Time	CO1	I'r.	35		50	Too	50	ns
t _{ELQx} /t _{LZ}	Chip Enable to Output in Low Z	2, 3	0	W	0	WW	0	oy.C	Ons
t _{EHQZ}	Chip Disable to Output in High Z	20	Σ_{Mr}	45		55	111.1	55	ns
tg.ax/to.z	Output Enable to Output in Low Z	2, 3	0	LTW	0	N	0	100	ns
tghqz/tdf	Output Disable to Output in High Z	2	.CO	30		30		30	ns
tон	Output Hold from Address, CE#, or OE# Change	1, 2	0	D_{M^*}	0		0	W.I	ns
twhgL	Write Recovery Time before Read	W.F	6	Oh	6		6	M MA	μs

NOTES:

- 1. Whichever occurs first.
- 2. Sampled, not 100% tested.
- 3. Guaranteed by design.
- WWW.100Y.COM.TW 4. See High Speed AC Testing Input/Output Waveform (Figure 8) and High Speed AC Testing Load Circuit (Figure 9) for WWW.100Y.COM.TW testing characteristics.
- 5. See Testing Input/Output Waveform (Figure 6) and AC Testing Load Circuit (Figure 7) for testing characteristics.

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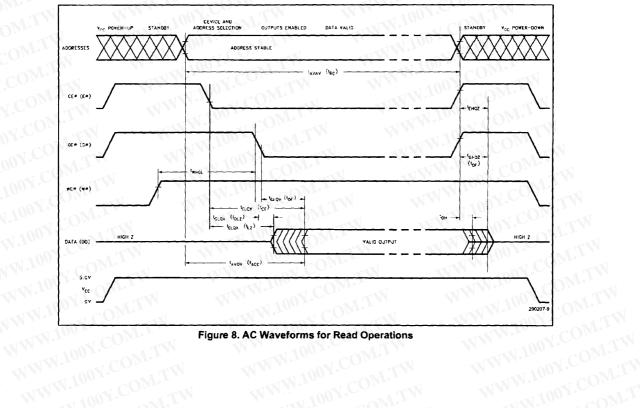


Figure 8. AC Waveforms for Read Operations WWW.100 WWW.100Y.COM.

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AC Characteristics—28F010—Write/Erase/Program Only Operations(1) 4.14 Commercial and Extended Temperature Products

	Versions		28F01	10-90(2)	28F01	0-120(2)	28F01	0-150(2)	- X
Symbol	Characteristic	Notes	Min	Max	Min	Max	Min	Max	Unit
tavav/twc	Write Cycle Time	LIT	90		120	-x110	150		ns
tavwl/tas	Address Set-Up Time) I v	0		0	1	0).		ns
twlax/tah	Address Hold Time	O_{Mr}	40		40	MM.	40	$C_{O_{L}}$	ns
TAN	M. 100 r.	3	55	1		WW	Inc	of CC	M.
t _{DVWH} /t _{DS}	Data Set-Up Time	601	40	- 7	40		40	- 0	ns
	WW 100		55	N		Mar	vi 10	01.	
twnox/ton	Data Hold Time	Y.C.	10	W	10	MM	10	001.	ns
twhgL	Write Recovery Time before Read	OY.C	6	TW	6	W	6	1007	μs
t _{GHWL}	Read Recovery Time before Write	047	0	I.TV	0	1	0	V.100	ns
telwi/tcs	Chip Enable Set-Up Time before Write	700	15	W.I	15		15	W.10	ns
twhEH/tcH	Chip Enable Hold Time	N.To.	0	O_{Mr}	0		0	(M.)	ns
twLWH/twp	Write Pulse Width	W.10	40	~OM	60		60	WW	ns
	M.TW	3	55		TIL			-311	1.10
twhwi/twph	Write Pulse Width High	- «1	20		20	N	20	NA	ns
twhwH1	Duration of Programming Operation	5	10	Y.CC	10	V	10	MM	μs
t _{WHWH2}	Duration of Erase Operation	5	9.5	OX:	9.5	IM	9.5	Z	ms
typel	V _{PP} Set-Up Time to Chip Enable Low	4	1	001	1	LTW	1	1	μs

NOTES:

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- 4. Guaranteed by design.
- The integrated stop timer terminates the programming/erase operations, thus eliminating the need for a maximum specification. WWW.100Y.COM.

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4.15 AC Characteristics—28F020—Write/Erase/Program Only Operations(1) **Commercial and Extended Temperature Products**

	Versions		28F02	20-90(4)	28F02	0-120(4)	28F02	0-150(4)	N
Symbol	Characteristics	Notes	Min	Max	Min	Max	Min	Max	Unit
tavav/ twc	Write Cycle Time		90		120	-110	150		ns
tavwl/ tas	Address Set-Up Time	Mr.	0		0	14.	0	O.	ns
twlax/tah	Address Hold Time	O_{MT} .	40		40	ΛM^{*}	40	$C_{O_{\overline{D}}}$	ns
TW	W. 100x.	5	55			WW	100	7 CO	M_{II}
tovwh/ tos	Data Set-Up Time		40		40	- 11	40		ns
WT	WWW	5	55	N	55	MAL	sī 10	N.C	
twhox/ toh	Data Hold Time	Y.CU	10	W	10	WW	10	NY.	ns
twigi	Write Recovery Time before Read	oy.C	6	TW	6	W	6	YOOY	μs
tGHWL	Read Recovery Time before Write	2/.	0	LTV	0	W	0	1.100	ns
telwi/tcs	Chip Enable Set-Up Time before Write	1007	15	M.T	15		15	N.10	ns
twhen/ tch	Chip Enable Hold Time	1.100	0	OM.	0		0	111.7	ns
twww/ twp	Write Pulse Width	CV.10	40	MO	60		60	WW.	ns
OOX.CO	W.TW WY	5	55		55			-111	
twhwi/	Write Pulse Width High	N V	20	0	20	N - × 1	20		ns
twhwh1	Duration of Programming Operation	3	10	₹.C'	10		10	WV	μs
twhwh2	Duration of Erase Operation	3	9.5	. ≤ 7 (9.5	E XXI	9.5	- T	ms
typel	V _{PP} Set-Up Time to Chip Enable Low	2	1.1	00A	COD		1	7	μs

NOTES:

- Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC 1. Characteristics for Read-Only Operations.
- Guaranteed by design.
- 3. The integrated stop timer terminates the programming/erase operations, thus eliminating the need for a maximum specification
- See Testing Input/Output Waveform (Figure 6) and AC Testing Load Circuit (Figure 7) for testing characteristics.
- Minimum Specification for Extended Temperature product.

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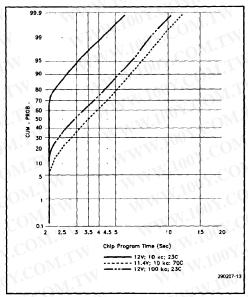


Figure 9. 28F010 Typical Programming Capability

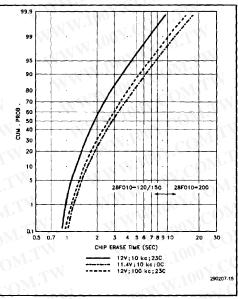


Figure 11. 28F010 Typical Erase Capability

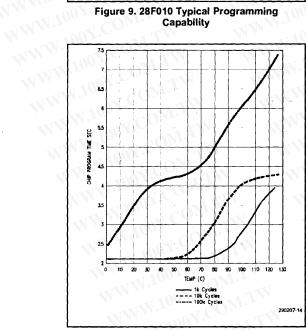


Figure 10. 28F010 Typical Program Time at 12 V

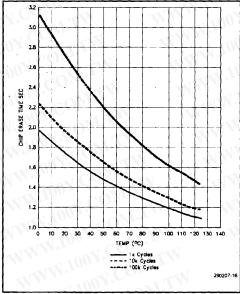


Figure 12. 28F010 Typical Erase Time at 12 V

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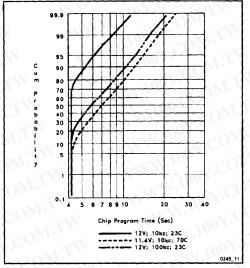


Figure 13. 28F020 Typical Programming Capability

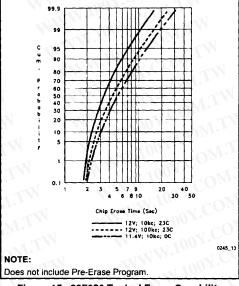


Figure 15. 28F020 Typical Erase Capability

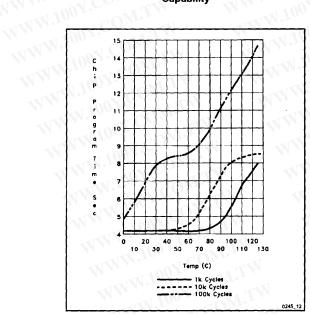


Figure 14. 28F020 Typical Program Time at 12 V

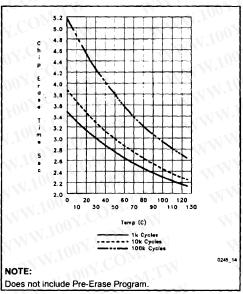


Figure 16. 28F020 Typical Erase Time at 12 V

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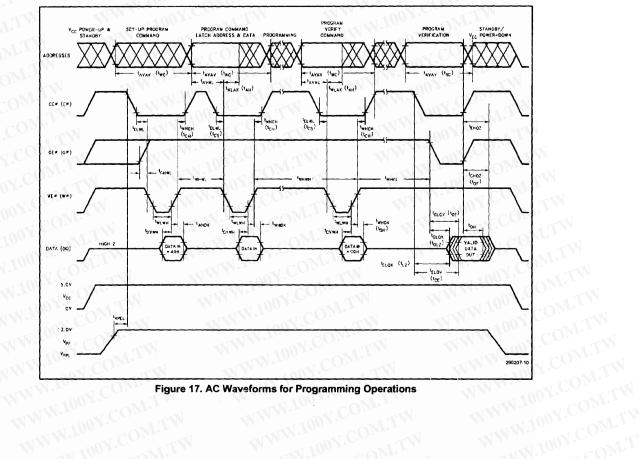
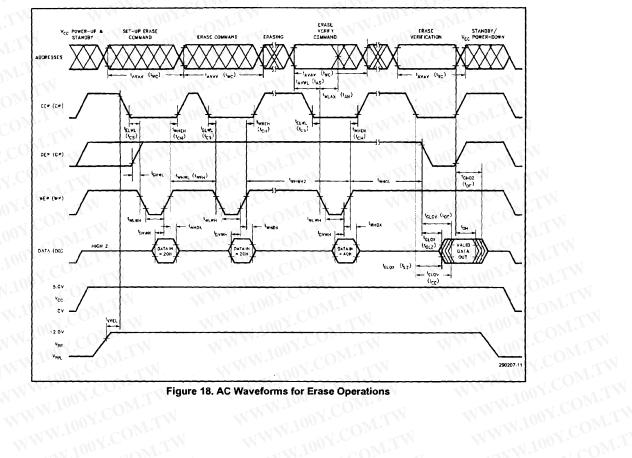


Figure 17. AC Waveforms for Programming Operations WWW.100Y.COM.



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AC Characteristics—28F010—Alternative CE#-Controlled Writes(1) 4.16 **Commercial and Extended Temperature**

N	Versions	100		0-90(2)		0-120(2)		0-150(2)	W
Symbol	Characteristic	Notes	Min	Max	Min	Max	Min	Max	Unit
tavav	Write Cycle Time	- 1	90	ļ	120	1	150		ns
tAVEL	Address Set-Up Time	$O_{P_{a_{a}}}$	0		0	N.	0	Co	ns
TELAX	Address Hold Time	CO_{N_I}	45		55		55	I.CO	ns
1.1.	W 1001	3	60	«1			The	<1 C	DM.
toveh	Data Set-Up Time		35	N.N.	45	W 1	45	Q Y	ns
TV	WWW	3	50	M	 	MA	- 11	2011.	
teHDX	Data Hold Time	MY.C	10	TW	10	W	10	1001	ns
tEHGL	Write Recovery Time before Read	00X.	6	LTV	6	V	6	1.100	μs
tghwL	Read Recovery Time before Write	4	0	M.T	0	1	0	N.10	ns
twiel	Write Enable Set-Up Time before Chip Enable	N.100	0	DM.	0		0	W.1	ns
tehwh	Write Enable Hold Time	M_{II}	0		0		0	WW.	ns
telen	Write Pulse Width	. W.	45	COL	70	r T	70	TAX V	ns
100 X.C	WILM.	3	60		M.T.	N		1	N.10
tehel	Write Pulse Width High	MA	20	V.C.	20	W	20	MA	ns
tenen1	Duration of Programming Operation	5	10	oy.C	10	TW	10	WV	μs
t _{EHEH2}	Duration of Erase Operation	5	9.5	00X	9.5	TW	9.5		ms
t _{VPEL}	V _{PP} Set-Up Time to Chip Enable Low	4	N Y	1001	CY	M.T	1	1	μs

NOTES:

- Read timing characteristics during read/write operations are the same as during read-only operations. Refer to ACCharacteristics for Read-Only Operations.
- See AC Input/Output Waveform and AC Testing Load Circuit for testing characteristics.
- Minimum specification for extended temperature product.
- Guaranteed by design.
- The integrated stop timer terminates the programming/erase operations, thus eliminating the need for a maximum specification. WWW.100Y.C WWW.100Y.COM.T



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AC Characteristics—28F020—Alternate CE# Controlled Writes⁽¹⁾ **Commercial and Extended Temperature Products**

	Versions		28F02	20-90(4)	28F02	0-120(4)	28F02	0-150(4)	αÑ
Symbol	Characteristics	Notes	Min	Max	Min	Max	Min	Max	Un
t _{AVAV}	Write Cycle Time	TIM	90		120	×x1 10	150	Mod	ns
taveL	Address Set-Up Time	DE T	0		0	1	0		ns
telax	Address Hold Time	$O_{M_{\mathbb{R}}}$	50		55	MAN	55	CO	ns
	WW.100 x	5	60		60	WW	70-	o CO	Mr.
toveh	Data Set-Up Time	CO1	40	-1	45	-7311	45	-1 C!	ns
	WW 100	5	50	NA.	50	N.	vV.10	Q.Y.	10
tenox	Data Hold Time	N.C.	10		10	MAI	10	001.	ns
t _{EHGL}	Write Recovery Time before Read	JOY.C	6	TW	6	W	6	100A	μs
tGHWL	Read Recovery Time before Write	2	0	1.17	0		0	1.100	ns
twiel	Write Enable Set-Up Time before Chip Enable	100	0	Wir	0		0	W.10	ns
tehwh	Write Enable Hold Time	N.To.	0	Olar.	0		0	111.	ns
teleh	Write Pulse Width	M.I.	50	COM	60		70	WW	ns
	OM.TW WY	5	60	COI	60	r T		TAN V	1.10
tehel	Write Pulse Width High		20		20	N	20	N	ns
t _{EHEH1}	Duration of Prog. Operation	3	10	Y.U.	10	W	10	MAA	μs
t _{EHEH2}	Duration of Erase Operation	3	9.5	N.C	9.5	TW	9.5	W	ms
typel	V _{PP} Set-Up Time to Chip Enable Low	2	111	001.	COL	TW	1	W	μs

NOTES:

- Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
- Guaranteed by design.
- 3. The integrated stop timer terminates the programming/erase operations, thus eliminating the need for a maximum specification.
- See Testing Input/Output Waveform (Figure 6) and AC Testing Load Circuit (Figure 7) for testing characteristics. WWW.100Y.CO
- Minimum specification for extended temperature product.

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MMM.100X.COW

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Erase and Programming Performance 4.18

Paramete	r Notes	Min	Тур	ical	М	Unit	
COW'I	W.100	- c0	28F010	28F020	28F010	28F020	
Chip Erase Tim	e 1, 3, 4	. c(1.1	2	10	30	Sec
Chip Program T	ime 1, 2, 4	17.0	2	4	12.5	25	Sec

NOTES:

- "Typicals" are not guaranteed, but based on samples from production lots. Data taken at 25 °C, 120 V Vpp.
- Minimum byte programming time excluding system overhead is 16 usec (10 usec program + 6 usec write recovery), while maximum is 400 µsec/byte (16 µsec x 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
- Excludes 00H programming prior to erasure
- Excludes system level overhead.

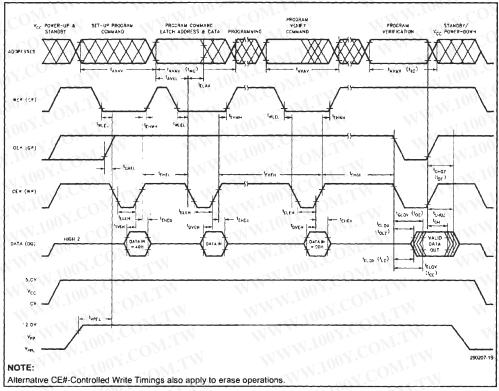
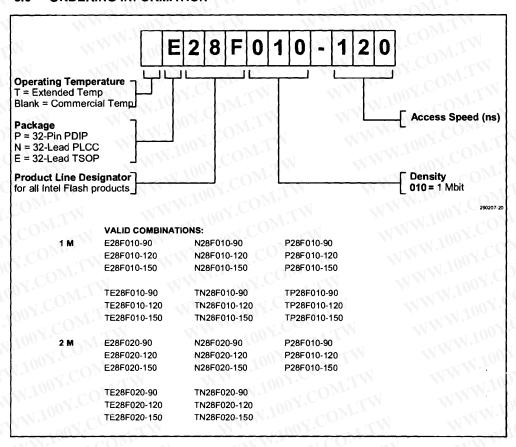


Figure 19. Alternate AC Waveforms for Programming Operations WW.100Y.COM.TW



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5.0 ORDERING INFORMATION



6.0 ADDITIONAL INFORMATION

Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.