

MOS FIELD EFFECT POWER TRANSISTOR
2SK1499/2SK1500

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

勝特力材料 886-3-5753170
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[Http://www.100y.com.tw](http://www.100y.com.tw)

DESCRIPTION

The 2SK1499/2SK1500 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 0.25 \Omega / 0.27 \Omega$ ($V_{GS} = 10 V, I_D = 13 A$)
- Low C_{iss} $C_{iss} = 3\ 300\ pF$ TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

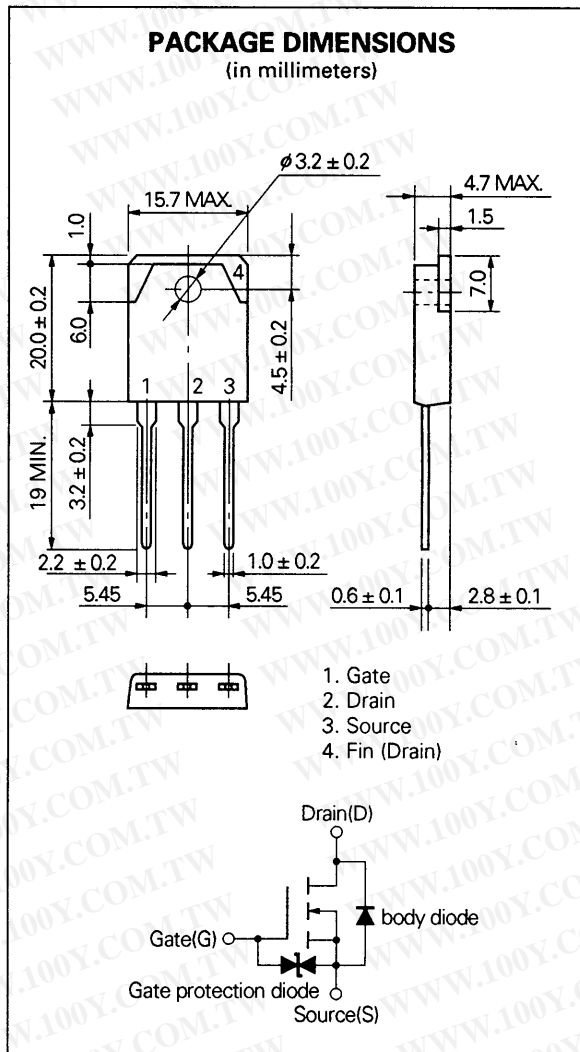
Standard
 Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25\ ^\circ C$)

Drain to Source Voltage	V_{DSS}	450/500	V
(2SK1499/2SK1500)			
Gate to Source Voltage	V_{GSS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 25	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 100	A
Total Power Dissipation ($T_c = 25\ ^\circ C$)	P_T	160	W
Channel Temperature	T_{ch}	150	$^\circ C$
Storage Temperature	T_{stg}	-55 to +150	$^\circ C$
Single Avalanche Current	I_{AS}^{**}	37.5	A
Single Avalanche Energy	E_{AS}^{**}	907	mJ

* $PW \leq 10\ \mu s$, Duty Cycle $\leq 2\ %$
 ** Starting $T_{ch} = 25\ ^\circ C$, $R_G = 25\ \Omega$, $V_{GS} = 20\ V \rightarrow 0$

PACKAGE DIMENSIONS
 (in millimeters)

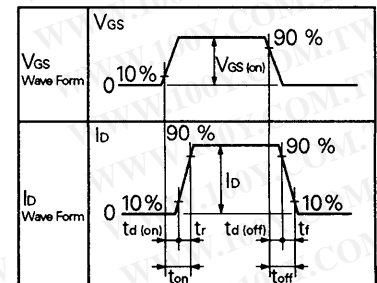
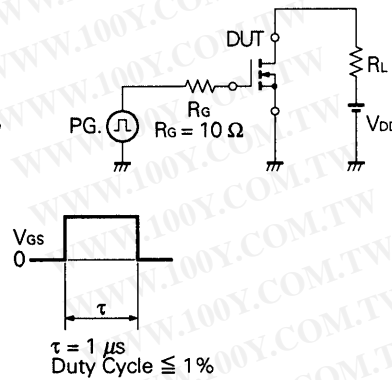
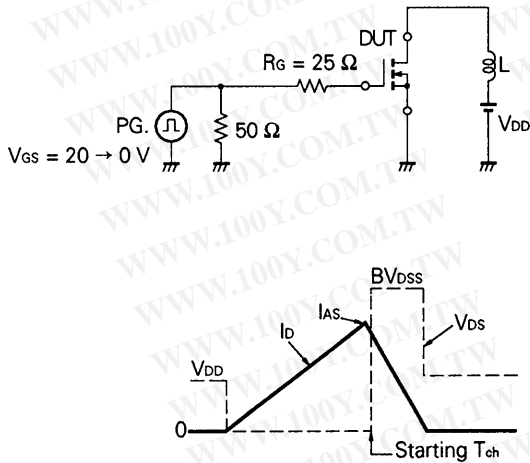


ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

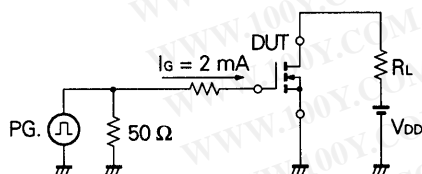
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance (2SK1499)	R _{DS(on)}		0.20	0.25	Ω	V _{GS} = 10 V, I _D = 13 A
Drain to Source On-state Resistance (2SK1500)	R _{DS(on)}		0.22	0.27	Ω	
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	8.0			S	V _{DS} = 10 V, I _D = 13 A
Drain Leakage Current (2SK1499)	I _{DSS}			100	μA	V _{DS} = 450 V, V _{GS} = 0
Drain Leakage Current (2SK1500)	I _{DSS}			100	μA	V _{DS} = 500 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		3 300		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		1 100		pF	
Reverse Transfer Capacitance	C _{rss}		480		pF	
Turn-On Delay Time	t _{d(on)}		50		ns	V _{GS} = 10 V V _{DD} = 150 V I _D = 13 A, R _G = 10 Ω R _L = 11.5 Ω
Rise Time	t _r		130		ns	
Turn-Off Delay Time	t _{d(off)}		180		ns	
Fall Time	t _f		70		ns	
Total Gate Charge	Q _G		115		nC	
Gate to Source Charge	Q _{GS}		20		nC	V _{GS} = 10 V I _D = 25 A V _{DD} = 400 V
Gate to Drain Charge	Q _{GD}		70		nC	
Diode Forward Voltage	V _{FI(S-D)}		1.0		V	I _D = 25 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		670		ns	I _D = 25 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		7.0		μC	di/dt = 50 A/μs

Test Circuit 1: Avalanche Capability

Test Circuit 2: Switching Time

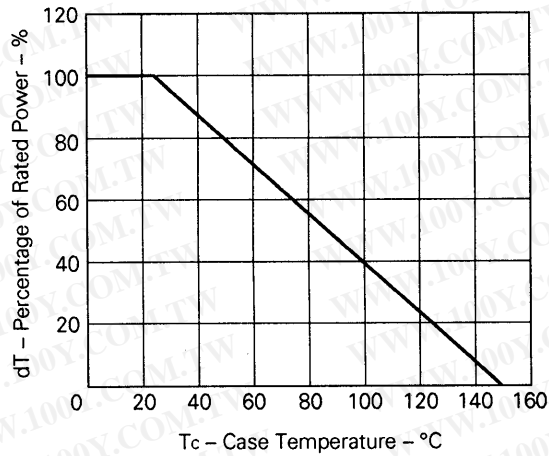


Test Circuit 3: Gate Charge

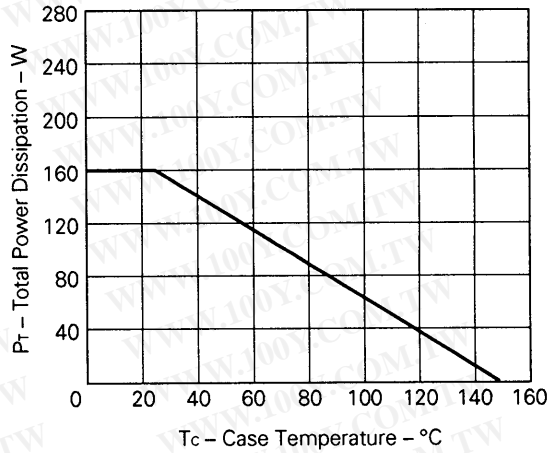


TYPICAL CHARACTERISTICS (T_a = 25 °C)

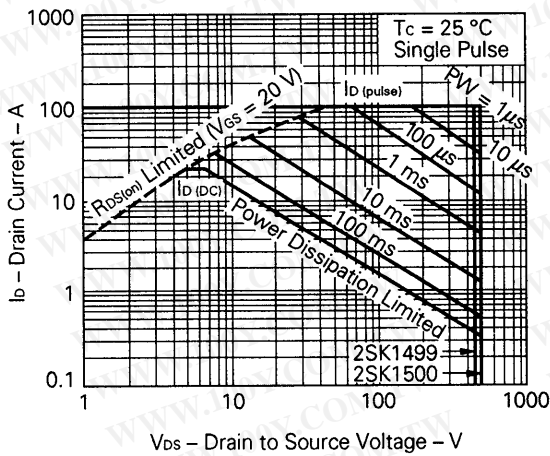
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



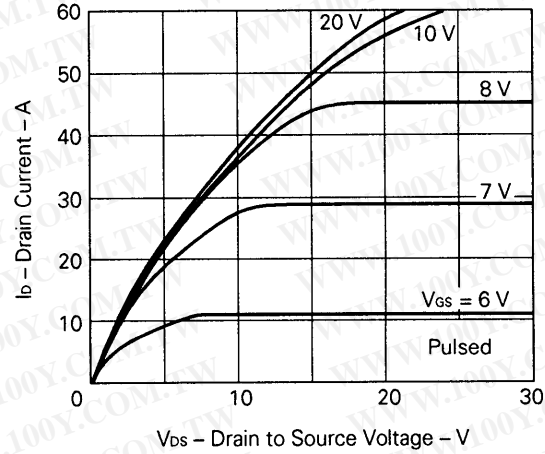
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



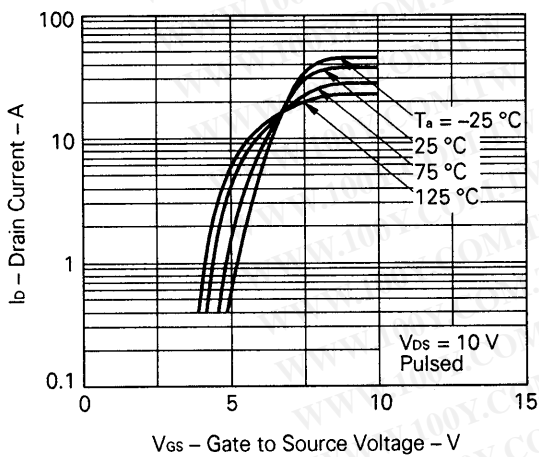
FORWARD BIAS SAFE OPERATING AREA



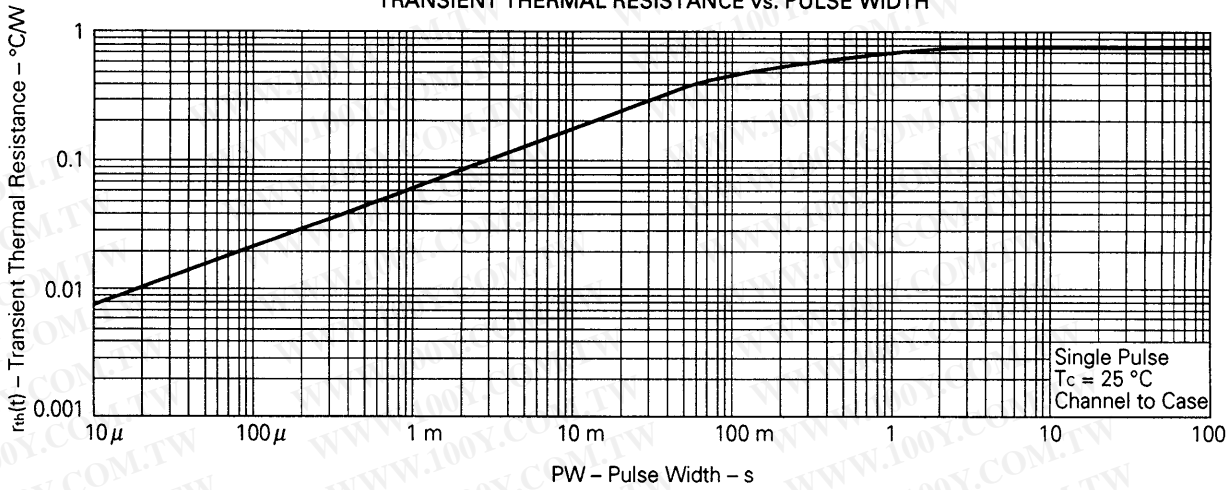
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



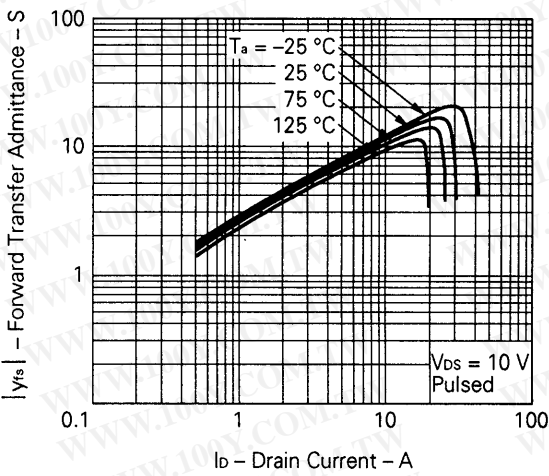
TRANSFER CHARACTERISTICS



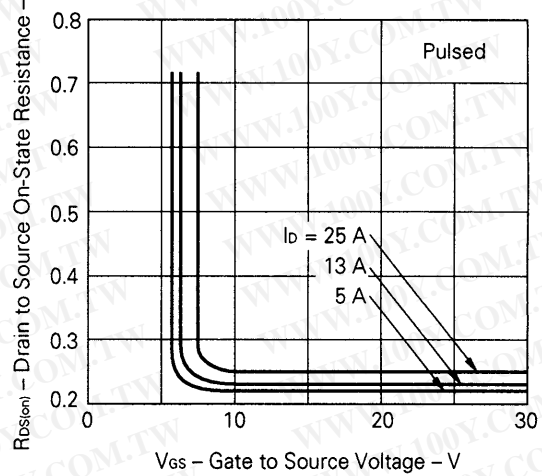
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



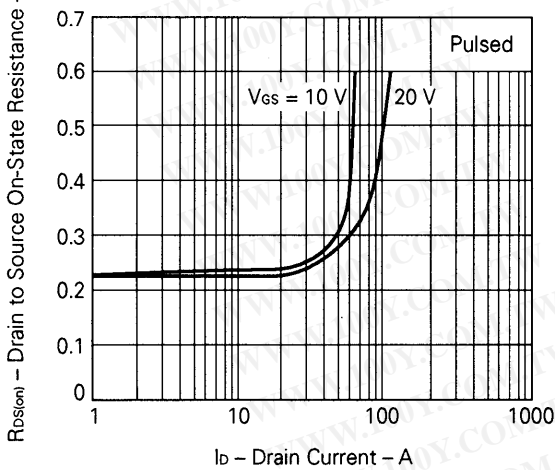
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



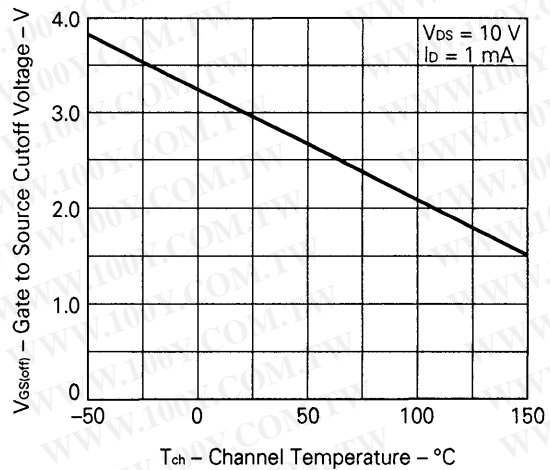
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



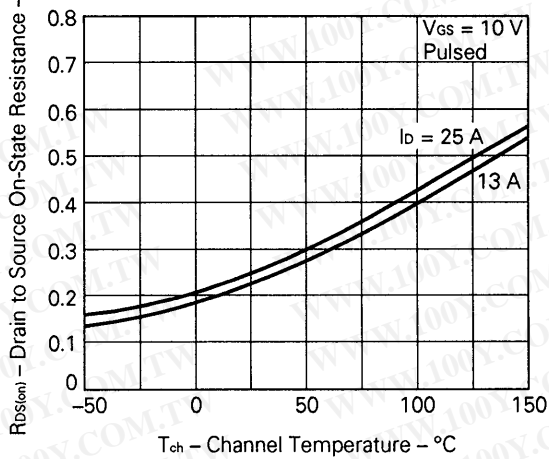
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



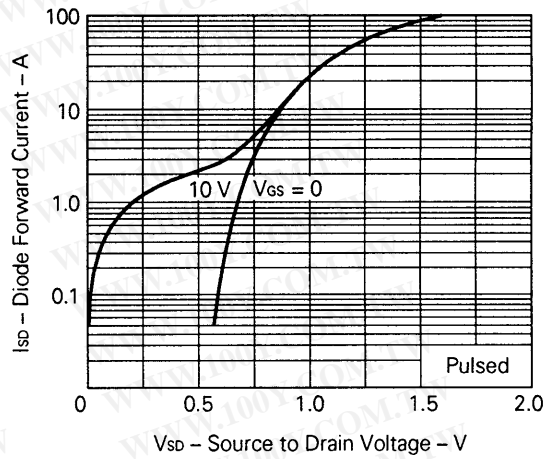
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



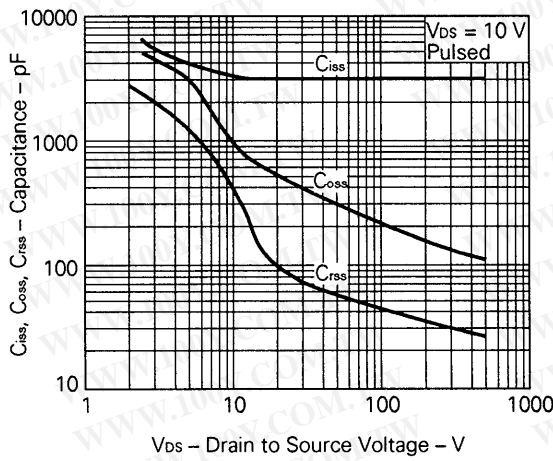
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



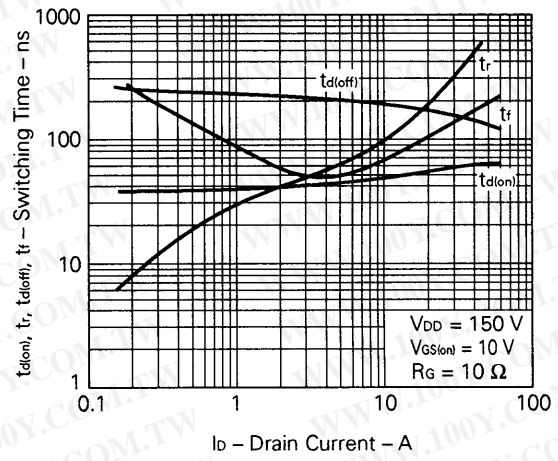
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



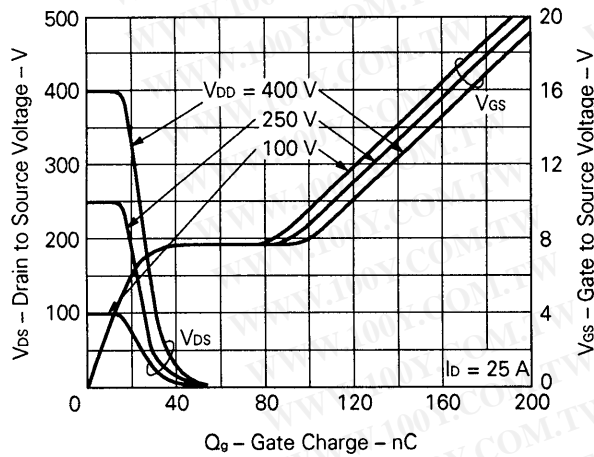
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



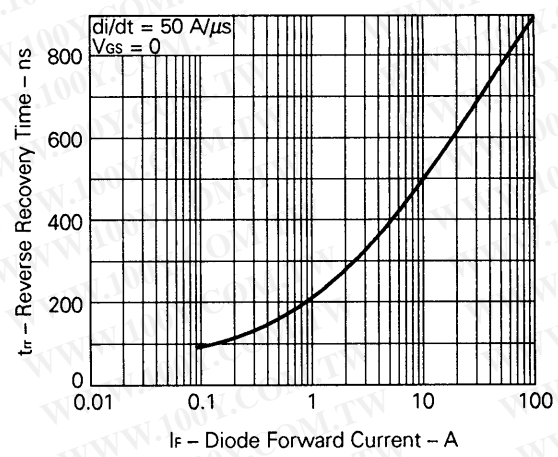
SWITCHING CHARACTERISTICS



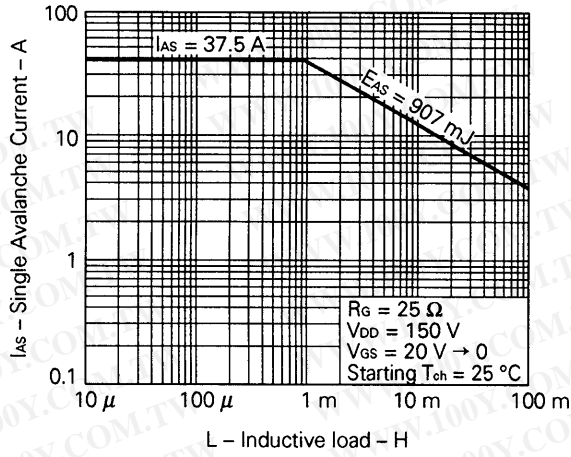
DYNAMIC INPUT CHARACTERISTICS



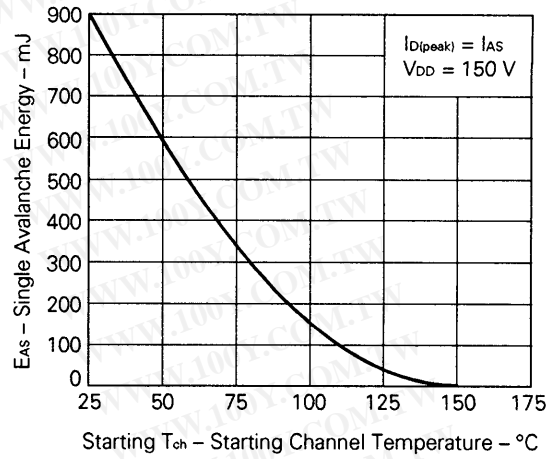
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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