

P-CHANNEL POWER MOS FET ARRAY SWITCHING INDUSTRIAL USE

DESCRIPTION

The μ PA1523B is P-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- Full Mold Package with 4 Circuits
- -4 V driving is possible
- Low On-state Resistance
 $R_{DS(on)1} = 0.8 \Omega$ MAX. (@ $V_{GS} = -10$ V, $I_D = -1$ A)
 $R_{DS(on)2} = 1.3 \Omega$ MAX. (@ $V_{GS} = -4$ V, $I_D = -1$ A)
- Low Input Capacitance $C_{iss} = 190$ pF TYP.

ORDERING INFORMATION

Type Number	Package
μ PA1523BH	10 Pin SIP

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0$)	V_{DSS}	-60	V
Gate to Source Voltage ($V_{DS} = 0$)	$V_{GSS(AC)}$	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 2.0	A/unit
Drain Current (pulse)	$I_{D(pulse)}$ *1	± 8.0	A/unit
Total Power Dissipation	P_{T1} *2	28	W
Total Power Dissipation	P_{T2} *3	3.5	W
Channel Temperature	T_{CH}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$
Single Avalanche Current	I_{AS} *4	-2.0	A
Single Avalanche Energy	E_{AS} *4	0.4	mJ

*1 $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

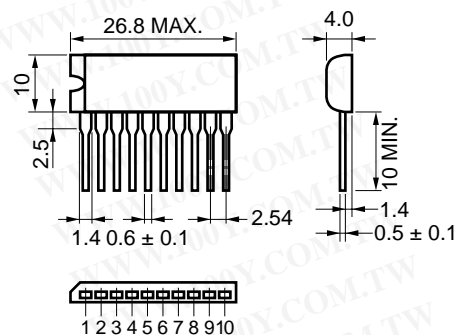
*2 4 Circuits, $T_C = 25^\circ\text{C}$

*3 4 Circuits, $T_A = 25^\circ\text{C}$

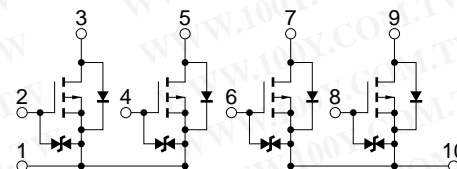
*4 Starting $T_{CH} = 25^\circ\text{C}$, $V_{DD} = -30$ V, $V_{GS} = -20$ V \rightarrow 0, $R_G = 25 \Omega$,
 $L = 100 \mu\text{H}$

Build-in Gate Diodes are for protection from static electricity in handling.
 In case high voltage over V_{GSS} is applied, please append gate protection circuits.

PACKAGE DIMENSIONS in millimeters



CONNECTION DIAGRAM



ELECTRODE CONNECTION

2, 4, 6, 8: Gate
 3, 5, 7, 9: Drain
 1, 10 : Source

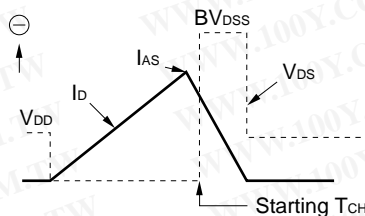
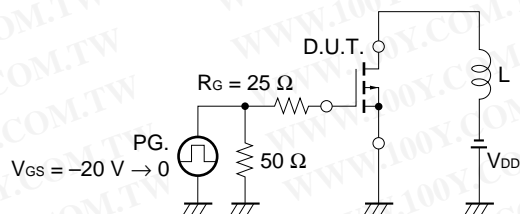
勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

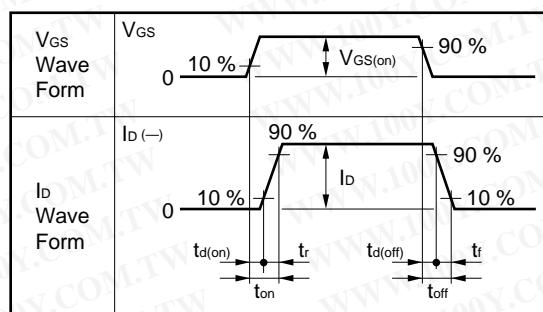
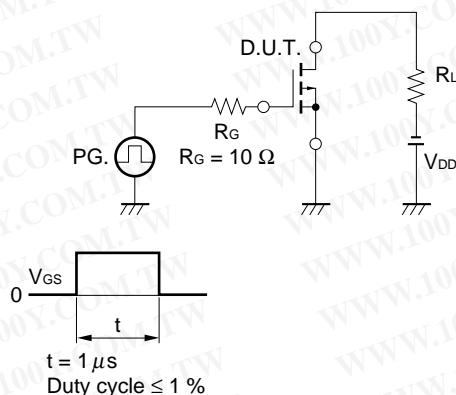
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I_{DSS}	$V_{DS} = -60\text{ V}, V_{GS} = 0$			-10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0$			± 10	μA
Gate Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1.0\text{ mA}$	-1.0		-2.0	V
Forward Transfer Admittance	$ Y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -1.0\text{ A}$	0.8			S
Drain to Source ON-Resistance	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -1.0\text{ A}$		0.5	0.8	Ω
Drain to Source ON-Resistance	$R_{DS(on)2}$	$V_{GS} = -4.0\text{ V}, I_D = -1.0\text{ A}$		0.8	1.3	Ω
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0, f = 1.0\text{ MHz}$		190		pF
Output Capacitance	C_{oss}			115		pF
Reverse Transfer Capacitance	C_{rss}			43		pF
Turn-on Delay Time	$t_{d(on)}$	$I_D = -1.0\text{ A}, V_{GS(on)} = -10\text{ V},$ $V_{DD} \approx -30\text{ V}, R_L = 30\ \Omega$		8		ns
Rise Time	t_r			53		ns
Turn-off Delay Time	$t_{d(off)}$			400		ns
Fall Time	t_f			230		ns
Total Gate Charge	Q_G	$V_{GS} = -10\text{ V}, I_D = -2.0\text{ A}, V_{DD} = -48\text{ V}$		10		nC
Gate to Source Charge	Q_{GS}			1.1		nC
Gate to Drain Charge	Q_{GD}			3.5		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 2.0\text{ A}, V_{GS} = 0$		1.0		V
Reverse Recovery Time	t_{rr}	$I_F = 2.0\text{ A}, V_{GS} = 0, di/dt = 50\text{ A}/\mu\text{s}$		180		ns
Reverse Recovery Charge	Q_{rr}			250		nC

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

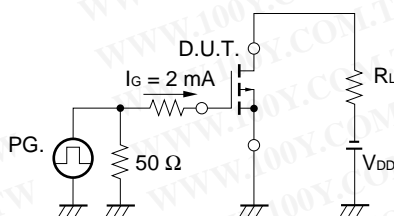
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

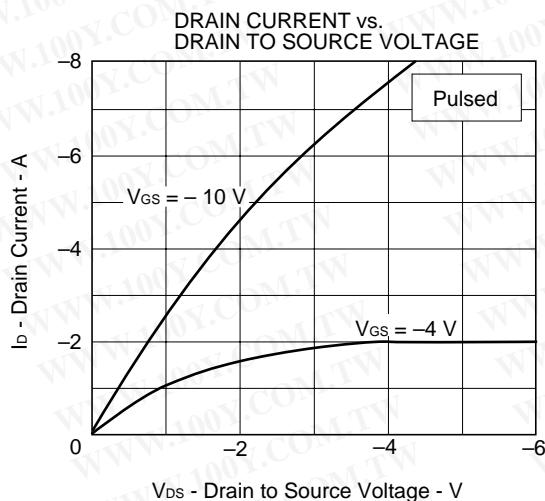
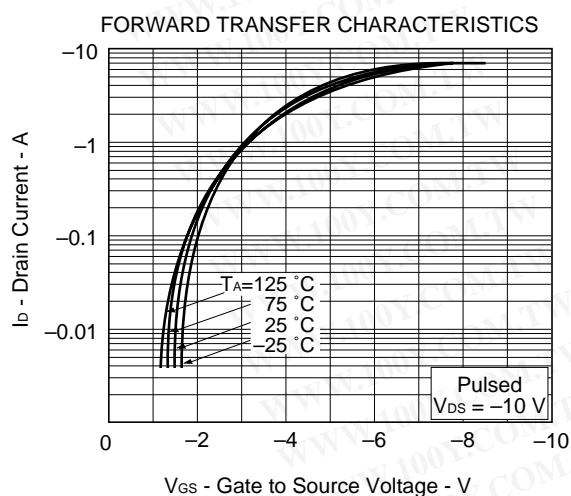
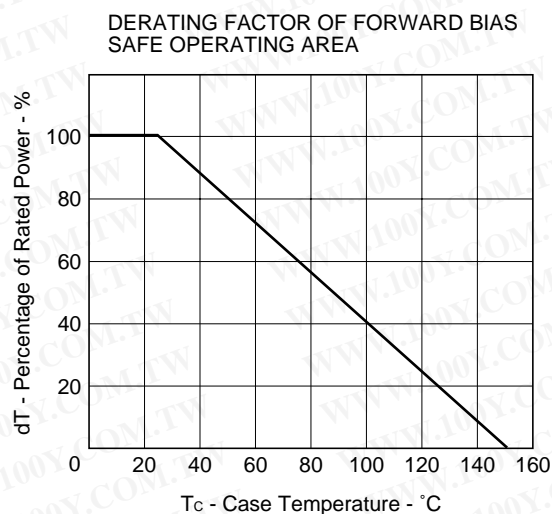
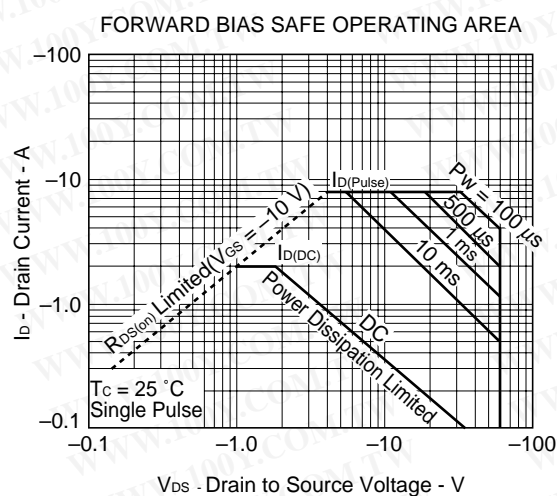
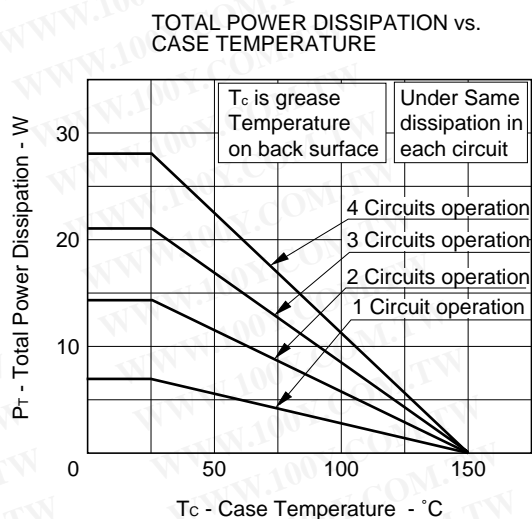
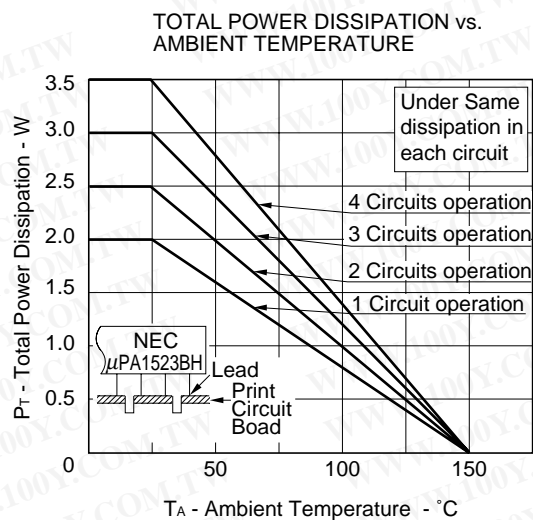


Test Circuit 3 Gate Charge



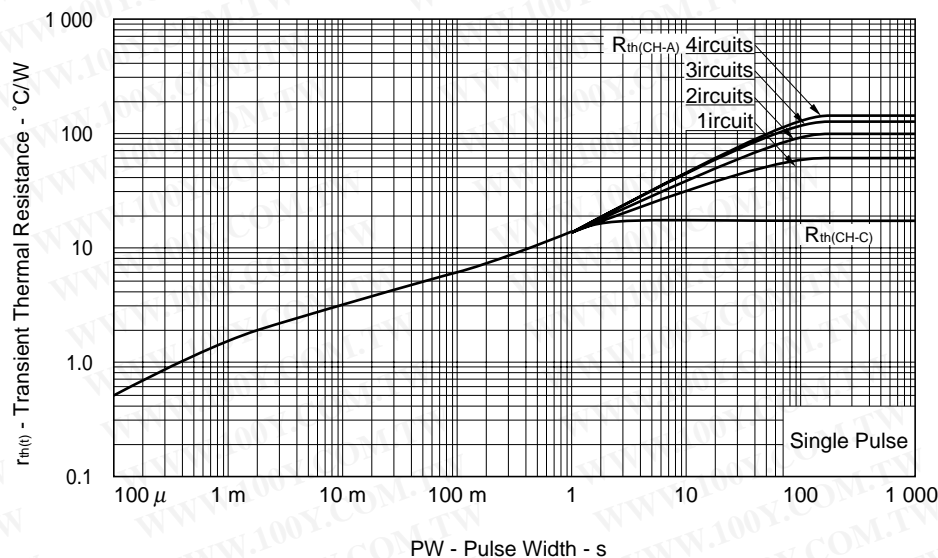
勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

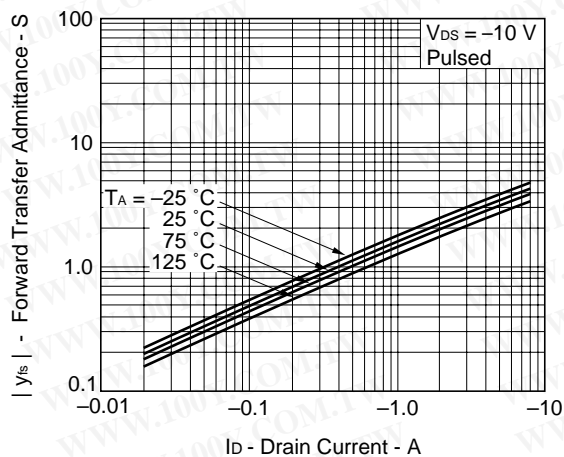


勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

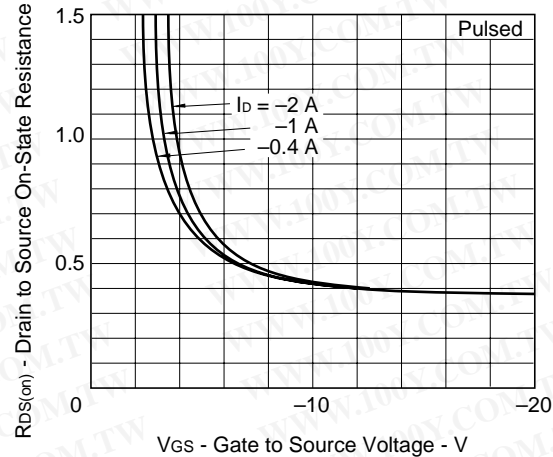
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



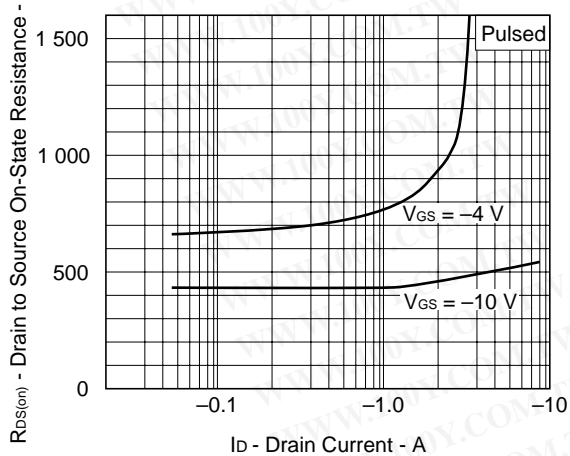
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



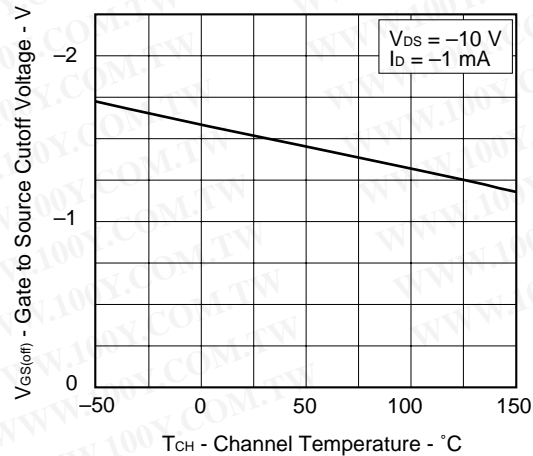
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

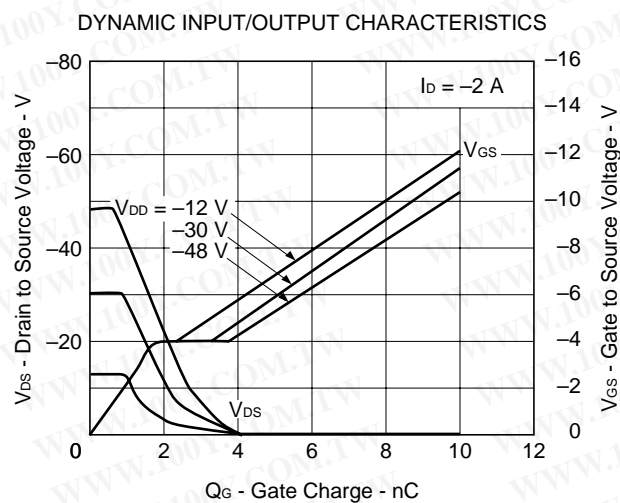
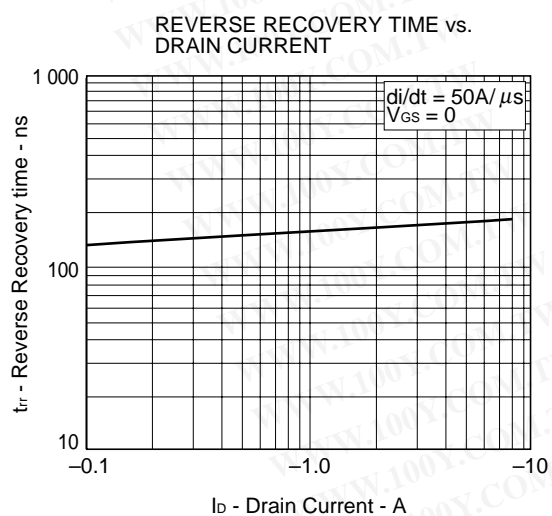
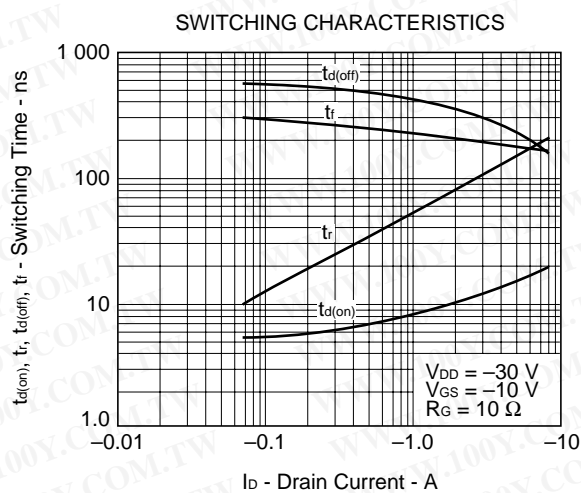
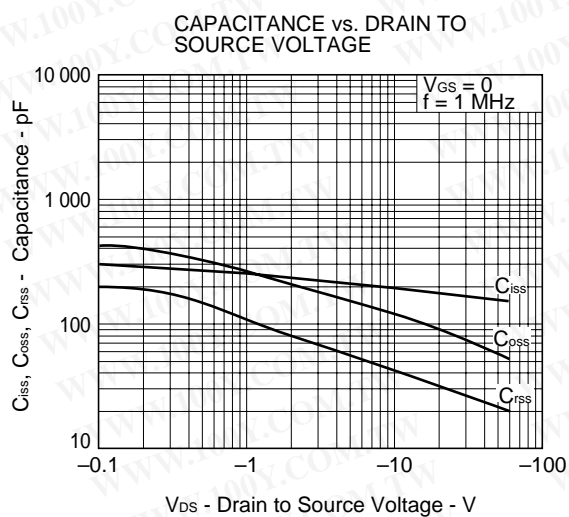
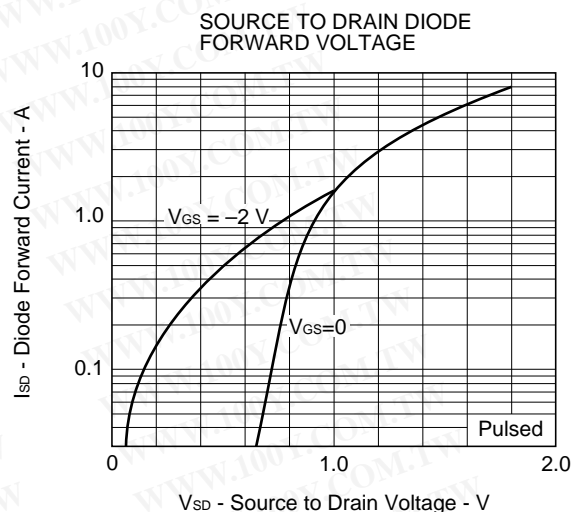
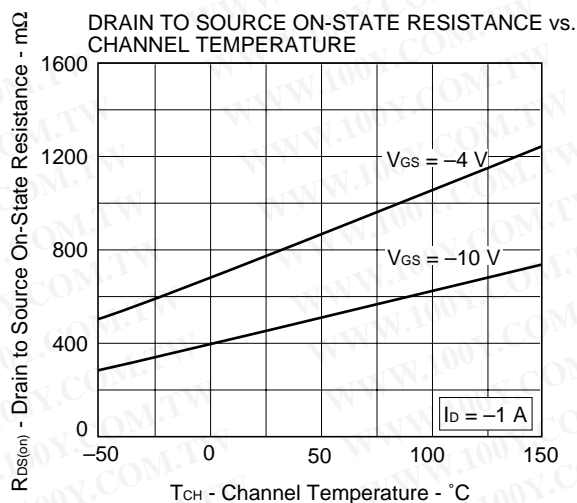


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

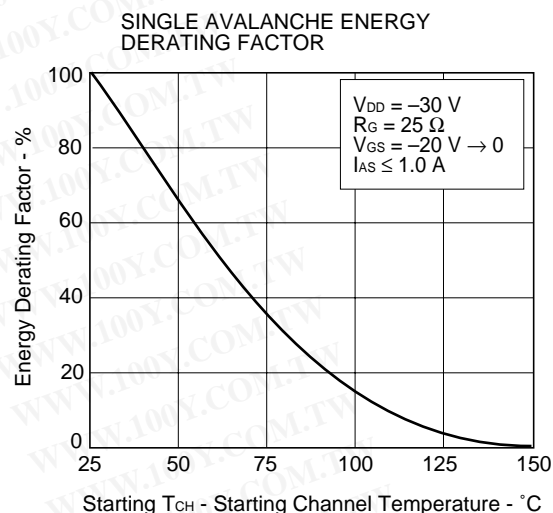
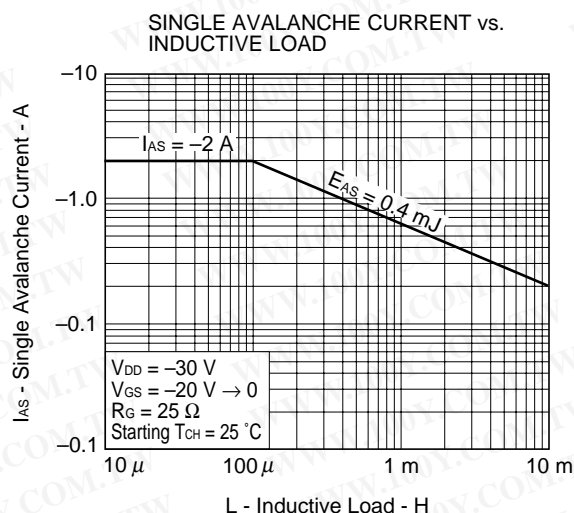


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



REFERENCE

Document Name	Document No.
NEC semiconductor for device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

[MEMO]

勝 特 力 材 料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customer must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices in "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.