

NTD110N02R

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-54151736
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Power MOSFET 24 V, 110 A, N-Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- Pb-Free Packages are Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	24	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	1.35	$^\circ\text{C/W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	110	W
Drain Current			
– Continuous @ $T_C = 25^\circ\text{C}$, Chip	I_D	110	A
– Continuous @ $T_C = 25^\circ\text{C}$, Limited by Package	I_D	110	A
– Continuous @ $T_A = 25^\circ\text{C}$, Limited by Wires	I_D	32	A
– Single Pulse ($t_p = 10 \mu\text{s}$)	I_D	110	A
Thermal Resistance			
– Junction-to-Ambient (Note 1)	$R_{\theta JA}$	52	$^\circ\text{C/W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.88	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	17.5	A
Thermal Resistance			
– Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.5	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	12.5	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, $I_L = 15.5 \text{ Apk}$, $L = 1.0 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	120	mJ
Maximum Lead Temperature for Soldering Purposes, (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 0.5 sq in drain pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.

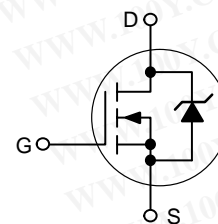


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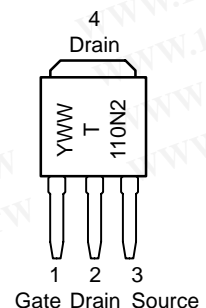
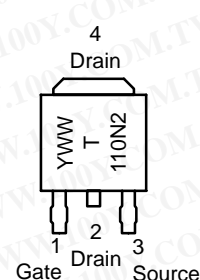
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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
24 V	4.1 m Ω @ 10 V	110 A

N-Channel



MARKING DIAGRAM & PIN ASSIGNMENTS



Y = Year
WW = Work Week
T110N2 = Device Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) ($V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$) Positive Temperature Coefficient	$V_{(BR)DSS}$	24	28 15		V mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$) ($V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$)	I_{DSS}			1.5 10	μA
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ($V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$) Negative Threshold Temperature Coefficient	$V_{GS(th)}$	1.0	1.5 5.0	2.0	V mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 10\text{ V}$, $I_D = 110\text{ A}$) ($V_{GS} = 4.5\text{ V}$, $I_D = 55\text{ A}$) ($V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$) ($V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$)	$R_{DS(on)}$		4.1 5.5 3.9 5.5	4.6 6.2	m Ω
Forward Transconductance ($V_{DS} = 10\text{ V}$, $I_D = 15\text{ A}$) (Note 3)	g_{FS}		44		Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz})$	C_{iss}		2710	3440	pF
Output Capacitance		C_{oss}		1105	1670	
Transfer Capacitance		C_{rss}		450	640	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$(V_{GS} = 10\text{ V}$, $V_{DD} = 10\text{ V}$, $I_D = 40\text{ A}$, $R_G = 3.0\text{ }\Omega$)	$t_{d(on)}$		11	22	ns
Rise Time		t_r		39	80	
Turn-Off Delay Time		$t_{d(off)}$		27	40	
Fall Time		t_f		21	40	
Gate Charge	$(V_{GS} = 4.5\text{ V}$, $I_D = 40\text{ A}$, $V_{DS} = 10\text{ V})$ (Note 3)	Q_T		23.6	28	nC
		Q_{GS}		5.1		
		Q_{DS}		11		

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 20\text{ A}$, $V_{GS} = 0\text{ V})$ (Note 3) $(I_S = 55\text{ A}$, $V_{GS} = 0\text{ V})$ $(I_S = 20\text{ A}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C})$	V_{SD}		0.82 0.99 0.65	1.2	V
Reverse Recovery Time	$(I_S = 30\text{ A}$, $V_{GS} = 0\text{ V}$, $di_S/dt = 100\text{ A}/\mu\text{s})$ (Note 3)	t_{rr}		36.5		ns
		t_a		30		
		t_b		25		
Reverse Recovery Stored Charge		Q_{rr}		0.048		μC

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

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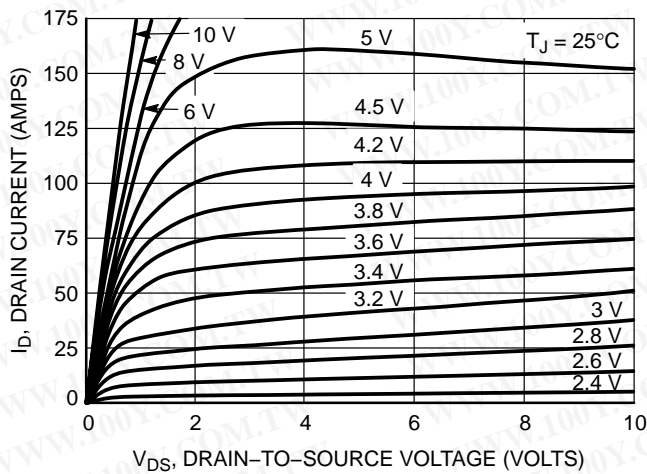


Figure 1. On-Region Characteristics

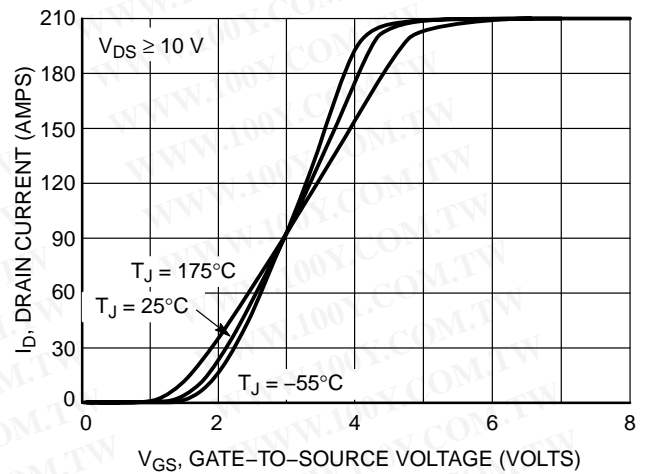


Figure 2. Transfer Characteristics

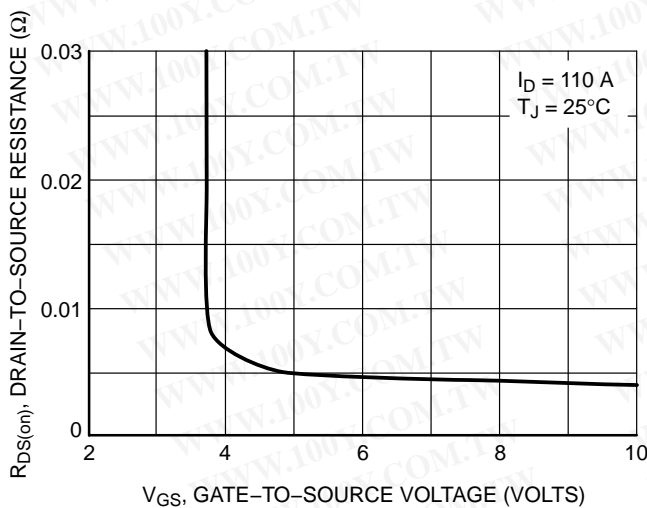


Figure 3. On-Resistance versus Gate-to-Source Voltage

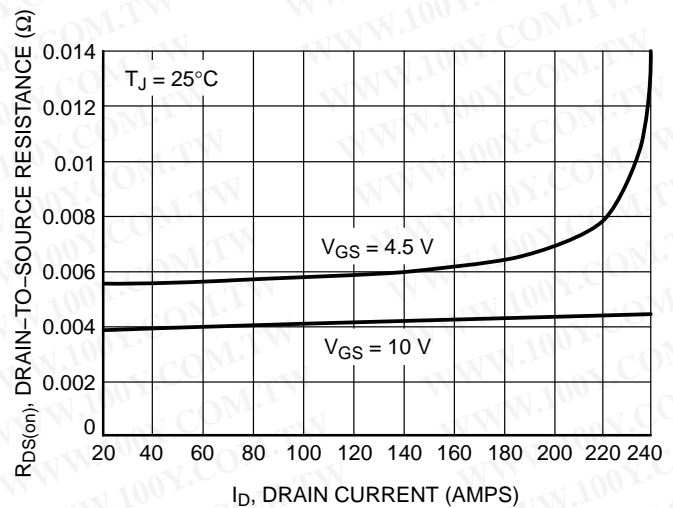


Figure 4. On-Resistance versus Drain Current and Gate Voltage

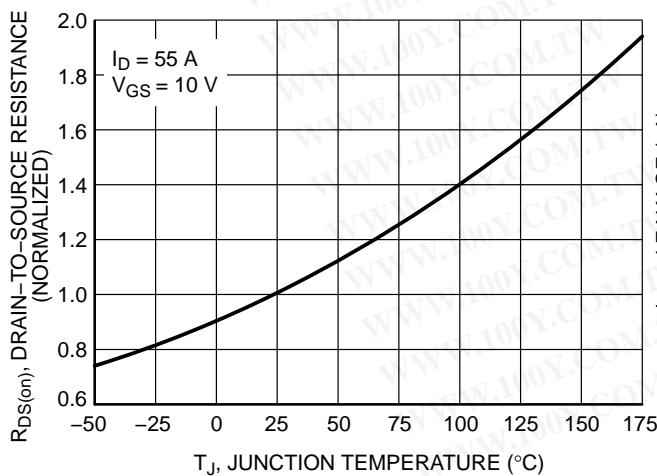


Figure 5. On-Resistance Variation with Temperature

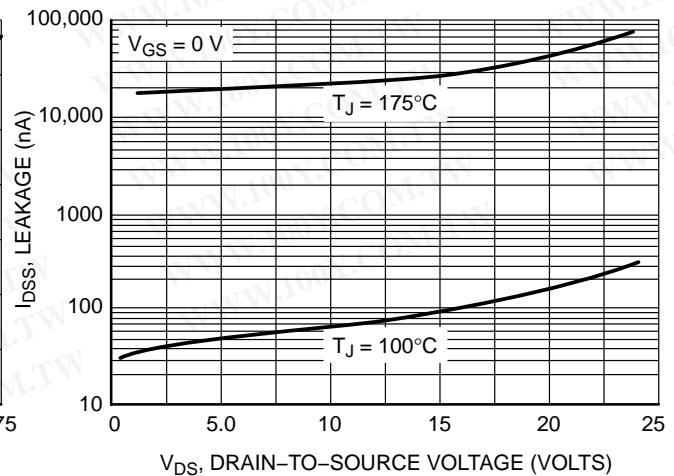


Figure 6. Drain-to-Source Leakage Current versus Voltage

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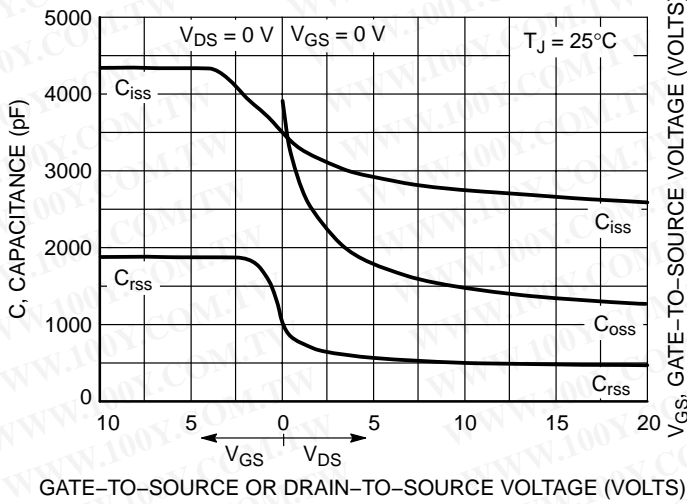


Figure 7. Capacitance Variation

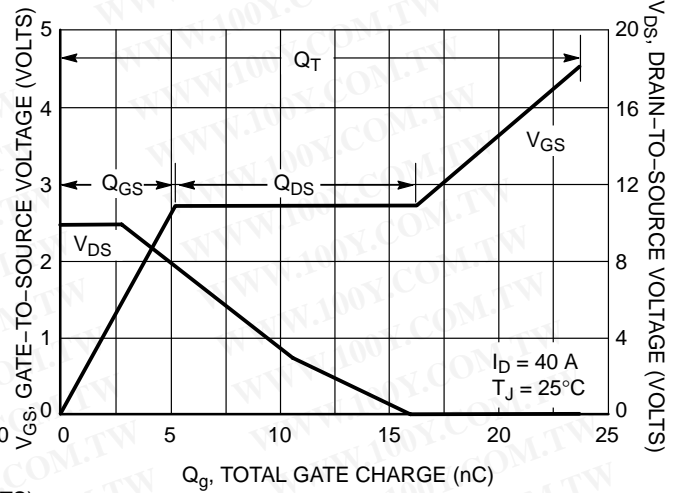


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

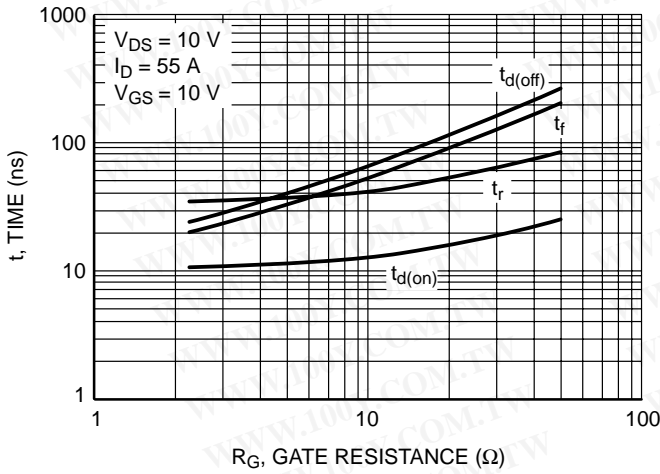


Figure 9. Resistive Switching Time Variation versus Gate Resistance

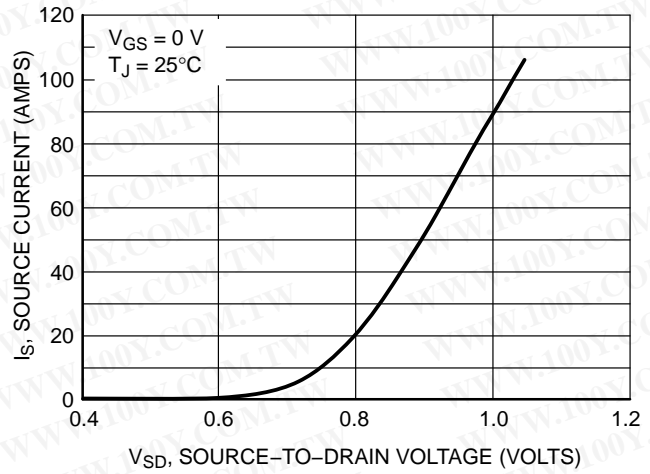


Figure 10. Diode Forward Voltage versus Current

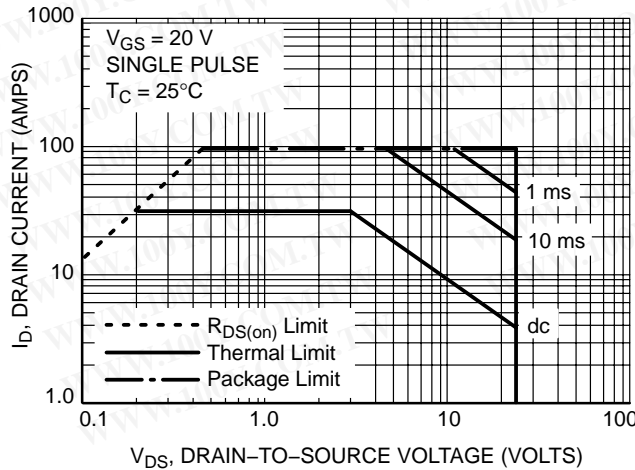


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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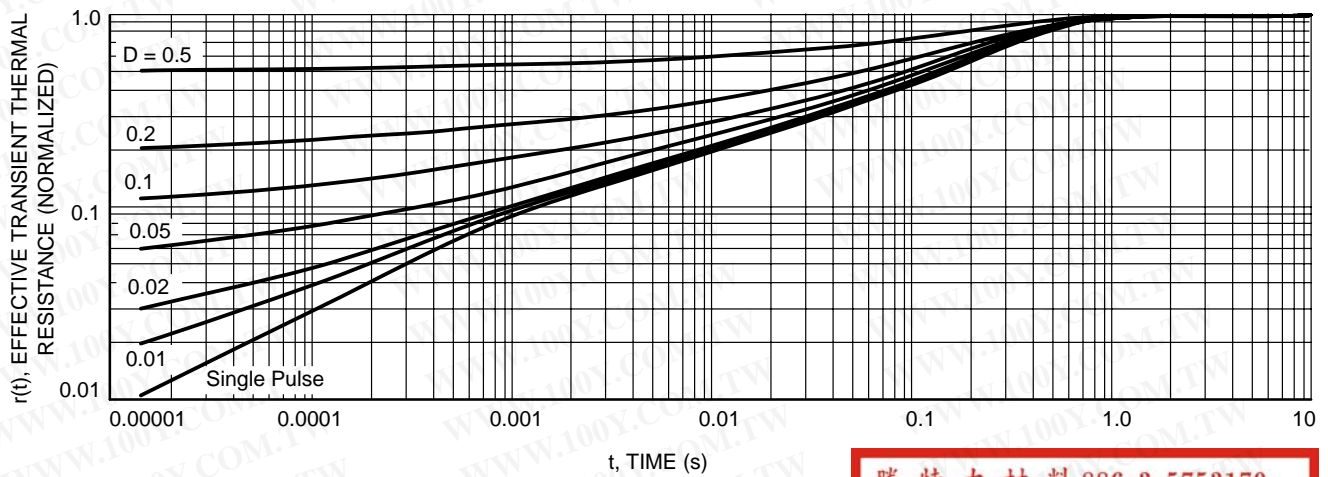


Figure 12. Thermal Response

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ORDERING INFORMATION

Device	Package	Shipping†
NTD110N02R	DPAK	75 Units/Rail
NTD110N02RG	DPAK (Pb-Free)	75 Units/Rail
NTD110N02R-001	DPAK (Straight Lead)	75 Units/Rail
NTD110N02R-001G	DPAK (Straight Lead) (Pb-Free)	75 Units/Rail
NTD110N02RT4	DPAK	2500 Tape & Reel
NTD110N02RT4G	DPAK (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

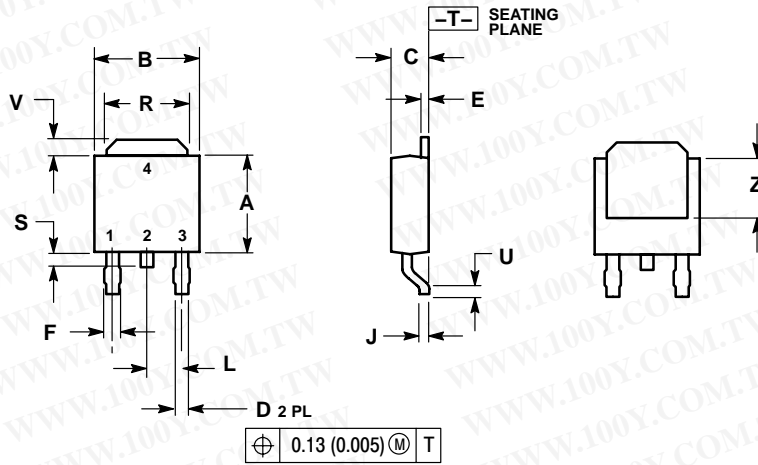
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PACKAGE DIMENSIONS

DPAK
CASE 369AA-01
ISSUE O

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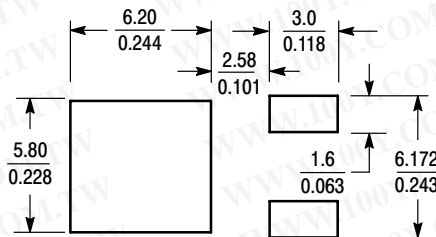


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
- PIN 1. GATE
 - DRAIN
 - SOURCE
 - DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

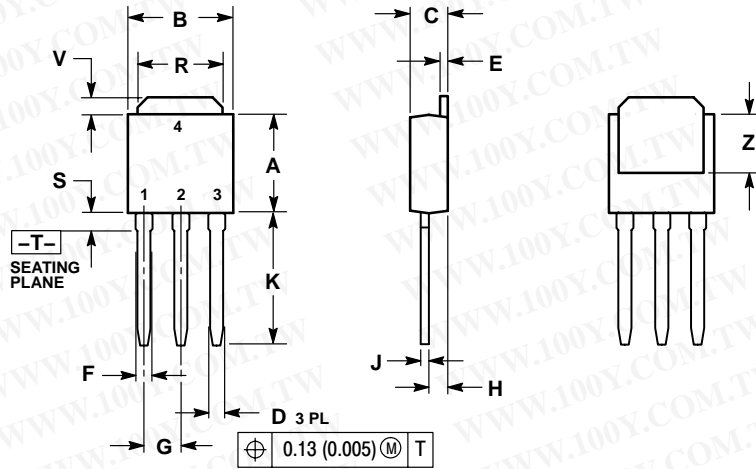
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

DPAK
CASE 369D-01
ISSUE O

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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC	2.29 BSC		
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

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