

NTMFS4708N

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-54151736
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)



Power MOSFET

30 V, 19 A, Single N-Channel, SOIC-8 FL

Features

- Fast Switching Times
- Low Gate Charge
- Low $R_{DS(on)}$
- Low Inductance SOIC-8 Package
- These are Pb-Free Devices

Applications

- Notebooks, Graphics Cards
- DC-DC Converters
- Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DSS}	30	V		
Gate-to-Source Voltage	V_{GS}	± 20	V		
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	11.5	A
		$T_A = 85^\circ\text{C}$		8.0	
		$t \leq 10\text{ s}$		$T_A = 25^\circ\text{C}$	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	2.2	W
		$t \leq 10\text{ s}$		6.25	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	7.8	A
		$T_A = 85^\circ\text{C}$		5.6	
Power Dissipation (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.0	W
Pulsed Drain Current	$t_p \leq 10\ \mu\text{s}$	I_{DM}	58	A	
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$		
Source Current (Body Diode)	I_S	6.25	A		
Single Pulse Drain-to-Source Avalanche Energy. $V_{DD} = 25\text{ V}, V_{GS} = 10\text{ V}, I_{PK} = 7.0\text{ A}, L = 10\text{ mH}, R_G = 25\ \Omega$	E_{AS}	245	mJ		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$		

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	56.5	$^\circ\text{C/W}$
Junction-to-Ambient - $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	20	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	124	

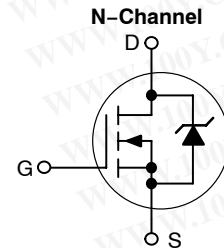
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq).

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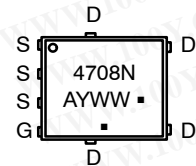
$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
30 V	7.3 m Ω @ 10 V	19 A
	10.1 m Ω @ 4.5 V	



MARKING DIAGRAM & PIN ASSIGNMENT



SOIC-8 FLAT LEAD
 CASE 488AA
 STYLE 1



4708N = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4708NT1G	SOIC-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4708NT3G	SOIC-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			10		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		50	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 11.5\text{ A}$		7.3	10	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 9.5\text{ A}$		10.1	14	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 11.5\text{ A}$		23		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 24\text{ V}$		970		pF
Output Capacitance	C_{OSS}			440		
Reverse Transfer Capacitance	C_{RSS}			115		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 11.5\text{ A}$		10	15	nC
Threshold Gate Charge	$Q_{G(TH)}$			1.3		
Gate-to-Source Charge	Q_{GS}			2.6		
Gate-to-Drain Charge	Q_{GD}			4.8		
Gate Resistance	R_G			1.95		Ω

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V}, I_D = 1.0\text{ A}, R_G = 3.0\ \Omega$		6.7		ns
Rise Time	t_r			4.3		
Turn-Off Delay Time	$t_{d(off)}$			20		
Fall Time	t_f			16		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 6.25\text{ A}$	$T_J = 25^\circ\text{C}$	0.78	1.0	V
			$T_J = 125^\circ\text{C}$	0.60		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 6.25\text{ A}$		32		ns
Charge Time	t_a			15.5		
Discharge Time	t_b			16.5		
Reverse Recovery Charge	Q_{RR}			24		nC

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

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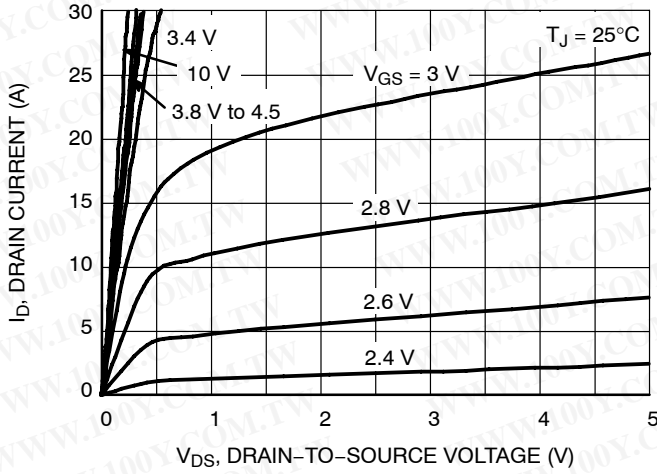


Figure 1. On-Region Characteristics

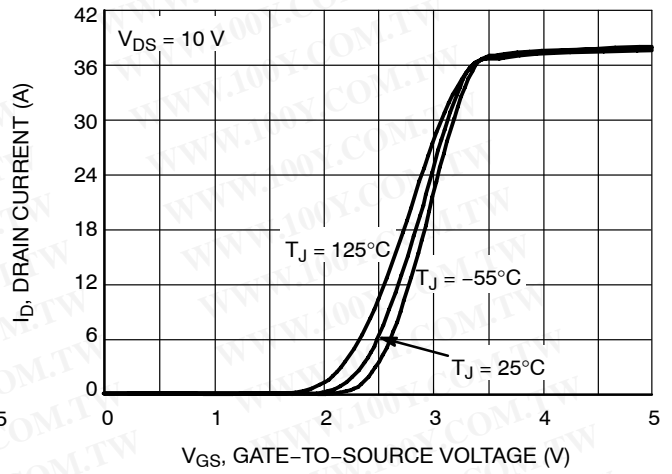


Figure 2. Transfer Characteristics

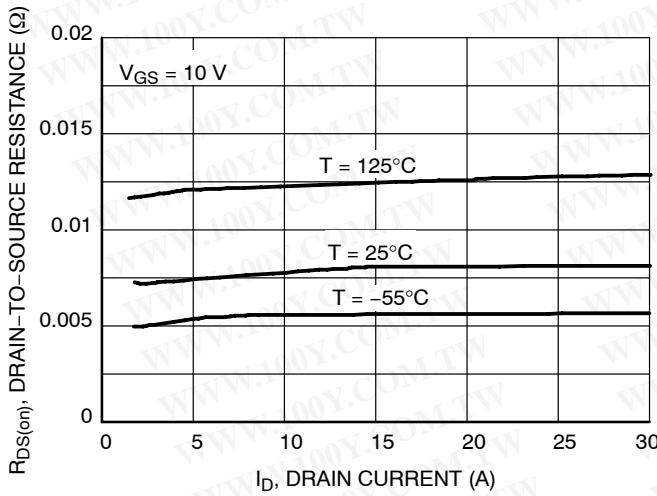


Figure 3. On-Resistance versus Drain Current and Temperature

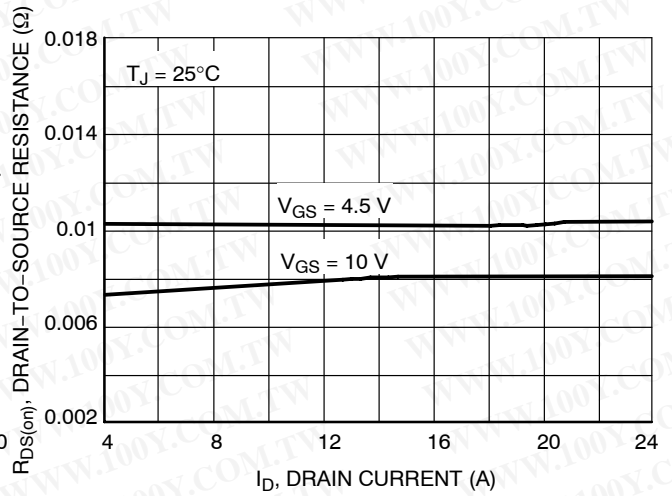


Figure 4. On-Resistance versus Drain Current and Gate Voltage

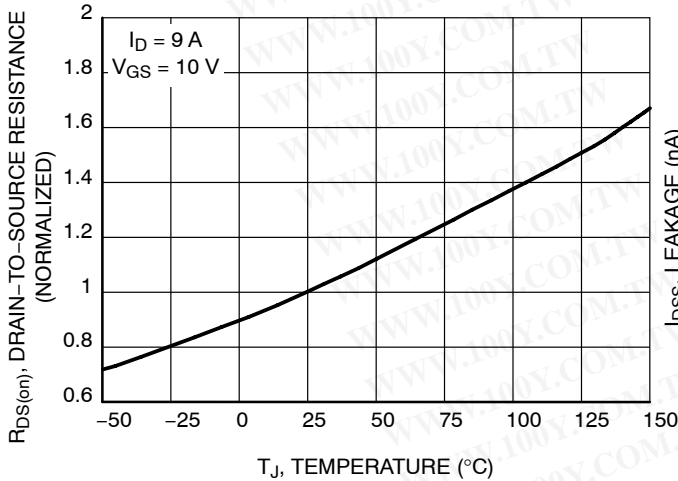


Figure 5. On-Resistance Variation with Temperature

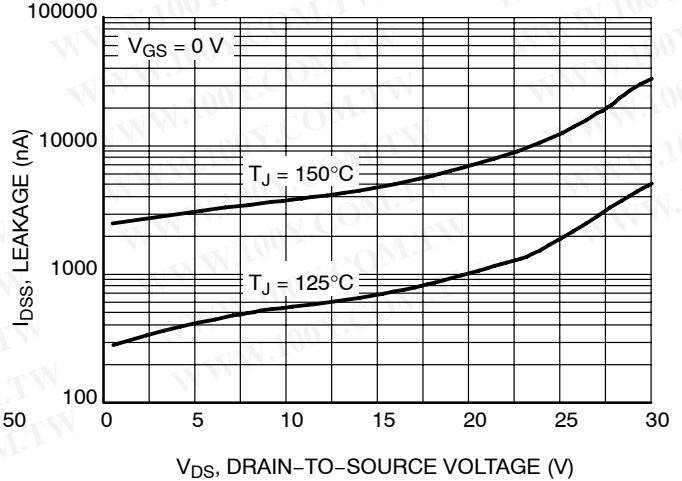


Figure 6. Drain-to-Source Leakage Current versus Voltage

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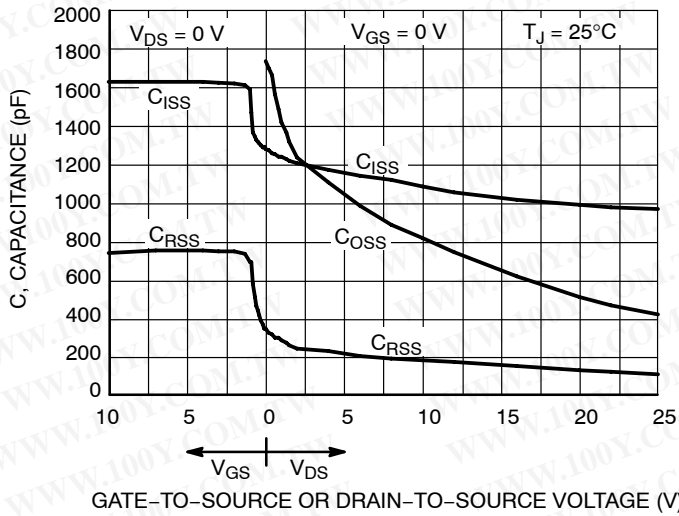


Figure 7. Capacitance Variation

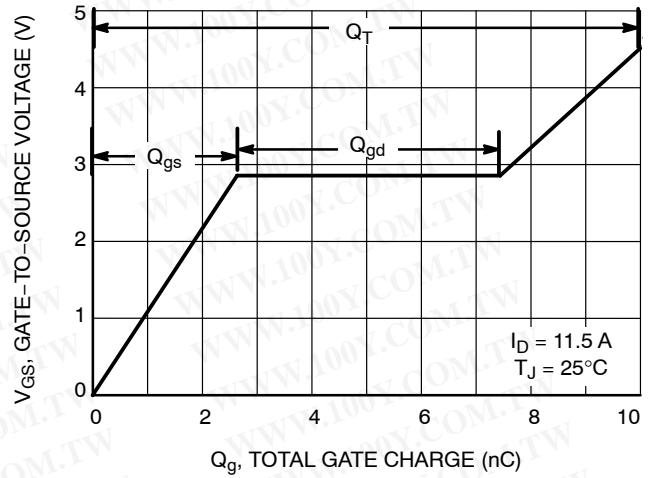


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

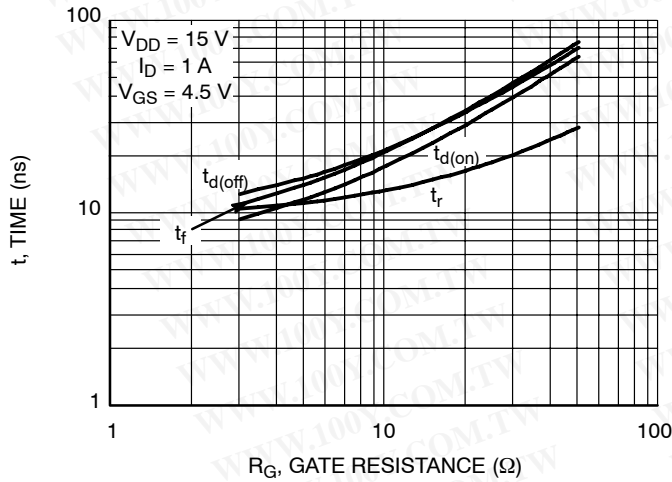


Figure 9. Resistive Switching Time Variation versus Gate Resistance

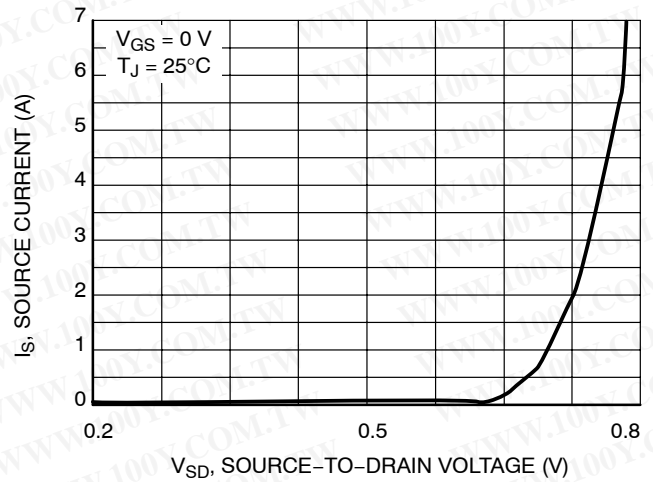


Figure 10. Diode Forward Voltage versus Current

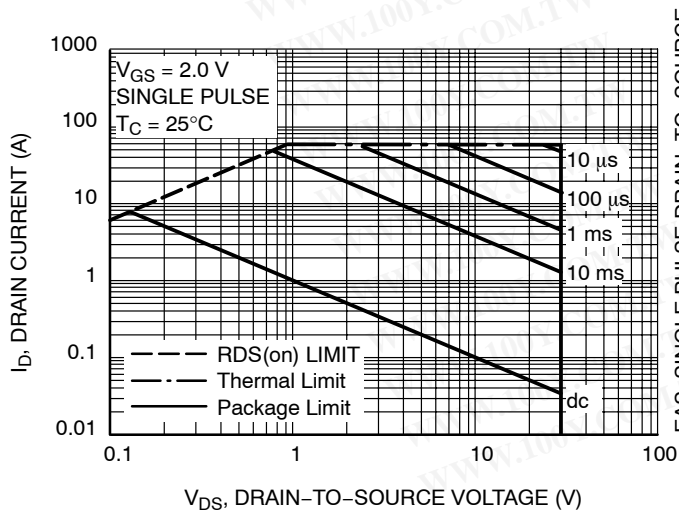


Figure 11. Maximum Rated Forward Biased Safe Operating Area

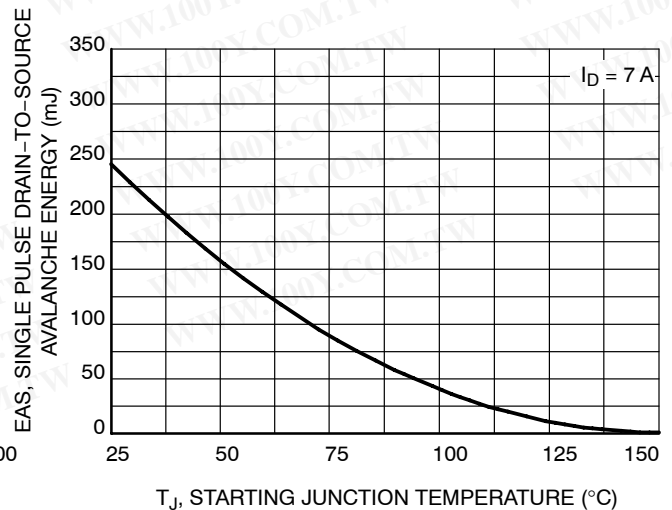


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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PACKAGE DIMENSIONS

DFN6 5*6*1 1.27 PITCH
(SO8 FL)
CASE 488AA-01
ISSUE B

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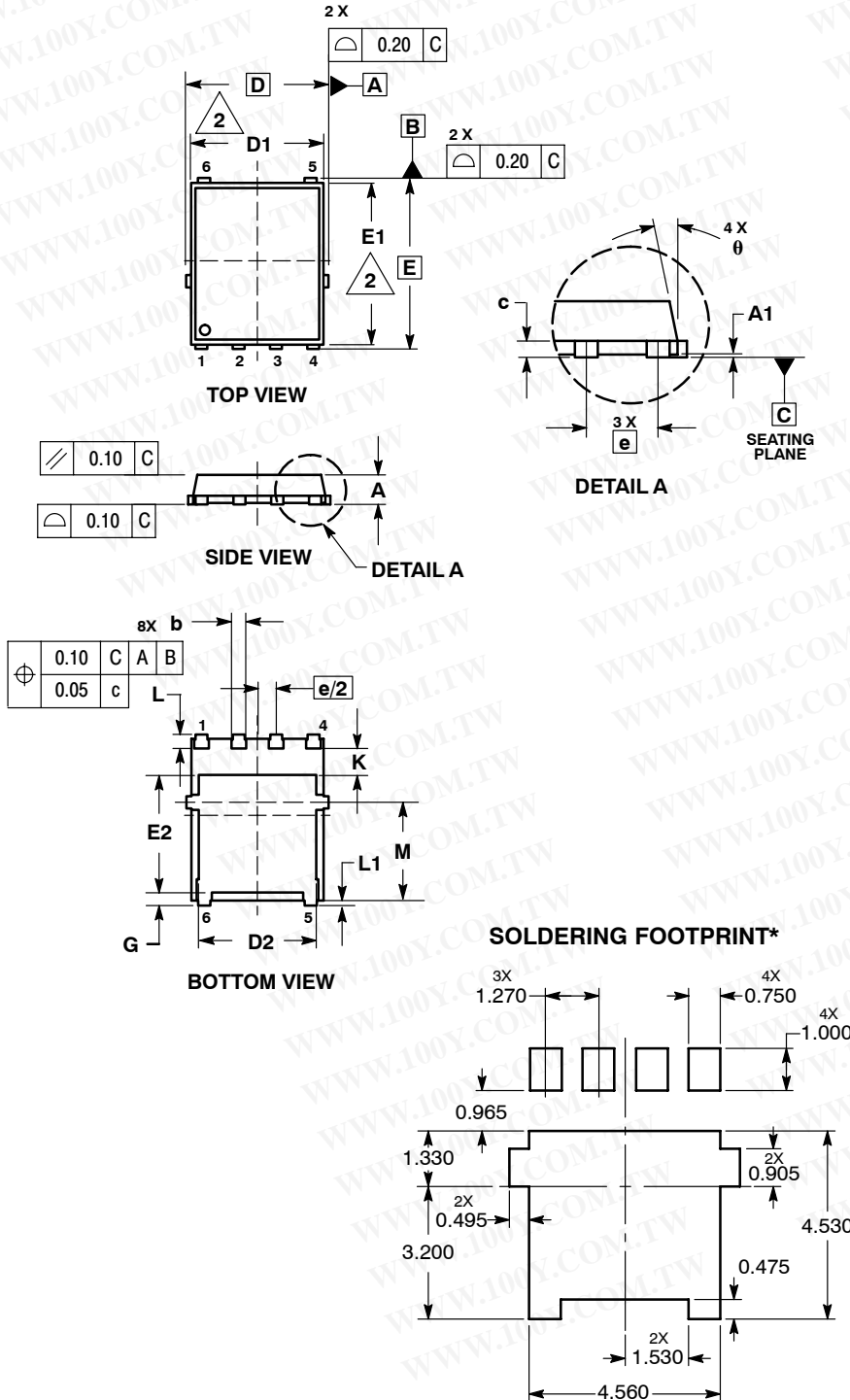
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	0.99	1.20
A1	0.00	----	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	----	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	----	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	0.51	----	----
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0°	----	12°

STYLE 1:

- PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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