Low Noise, Low Drift Single-Supply Operational Amplifiers

OP113/OP213/OP413

FEATURES

Single- or Dual-Supply Operation
Low Noise: 4.7 nV/√Hz @ 1 kHz
Wide Bandwidth: 3.4 MHz
Low Offset Voltage: 100 μV
Very Low Drift: 0.2 μV/°C
Unity Gain Stable
No Phase Reversal

APPLICATIONS

Digital Scales
Multimedia
Strain Gages
Battery-Powered Instrumentation
Temperature Transducer Amplifier

GENERAL DESCRIPTION

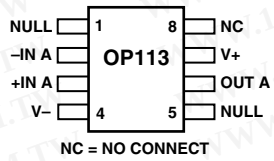
The OP113 family of single supply operational amplifiers features both low noise and drift. It has been designed for systems with internal calibration. Often these processor-based systems are capable of calibrating corrections for offset and gain, but they cannot correct for temperature drifts and noise. Optimized for these parameters, the OP113 family can be used to take advantage of superior analog performance combined with digital correction. Many systems using internal calibration operate from unipolar supplies, usually either 5 V or 12 V. The OP113 family is designed to operate from single supplies from 4 V to 36 V, and to maintain its low noise and precision performance.

The OP113 family is unity gain stable and has a typical gain bandwidth product of 3.4 MHz. Slew rate is in excess of 1 V/μs. Noise density is a very low 4.7 nV/√Hz, and noise in the 0.1 Hz to 10 Hz band is 120 nV p-p. Input offset voltage is guaranteed and offset drift is guaranteed to be less than 0.8 μV/°C. Input common-mode range includes the negative supply and to within 1 V of the positive supply over the full supply range. Phase reversal protection is designed into the OP113 family for cases where input voltage range is exceeded. Output voltage swings also include the negative supply and go to within 1 V of the positive rail. The output is capable of sinking and sourcing current throughout its range and is specified with 600 Ω loads.

Digital scales and other strain gage applications benefit from the very low noise and low drift of the OP113 family. Other applications include use as a buffer or amplifier for both A/D and D/A sigma-delta converters. Often these converters have high resolutions requiring the lowest noise amplifier to utilize their full potential. Many of these converters operate in either single supply or low supply voltage systems, and attaining the greater signal swing possible increases system performance.

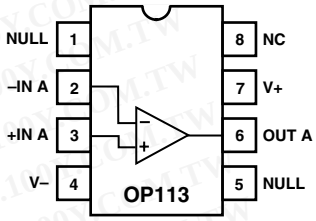
PIN CONNECTIONS

8-Lead Narrow-Body SO



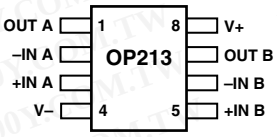
NC = NO CONNECT

8-Lead Plastic DIP

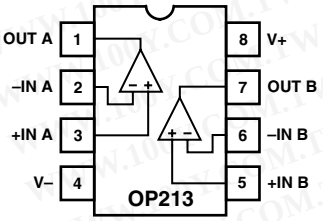


NC = NO CONNECT

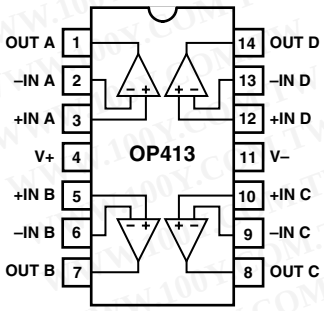
8-Lead Narrow-Body SO



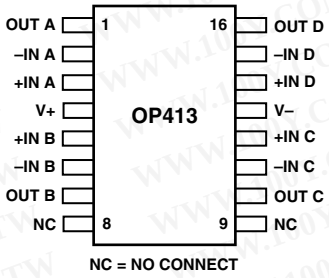
8-Lead Plastic DIP



14-Lead Plastic DIP



16-Lead Wide-Body SO



NC = NO CONNECT

The OP113 family is specified for single 5 V and dual ±15 V operation over the XIND—extended industrial (–40°C to +85°C) temperature range. They are available in plastic and SOIC surface mount packages.

REV. D

OP113/OP213/OP413–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = 25°C unless otherwise noted.

Parameter	Symbol	Conditions	E Grade Min	E Grade Typ	E Grade Max	F Grade Min	F Grade Typ	F Grade Max	Unit
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP113			75			150	µV
		–40°C ≤ T_A ≤ +85°C			125			225	µV
		OP213			100			250	µV
		–40°C ≤ T_A ≤ +85°C			150			325	µV
		OP413			125			275	µV
		–40°C ≤ T_A ≤ +85°C			175			350	µV
Input Bias Current	I_B	V_{CM} = 0 V,		240	600			600	nA
		–40°C ≤ T_A ≤ +85°C			700			700	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V							
		–40°C ≤ T_A ≤ +85°C			50			50	nA
Input Voltage Range	V_{CM}		–15		+14	–15		+14	V
Common-Mode Rejection	CMR	–15 V ≤ V_{CM} ≤ +14 V	100	116		96			dB
		–15 V ≤ V_{CM} ≤ +14 V,							
		–40°C ≤ T_A ≤ +85°C	97	116		94			dB
Large Signal Voltage Gain	A_{VO}	OP113, OP213,							
		R_L = 600 Ω,							
		–40°C ≤ T_A ≤ +85°C	1	2.4		1			V/µV
		OP413, R_L = 1 kΩ,							
		–40°C ≤ T_A ≤ +85°C	1	2.4		1			V/µV
		R_L = 2 kΩ,							
		–40°C ≤ T_A ≤ +85°C	2	8		2			V/µV
Long-Term Offset Voltage[1]	V_{OS}	Note 1			150			300	µV
Offset Voltage Drift[2]	$\Delta V_{OS}/\Delta T$	Note 2		0.2	0.8			1.5	µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	14			14			V
		R_L = 2 kΩ,							
		–40°C ≤ T_A ≤ +85°C	13.9			13.9			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ			–14.5			–14.5	V
		R_L = 2 kΩ,							
		–40°C ≤ T_A ≤ +85°C			–14.5			–14.5	V
Short Circuit Limit	I_{SC}			±40			±40		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±2 V to ±18 V	103	120		100			dB
		V_S = ±2 V to ±18 V							
		–40°C ≤ T_A ≤ +85°C	100	120		97			dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 0 V, R_L = ∞,							
		V_S = ±18 V			3			3	mA
		–40°C ≤ T_A ≤ +85°C			3.8			3.8	mA
Supply Voltage Range	V_S		4		±18	4		±18	V
AUDIO PERFORMANCE									
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ							
		f = 1 kHz,		0.0009			0.0009		%
Voltage Noise Density	e_n	f = 10 Hz		9			9		nV/√Hz
		f = 1 kHz		4.7			4.7		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4			0.4		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		120			120		nV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ	0.8	1.2		0.8	1.2		V/µs
Gain Bandwidth Product	GBP			3.4			3.4		MHz
Channel Separation		V_{OUT} = 10 V p-p							
		R_L = 2 kΩ, f = 1 kHz		105			105		dB
Settling Time	t_S	to 0.01%, 0 V to 10 V Step		9			9		µs

NOTES
[1]Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125 °C, with an LTPD of 1.3.
[2]Guaranteed specifications, based on characterization data.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = 5.0 V, T_A = 25°C unless otherwise noted.)

Parameter	Symbol	Conditions	E Grade Min	E Grade Typ	E Grade Max	F Grade Min	F Grade Typ	F Grade Max	Unit
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP113			125			175	µV
		–40°C ≤ T_A ≤ +85°C			175			250	µV
		OP213			150			300	µV
		–40°C ≤ T_A ≤ +85°C			225			375	µV
		OP413			175			325	µV
		–40°C ≤ T_A ≤ +85°C			250			400	µV
Input Bias Current	I_B	V_{CM} = 0 V, V_{OUT} = 2		300	650			650	nA
		–40°C ≤ T_A ≤ +85°C			750			750	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V, V_{OUT} = 2							
		–40°C ≤ T_A ≤ +85°C			50			50	nA
Input Voltage Range	V_{CM}		0		+4			+4	V
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 4 V	93	106		90			dB
		0 V ≤ V_{CM} ≤ 4 V, –40°C ≤ T_A ≤ +85°C	90			87			dB
Large Signal Voltage Gain	A_{VO}	OP113, OP213, R_L = 600 Ω, 2 kΩ							
		0.01 V ≤ V_{OUT} ≤ 3.9 V	2			2			V/µV
		OP413, R_L = 600, 2 kΩ, 0.01 V ≤ V_{OUT} ≤ 3.9 V	1			1			V/µV
Long-Term Offset Voltage[1]	V_{OS}	Note 1			200			350	µV
Offset Voltage Drift[2]	DV_{OS}/DT	Note 2		0.2	1.0			1.5	µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	R_L = 600 kΩ	4.0			4.0			V
		R_L = 100 kΩ, –40°C ≤ T_A ≤ +85°C	4.1			4.1			V
		R_L = 600 Ω, –40°C ≤ T_A ≤ +85°C	3.9			3.9			V
Output Voltage Swing Low	V_{OL}	R_L = 600 Ω, –40°C ≤ T_A ≤ +85°C			8			8	mV
		R_L = 100 kΩ, –40°C ≤ T_A ≤ +85°C		8			8		mV
Short Circuit Limit	I_{SC}			±30			±30		mA
POWER SUPPLY									
Supply Current	I_{SY}	V_{OUT} = 2.0 V, No Load		1.6	2.7			2.7	mA
	I_{SY}	–40°C ≤ T_A ≤ +85°C			3.0			3.0	mA
AUDIO PERFORMANCE									
THD + Noise		V_{OUT} = 0 dBu, f = 1 kHz		0.001			0.001		%
Voltage Noise Density	e_n	f = 10 Hz		9			9		nV/√Hz
		f = 1 kHz		4.7			4.7		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.45			0.45		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		120			120		nV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ	0.6	0.9		0.6			V/µs
Gain Bandwidth Product	GBP			3.5			3.5		MHz
Settling Time	t_S	to 0.01%, 2 V Step		5.8			5.8		µs

NOTES

[1]Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125 °C, with an LTPD of 1.3.

[2]Guaranteed specifications, based on characterization data.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage . . . . . ±18 V
Differential Input Voltage . . . . . ±10 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
P, S Packages . . . . . –65°C to +150°C
Operating Temperature Range
OP113/OP213/OP413E, F . . . . . –40°C to +85°C
Junction Temperature Range
P, S Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

Package Type	θ_{JA}[2]	θ_{JC}	Unit
8-Lead Plastic DIP (P)	103	43	°C/W
8-Lead SOIC (S)	158	43	°C/W
14-Lead Plastic DIP (P)	83	39	°C/W
16-Lead SOIC (S)	92	27	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

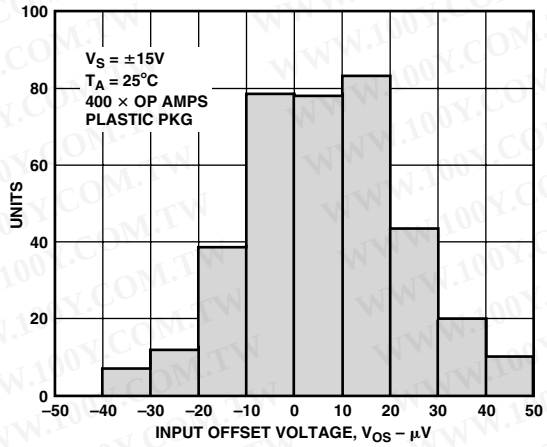
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
OP113ES	–40°C to +85°C	8-Lead SOIC	SO-8
OP113FP*	–40°C to +85°C	8-Lead Plastic DIP	N-8
OP113FS	–40°C to +85°C	8-Lead SOIC	SO-8
OP213EP*	–40°C to +85°C	8-Lead Plastic DIP	N-8
OP213ES	–40°C to +85°C	8-Lead SOIC	SO-8
OP213FP	–40°C to +85°C	8-Lead Plastic DIP	N-8
OP213FS	–40°C to +85°C	8-Lead SOIC	SO-8
OP413ES	–40°C to +85°C	16-Lead Wide SOIC	R-16
OP413FP*	–40°C to +85°C	14-Lead Plastic DIP	N-14
OP413FS	–40°C to +85°C	16-Lead Wide SOIC	R-16

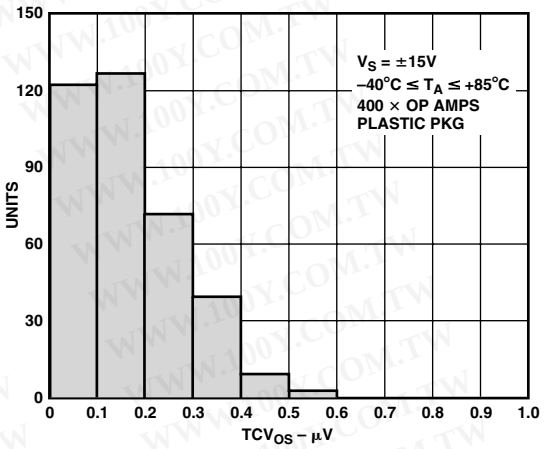
*Not for new designs; obsolete April 2002.

CAUTION

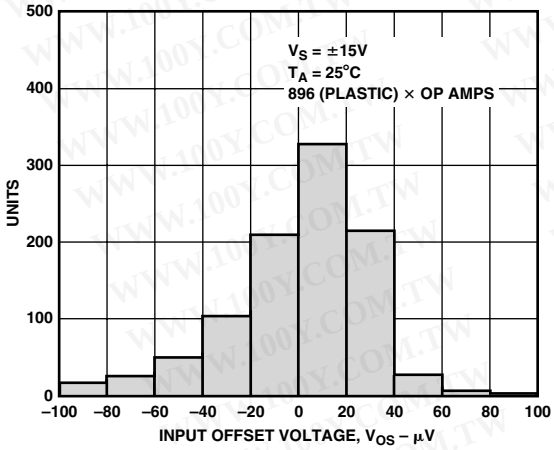
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP113/OP213/OP413 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



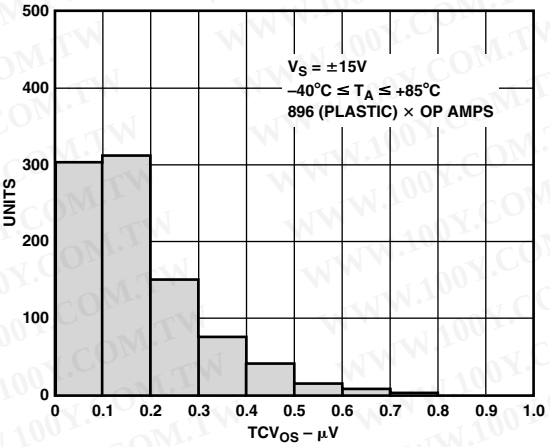
TPC 1a. OP113 Input Offset (V_{OS}) Distribution @ ±15 V



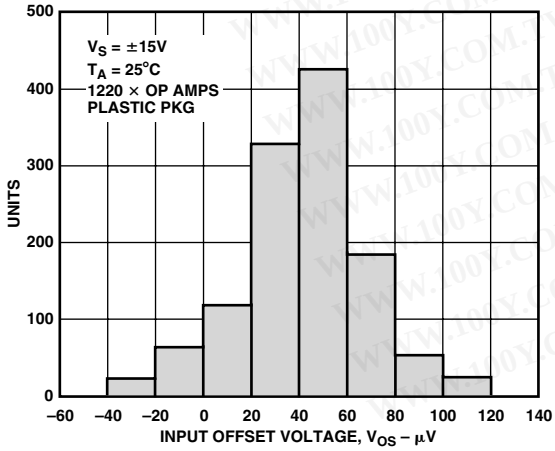
TPC 2a. OP113 Temperature Drift (TCV_{OS}) Distribution @ ±15 V



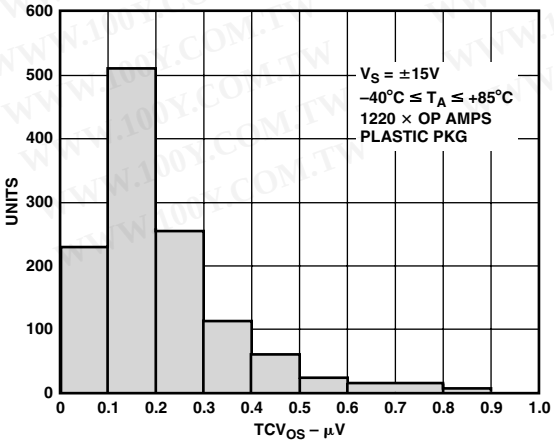
TPC 1b. OP213 Input Offset (V_{OS}) Distribution @ ±15 V



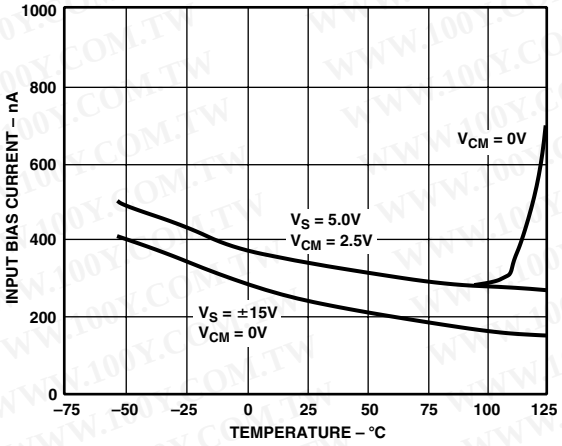
TPC 2b. OP213 Temperature Drift (TCV_{OS}) Distribution @ ±15 V



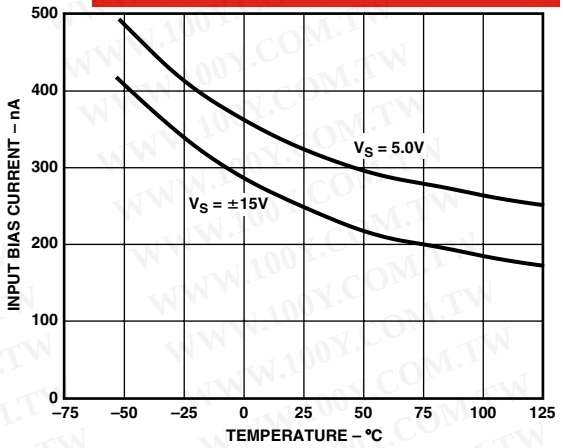
TPC 1c. OP413 Input Offset (V_{OS}) Distribution @ ±15 V



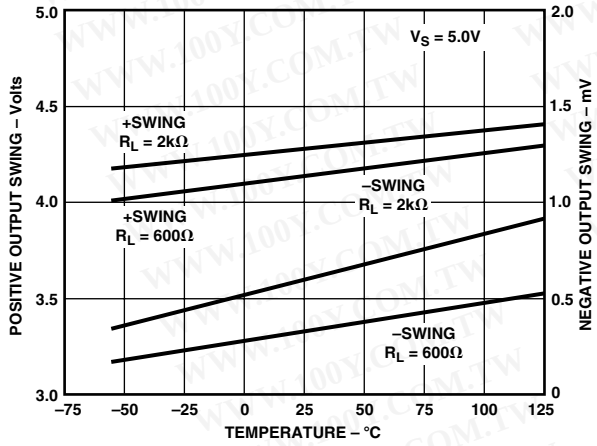
TPC 2c. OP413 Temperature Drift (TCV_{OS}) Distribution @ ±15 V



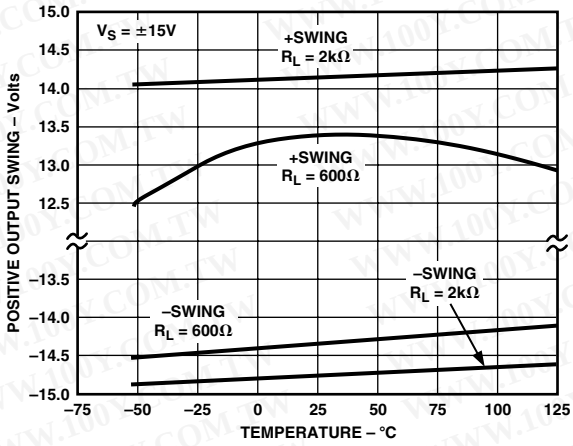
TPC 3. OP113 Input Bias Current vs. Temperature



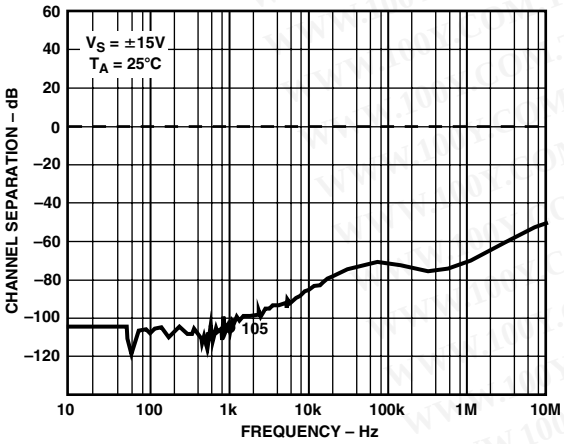
TPC 6. OP213 Input Bias Current vs. Temperature



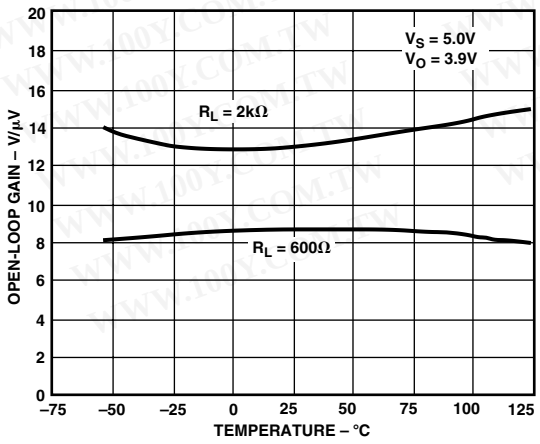
TPC 4. Output Swing vs. Temperature and R_L @ 5 V



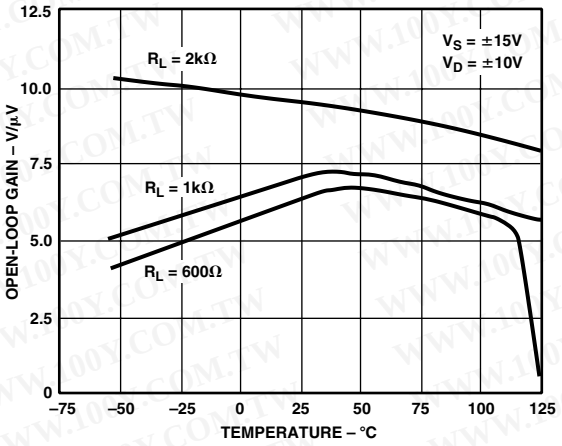
TPC 7. Output Swing vs. Temperature and R_L @ ±15 V



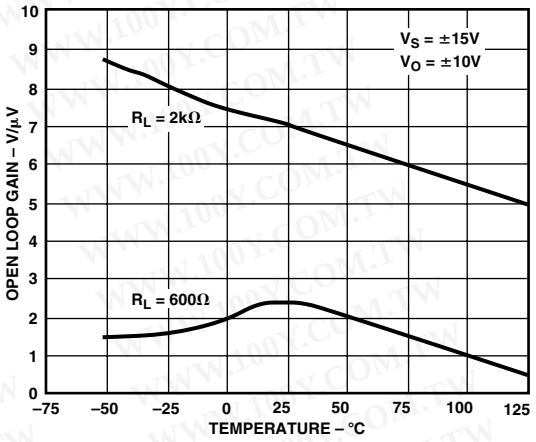
TPC 5. Channel Separation



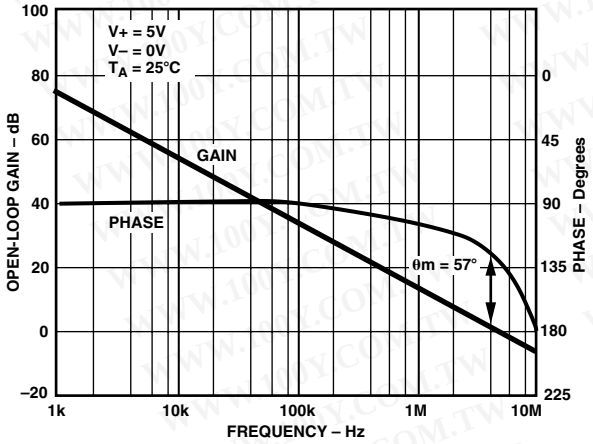
TPC 8. Open-Loop Gain vs. Temperature @ 5 V



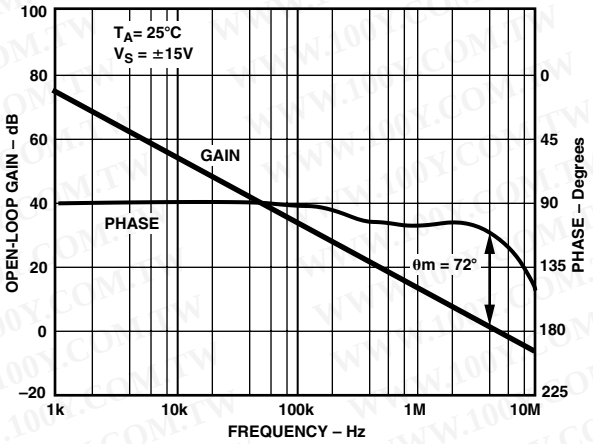
TPC 9. OP413 Open-Loop Gain vs. Temperature



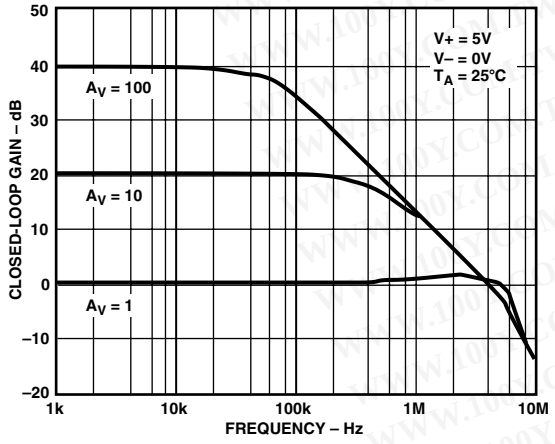
TPC 12. OP213 Open-Loop Gain vs. Temperature



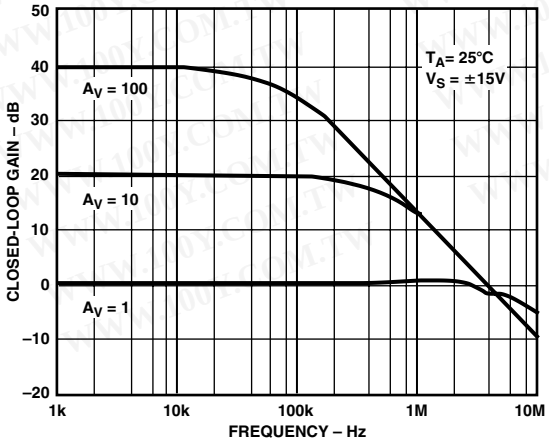
TPC 10. Open-Loop Gain, Phase vs. Frequency @ 5 V



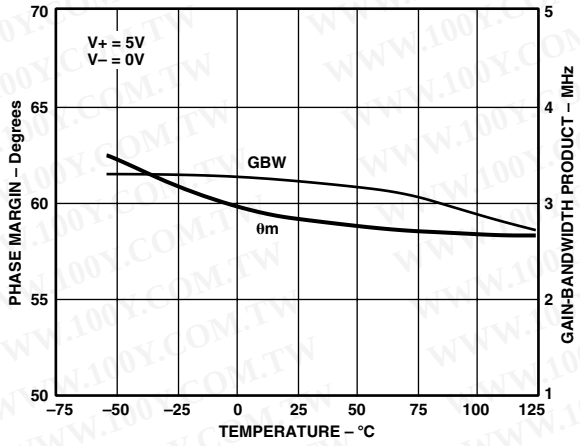
TPC 13. Open-Loop Gain, Phase vs. Frequency @ ±15 V



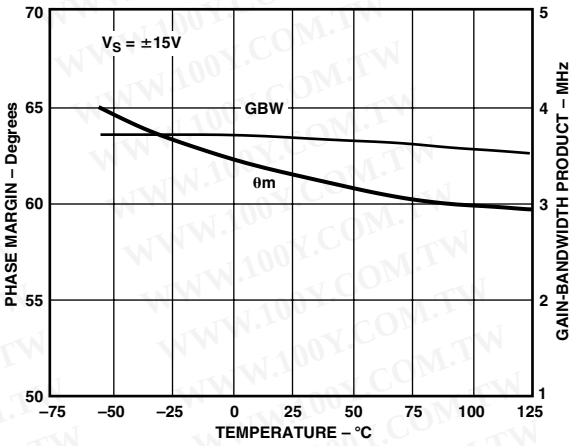
TPC 11. Closed-Loop Gain vs. Frequency @ 5 V



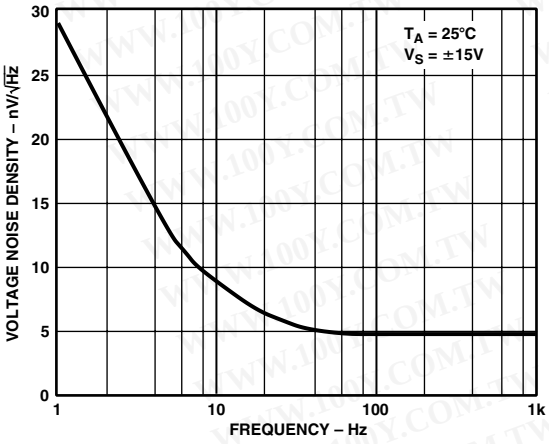
TPC 14. Closed-Loop Gain vs. Frequency @ ±15 V



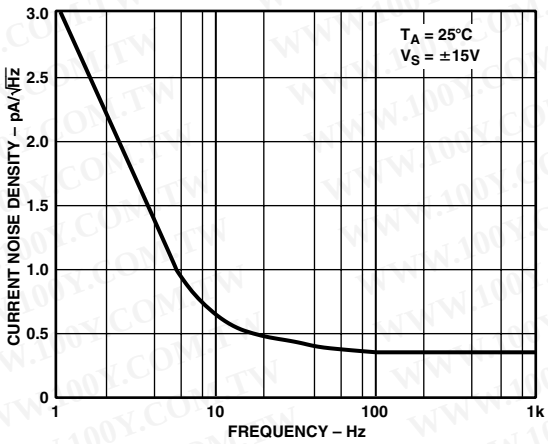
TPC 15. Gain Bandwidth Product and Phase Margin vs. Temperature @ 5 V



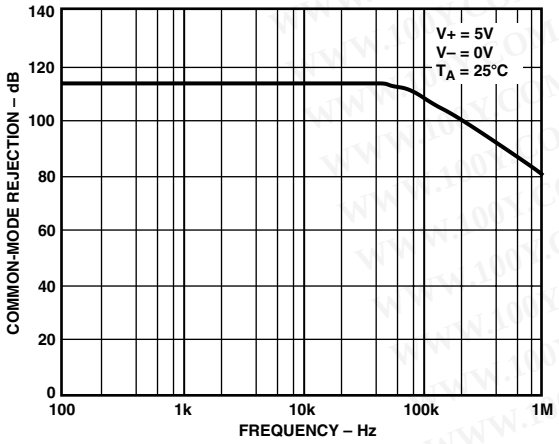
TPC 18. Gain Bandwidth Product and Phase Margin vs. Temperature @ ±15 V



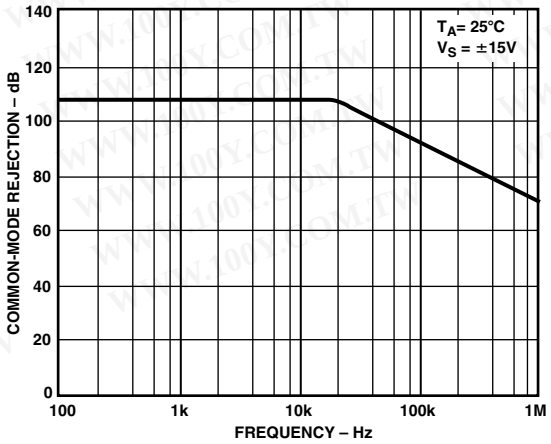
TPC 16. Voltage Noise Density vs. Frequency



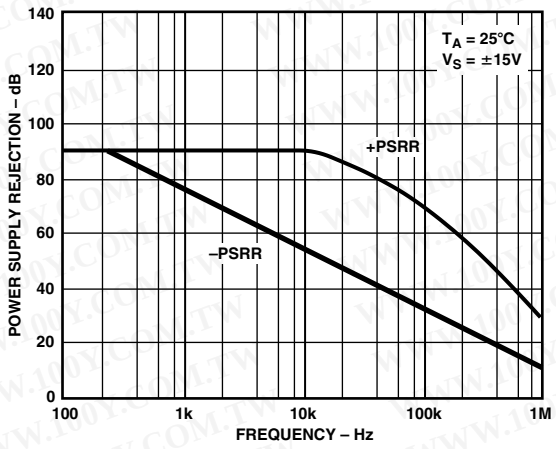
TPC 19. Current Noise Density vs. Frequency



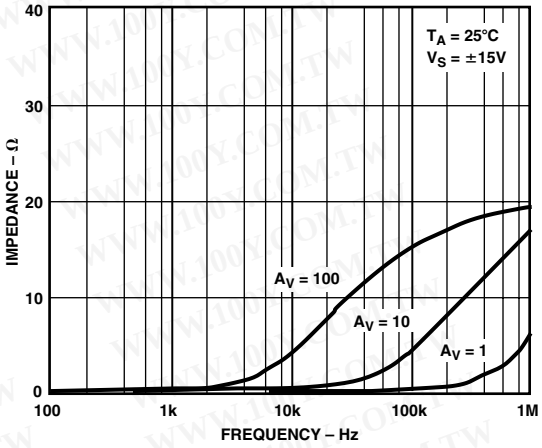
TPC 17. Common-Mode Rejection vs. Frequency @ 5 V



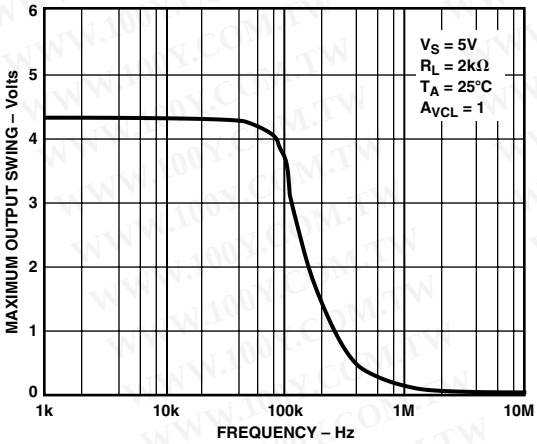
TPC 20. Common-Mode Rejection vs. Frequency @ ±15 V



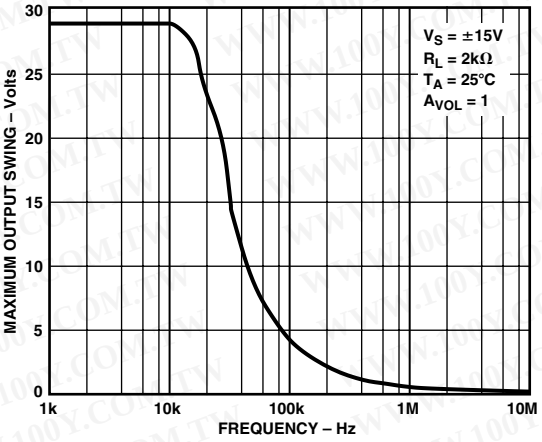
TPC 21. Power Supply Rejection vs. Frequency @ ±15 V



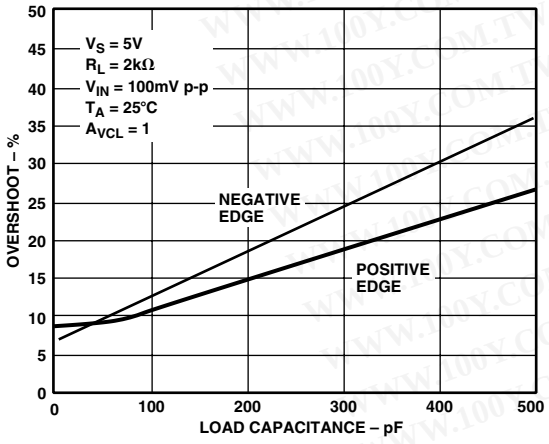
TPC 24. Closed-Loop Output Impedance vs. Frequency @ ±15 V



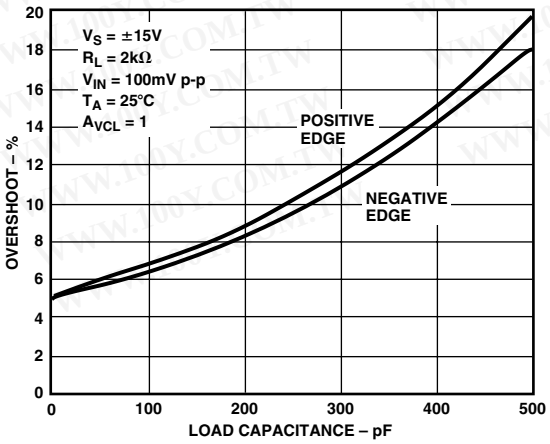
TPC 22. Maximum Output Swing vs. Frequency @ 5 V



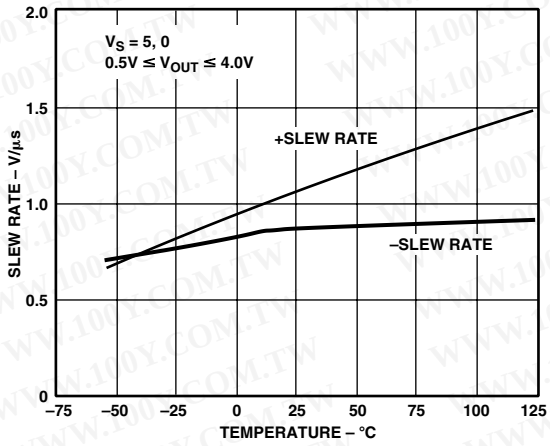
TPC 25. Maximum Output Swing vs. Frequency @ ±15 V



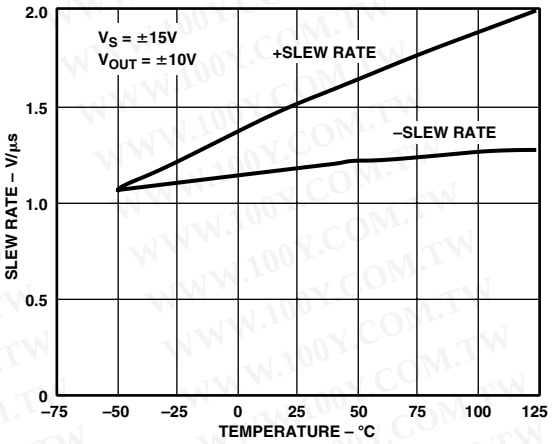
TPC 23. Small Signal Overshoot vs. Load Capacitance @ 5 V



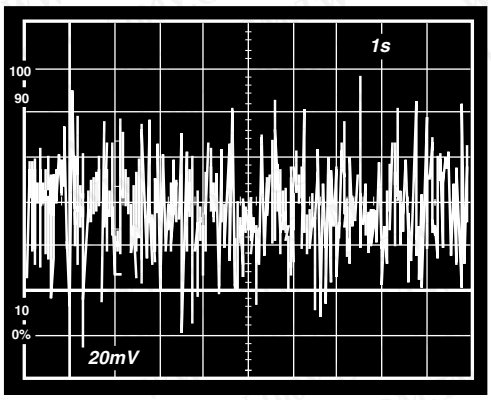
TPC 26. Small Signal Overshoot vs. Load Capacitance @ ±15 V



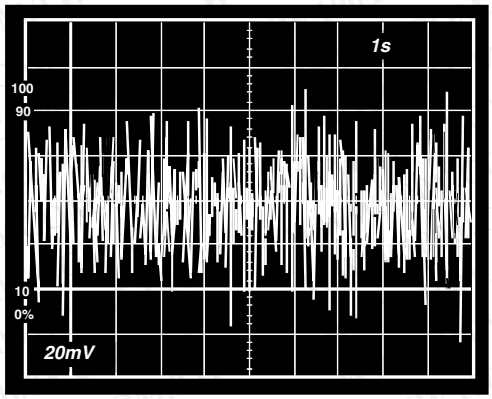
TPC 27. Slew Rate vs. Temperature @ 5 V (0.5 V ≤ V_{OUT} ≤ 4.0 V)



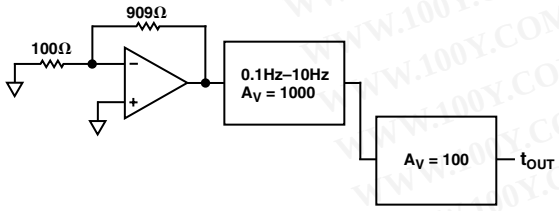
TPC 30. Slew Rate vs. Temperature @ ±15 V (–10 V ≤ V_{OUT} ≤ +10.0 V)



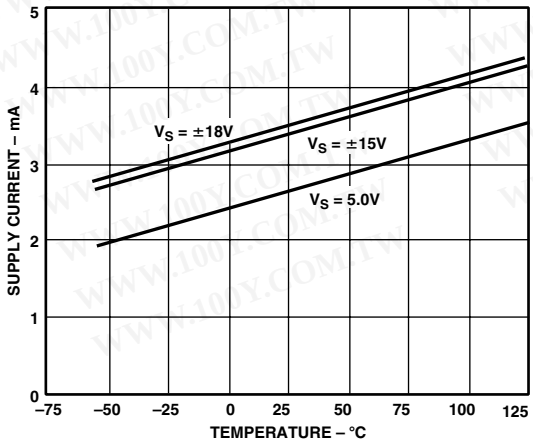
TPC 28. Input Voltage Noise @ ±15 V (20 nV/div)



TPC 31. Input Voltage Noise @ 5 V (20 nV/div)



TPC 29. Noise Test Diagram



TPC 32. Supply Current vs. Temperature

APPLICATIONS

The OP113, OP213, and OP413 form a new family of high performance amplifiers that feature precision performance in standard dual supply configurations and, more importantly, maintain precision performance when a single power supply is used. In addition to accurate dc specifications, it is the lowest noise single supply amplifier available with only 4.7 nV/$\sqrt{\text{Hz}}$ typical noise density.

Single supply applications have special requirements due to the generally reduced dynamic range of the output signal. Single supply applications are often operated at voltages of 5 V or 12 V, compared to dual supply applications with supplies of ±12 V or ±15 V. This results in reduced output swings. Where a dual supply application may often have 20 V of signal output swing, single supply applications are limited to, at most, the supply range and, more commonly, several volts below the supply. In order to attain the greatest swing, the single supply output stage must swing closer to the supply rails than in dual supply applications.

The OP113 family has a new patented output stage that allows the output to swing closer to ground, or the negative supply, than previous bipolar output stages. Previous op amps had outputs that could swing to within about ten millivolts of the negative supply in single supply applications. However, the OP113 family combines both a bipolar and a CMOS device in the output stage, enabling it to swing to within a few hundred microvolts of ground.

When operating with reduced supply voltages, the input range is also reduced. This reduction in signal range results in reduced signal-to-noise ratio, for any given amplifier. There are only two ways to improve this: increase the signal range or reduce the noise. The OP113 family addresses both of these parameters. Input signal range is from the negative supply to within one volt of the positive supply over the full supply range. Competitive parts have input ranges that are a half a volt to five volts less than this. Noise has also been optimized in the OP113 family. At 4.7 nV/$\sqrt{\text{Hz}}$, it is less than one fourth that of competitive devices.

Phase Reversal

The OP113 family is protected against phase reversal as long as both of the inputs are within the supply ranges. However, if there is a possibility of either input going below the negative supply (or ground in the single supply case), the inputs should be protected with a series resistor to limit input current to 2 mA.

OP113 Offset Adjust

The OP113 has the facility for external offset adjustment, using the industry standard arrangement. Pins 1 and 5 are used in conjunction with a potentiometer of 10 kΩ total resistance, connected with the wiper to V– (or ground in single supply applications). The total adjustment range is about ±2 mV using this configuration.

Adjusting the offset to zero has minimal effect on offset drift (assuming the potentiometer has a tempco of less than 1000 ppm/°C). Adjustment away from zero, however, (like all bipolar amplifiers) will result in a TCV_{OS} of approximately 3.3 µV/°C for every millivolt of induced offset.

It is therefore not generally recommended that this trim be used to compensate for system errors originating outside of the OP113. The initial offset of the OP113 is low enough that external trimming is almost never required but, if necessary, the 2 mV trim range may be somewhat excessive. Reducing the trimming potentiometer to a 2 kΩ value will give a more reasonable range of ±400 µV.

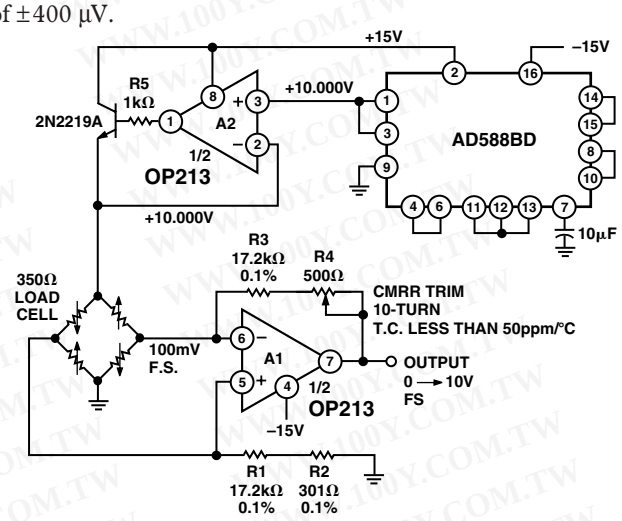


Figure 1. Precision Load Cell Scale Amplifier

APPLICATION CIRCUITS

A High Precision Industrial Load-Cell Scale Amplifier

The OP113 family makes an excellent amplifier for conditioning a load-cell bridge. Its low noise greatly improves the signal resolution, allowing the load cell to operate with a smaller output range, thus reducing its nonlinearity. Figure 1 shows one half of the OP113 family used to generate a very stable 10.000 V bridge excitation voltage while the second amplifier provides a differential gain. R4 should be trimmed for maximum common-mode rejection.

A Low Voltage Single Supply, Strain-Gage Amplifier

The true zero swing capability of the OP113 family allows the amplifier in Figure 2 to amplify the strain-gage bridge accurately even with no signal input while being powered by a single 5 V supply. A stable 4.000 V bridge voltage is made possible by the rail-to-rail OP295 amplifier, whose output can swing to within a millivolt of either rail. This high voltage swing greatly increases the bridge output signal without a corresponding increase in bridge input.

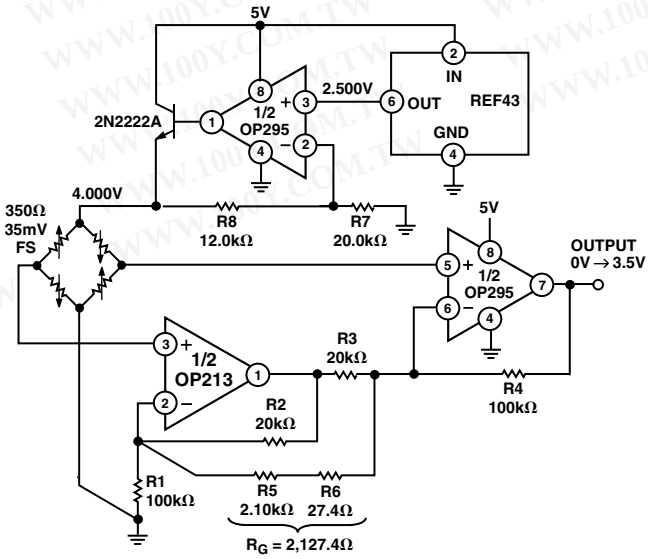


Figure 2. Single Supply Strain-Gage Amplifier

A High Accuracy Linearized RTD Thermometer Amplifier

Zero suppressing the bridge facilitates simple linearization of the RTD by feeding back a small amount of the output signal to the RTD (Resistor Temperature Device). In Figure 3, the left leg of the bridge is servoed to a virtual ground voltage by amplifier A1, while the right leg of the bridge is also servoed to zero volt by amplifier A2. This eliminates any error resulting from common-mode voltage change in the amplifier. A 3-wire RTD is used to balance the wire resistance on both legs of the bridge, thereby reducing temperature mismatch errors. The 5.000 V bridge excitation is derived from the extremely stable AD588 reference device with 1.5 ppm/°C drift performance.

Linearization of the RTD is done by feeding a fraction of the output voltage back to the RTD in the form of a current. With just the right amount of positive feedback, the amplifier output will be linearly proportional to the temperature of the RTD.

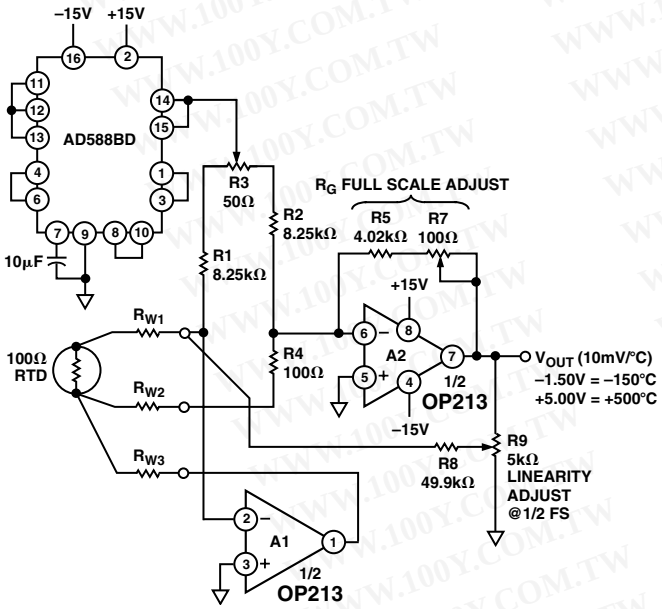


Figure 3. Ultraprecision RTD Amplifier

To calibrate the circuit, first immerse the RTD in a zero-degree ice bath or substitute an exact 100 Ω resistor in place of the RTD. Adjust the ZERO ADJUST potentiometer for a 0.000 V output, then set R9 LINEARITY ADJUST potentiometer to the middle of its adjustment range. Substitute a 280.9 Ω resistor (equivalent to 500°C) in place of the RTD, and adjust the FULL-SCALE ADJUST potentiometer for a full-scale voltage of 5.000 V.

To calibrate out the nonlinearity, substitute a 194.07 Ω resistor (equivalent to 250°C) in place of the RTD, then adjust the LINEARITY ADJUST potentiometer for a 2.500 V output. Check and readjust the full-scale and half-scale as needed.

Once calibrated, the amplifier outputs a 10 mV/°C temperature coefficient with an accuracy better than ±0.5°C over an RTD measurement range of –150°C to +500°C. Indeed the amplifier can be calibrated to a higher temperature range, up to 850°C.

A High Accuracy Thermocouple Amplifier

Figure 4 shows a popular K-type thermocouple amplifier with cold-junction compensation. Operating from a single 12 V supply, the OP113 family's low noise allows temperature measurement to better than 0.02°C resolution from 0°C to 1000°C range. The cold-junction error is corrected by using an inexpensive silicon diode as a temperature measuring device. It should be placed as close to the two terminating junctions as physically possible. An aluminum block might serve well as an isothermal system.

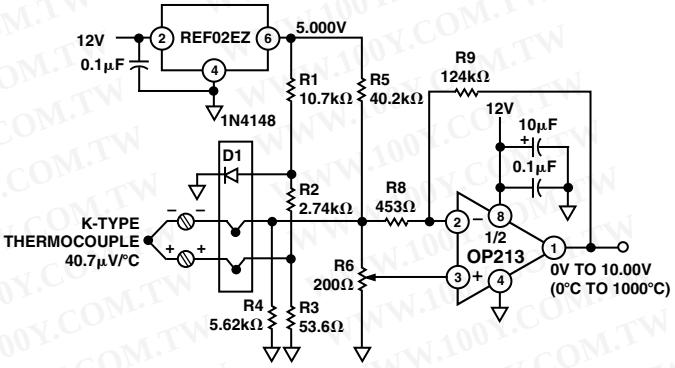


Figure 4. Accurate K-Type Thermocouple Amplifier

R6 should be adjusted for a zero-volt output with the thermocouple measuring tip immersed in a zero-degree ice bath. When calibrating, be sure to adjust R6 initially to cause the output to swing in the positive direction first. Then back off in the negative direction until the output just stops changing.

An Ultralow Noise, Single Supply Instrumentation Amplifier

Extremely low noise instrumentation amplifiers can be built using the OP113 family. Such an amplifier that operates off a single supply is shown in Figure 5. Resistors R1–R5 should be of high precision and low drift type to maximize CMRR performance. Although the two inputs are capable of operating to zero volt, the gain of –100 configuration will limit the amplifier input common mode to not less than 0.33 V.

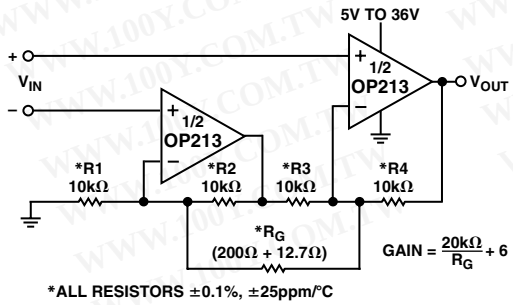


Figure 5. Ultralow Noise, Single Supply Instrumentation Amplifier

Supply Splitter Circuit

The OP113 family has excellent frequency response characteristic that makes it an ideal pseudo-ground reference generator as shown in Figure 6. The OP113 family serves as a voltage follower buffer. In addition, it drives a large capacitor that serves as a charge reservoir to minimize transient load changes, as well as a low impedance output device at high frequencies. The circuit easily supplies 25 mA load current with good settling characteristics.

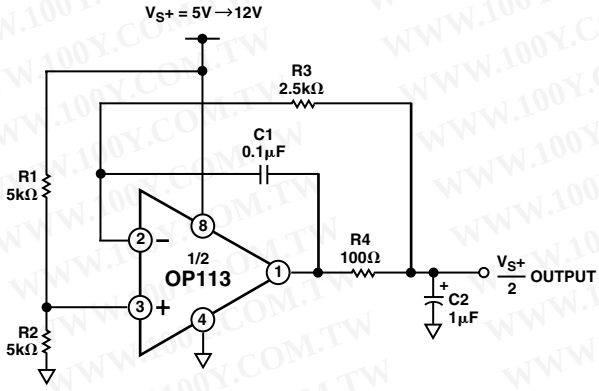


Figure 6. False Ground Generator

Low Noise Voltage Reference

Few reference devices combine low noise and high output drive capabilities. Figure 7 shows the OP113 family used as a two-pole active filter that band limits the noise of the 2.500 V reference. Total noise measures 3 µV p-p.

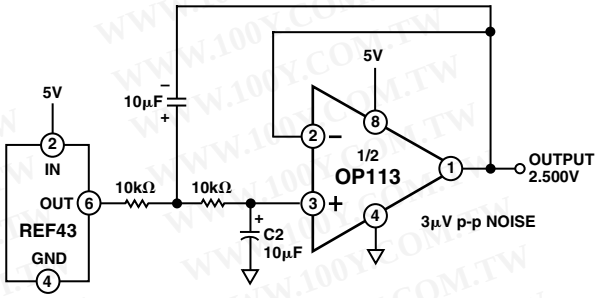


Figure 7. Low Noise Voltage Reference

5 V Only Stereo DAC for Multimedia

The OP113 family's low noise and single supply capability are ideally suited for stereo DAC audio reproduction or sound synthesis applications such as multimedia systems. Figure 8 shows an 18-bit stereo DAC output setup that is powered from a single 5 V supply. The low noise preserves the 18-bit dynamic range of the AD1868. For DACs that operate on dual supplies, the OP113 family can also be powered from the same supplies.

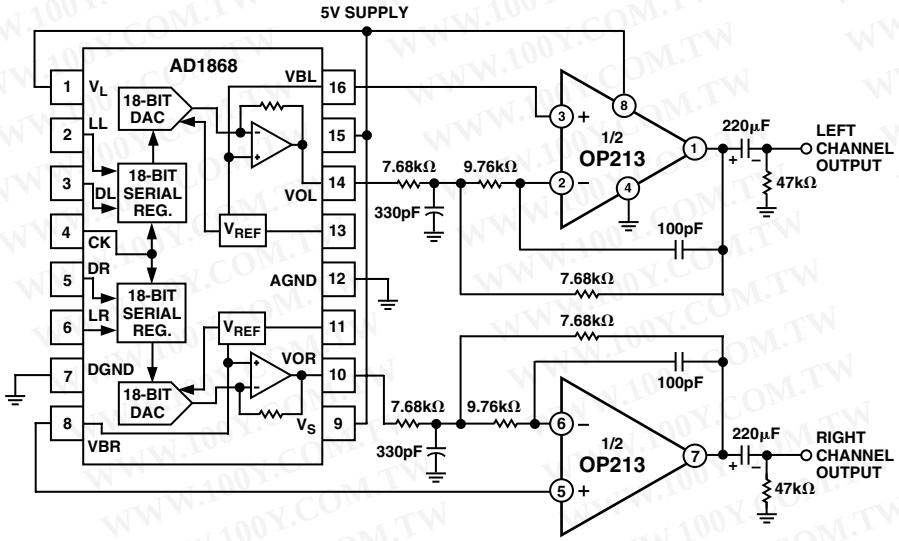


Figure 8. 5 V Only 18-Bit Stereo DAC

SoundPort is a registered trademark of Analog Devices, Inc.

Low Voltage Headphone Amplifiers

Figure 9 shows a stereo headphone output amplifier for the AD1849 16-bit SoundPort® Stereo Codec device. The pseudo-reference voltage is derived from the common-mode voltage generated internally by the AD1849, thus providing a convenient bias for the headphone output amplifiers.

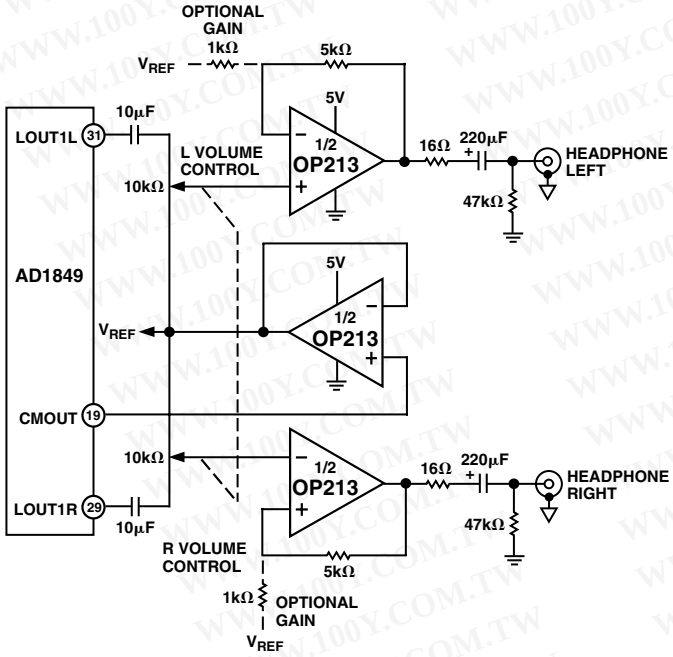


Figure 9. Headphone Output Amplifier for Multimedia Sound Codec

Low Noise Microphone Amplifier for Multimedia

The OP113 family is ideally suited as a low noise microphone preamp for low voltage audio applications. Figure 10 shows a gain of 100 stereo preamp for the AD1849 16-bit SoundPort Stereo Codec chip. The common-mode output buffer serves as a "phantom power" driver for the microphones.

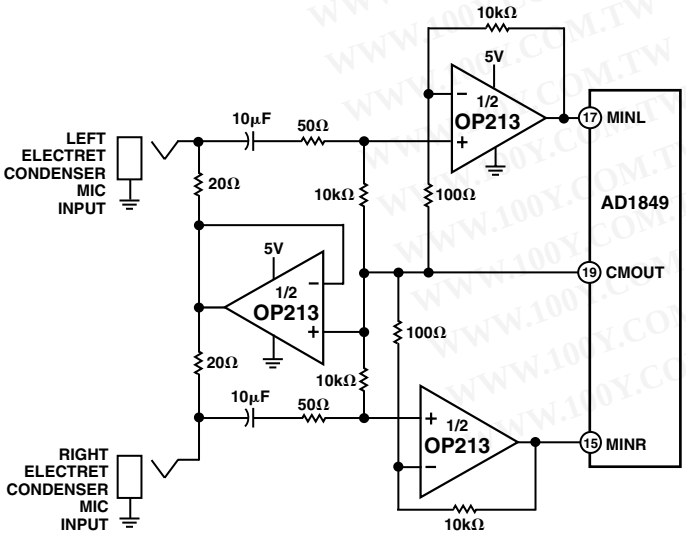


Figure 10. Low Noise Stereo Microphone Amplifier for Multimedia Sound Codec

Precision Voltage Comparator

With its PNP inputs and zero volt common-mode capability, the OP113 family can make useful voltage comparators. There is only a slight penalty in speed in comparison to IC comparators. However, the significant advantage is its voltage accuracy. For example, V_{OS} can be a few hundred microvolts or less, combined with CMRR and PSRR exceeding 100 dB, while operating on 5 V supply. Standard comparators like the 111/311 family operate on 5 V, but not with common-mode at ground, nor with offset below 3 mV. Indeed, no commercially available single supply comparator has a V_{OS} less than 200 µV.

Figure 11 shows the OP113 family response to a 10 mV overdrive signal when operating in open loop. The top trace shows the output rising edge has a 15 µs propagation delay, while the bottom trace shows a 7 µs delay on the output falling edge. This ac response is quite acceptable in many applications.

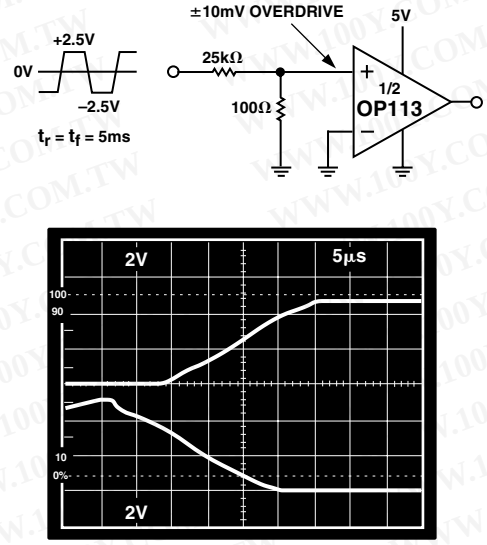


Figure 11. Precision Comparator

The low noise and 250 µV (maximum) offset voltage enhance the overall dc accuracy of this type of comparator. Note that zero crossing detectors and similar ground referred comparisons can be implemented even if the input swings to –0.3 V below ground.

SoundPort is a registered trademark of Analog Devices, Inc.

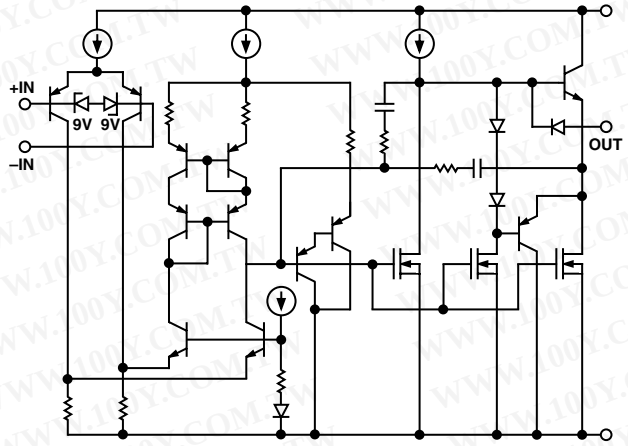


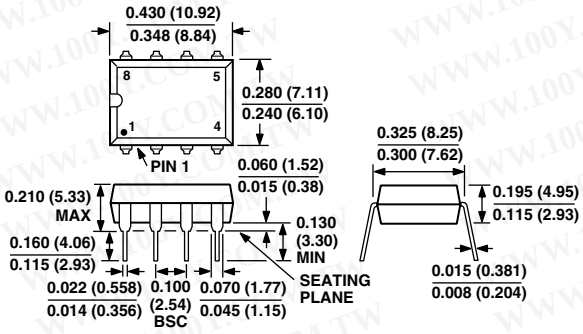
Figure 12. OP213 Simplified Schematic

```
*OP113 Family SPICE Macro-Model
*
*Copyright 1992 by Analog Devices, Inc.
*
*Node Assignments
*
*                              Noninverting Input
*                                 Inverting Input
*                                    Positive Supply
*                                       Negative Supply
*                                          Output
*
.SUBCKT OP113 Family      3  2  7  4  6
*
* INPUT STAGE
R3      4   19   1.5E3
R4      4   20   1.5E3
C1      19  20   5.31E–12
I1      7   18   106E–6
IOS     2   3    25E–09
EOS     12  5    POLY(1)   51   4      25E–06  1
Q1      19  3    18   PNP1
Q2      20  12   18   PNP1
CIN     3   2    3E–12
D1      3   1    DY
D2      2   1    DY
EN      5   2    22   0      1
GN1     0   2    25   0      1E–5
GN2     0   3    28   0      1E–5
*
* VOLTAGE NOISE SOURCE WITH FLICKER NOISE
DN1     21  22   DEN
DN2     22  23   DEN
VN1     21  0    DC 2
VN2     0   23   DC 2
*
* CURRENT NOISE SOURCE WITH FLICKER NOISE
DN3     24  25   DIN
DN4     25  26   DIN
VN3     24  0    DC 2
VN4     0   26   DC 2
*
* SECOND CURRENT NOISE SOURCE
DN5     27  28   DIN
DN6     28  29   DIN
VN5     27  0    DC 2
VN6     0   29   DC 2
*
* GAIN STAGE & DOMINANT POLE AT .2000E+01 HZ
G2      34  36   19   20   2.65E–04
R7      34  36   39E+06
V3      35  4    DC   6
D4      36  35   DX
VB2     34  4    1.6
*
* SUPPLY/2 GENERATOR
ISY     7   4    0.2E–3
R10     7   60   40E+3
R11     60  4    40E+3
C3      60  0    1E–9
*
* CMRR STAGE & POLE AT 6 kHZ
ECM   50  4    POLY(2) 3 BŒ 60   2    60   0    1.6  0    1.6
CCM   50  51   26.5E–12
RCM1  50  51   1E6
RCM2  51  4    1
*
*
OUTPUT STAGE
R12     37  36   1E3
R13     38  36   500
C4      37  6    20E–12
C5      38  39   20E–12
M1      39  36   4 4 MN L=9E–6 W=1000E–6 AD=15E–9 AS=15E–9
M2      45  36   4 4 MN L=9E–6 W=1000E–6 AD=15E–9 AS=15E–9
D5      39  47   DX
D6      47  45   DX
Q3      39  40   41   QPA 8
VB      7   40   DC   0.861
R14     7   41   375
Q4      41  7    43   QNA 1
R17     7   43   15
Q5      43  39   6    QNA 20
Q6      46  45   6    QPA 20
R18     46  4    15
Q7      36  46   4    QNA 1
M3      6   36   4 4 MN L = 9E–6 W=2000E–6 AD=30E–9 AS=30E–9
*
* NONLINEAR MODELS USED
*
.MODEL DX D (IS=1E–15)
.MODEL DY D (IS=1E–15 BV=7)
.MODEL PNP1 PNP (BF=220)
.MODEL DEN D(IS=1E–12 RS=1016 KF=3.278E–15 AF=1)
.MODEL DIN D(IS=1E–12 RS=100019 KF=4.173E–15 AF=1)
.MODEL QNA NPN(IS=1.19E–16 BF=253 VAF=193 VAR=15 RB=2.0E3
+ IRB=7.73E–6 RBM=132.8 RE=4 RC=209 CJE=2.1E–13 VJE=0.573
+ MJE=0.364 CJC=1.64E–13 VJC=0.534 MJC=0.5 CJS=1.37E–12
+ VJS=0.59 MJS=0.5 TF=0.43E–9 PTF=30)
.MODEL QPA PNP(IS=5.21E–17 BF=131 VAF=62 VAR= 15 RB=1.52E3
+ IRB=1.67E–5 RBM=368.5 RE=6.31 RC=354.4 CJE=1.1E–13
+ VJE=0.745 MJE=0.33 CJC=2.37E–13 VJC=0.762 MJC=0.4
+ CJS=7.11E–13 VJS=0.45 MJS=0.412 TF=1.0E–9 PTF=30)
.MODEL MN NMOS(LEVEL=3 VTO=1.3 RS=0.3 RD=0.3 TOX=8.5E–8
+ LD=1.48E–6 WD=1E–6 NSUB=1.53E16 UO=650 DELTA=10 VMAX=2E5
+ XJ=1.75E–6 KAPPA=0.8 ETA=0.066 THETA=0.01 TPG=1 CJ=2.9E–4
+ PB=0.837 MJ=0.407 CJSW=0.5E–9 MJSW=0.33)
*
.ENDS OP113 Fa
```

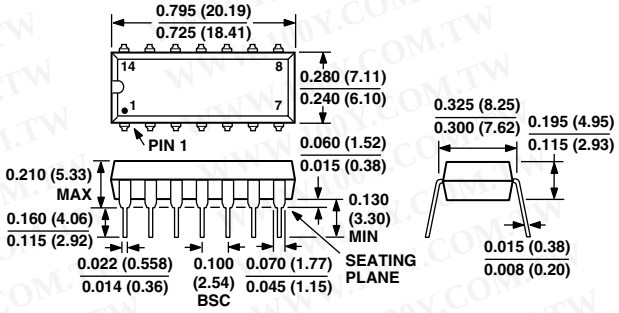
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

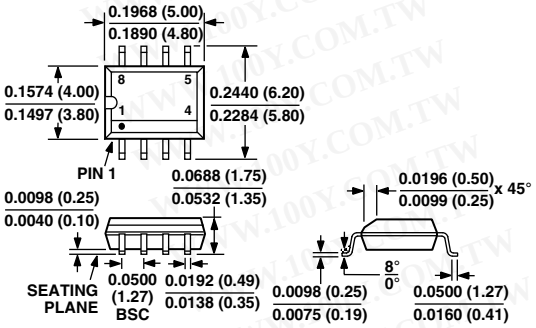
8-Lead Plastic DIP (N-8)



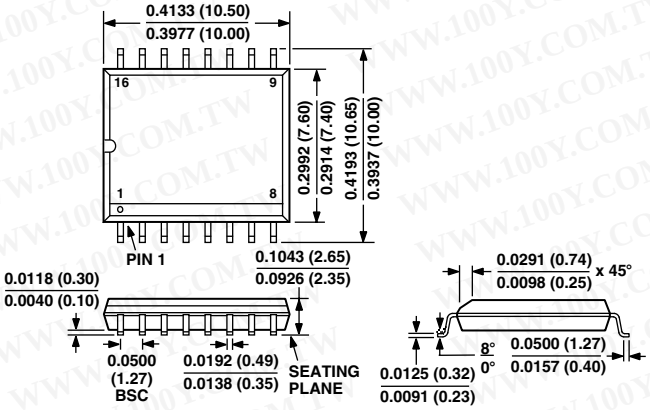
14-Lead Plastic DIP (N-14)



8-Lead Narrow-Body Plastic DIP (SO-8)



16-Lead Wide Body SOIC (R-16)



Revision History

Location	Page
9/01—Data Sheet changed from REV. C to REV. D.	
Edits to ORDERING GUIDE	4

C00286–0–1/02(D)

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