# PA05 • PA05A



## FEATURES

- HIGH INTERNAL DISSIPATION — 250 WATTS
- HIGH VOLTAGE, HIGH CURRENT — 100V, 30A
- HIGH SLEW RATE — 100V/μS
- 4 WIRE CURRENT LIMIT SENSING
- LOW DISTORTION
- EXTERNAL SHUTDOWN CONTROL
- OPTIONAL BOOST VOLTAGE INPUTS
- EVALUATION KIT — SEE EK04

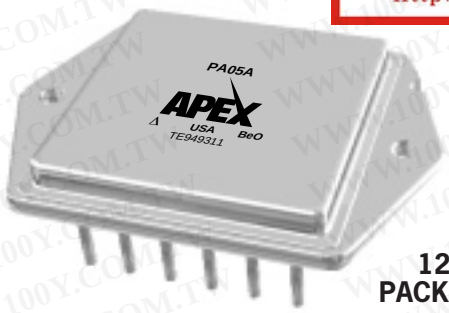
## APPLICATIONS

- LINEAR AND ROTARY MOTOR DRIVES
- SONAR TRANSDUCER DRIVER
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±45V
- AUDIO UP TO 500W

## DESCRIPTION

The PA05 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

The PA05 is a highly flexible amplifier. The shutdown control feature allows the output stage to be turned off for standby operation or load protection during fault conditions. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors slew rate and bandwidth performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external milliohm parasitic resistance in the output line. The output stage is protected by thermal limiting circuits above junction temperatures of 175°C.

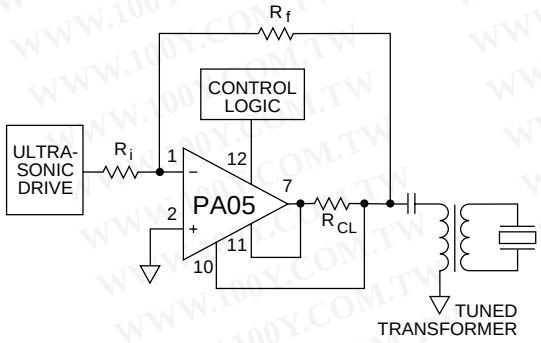



**12-pin Power DIP**
**PACKAGE STYLE CR**

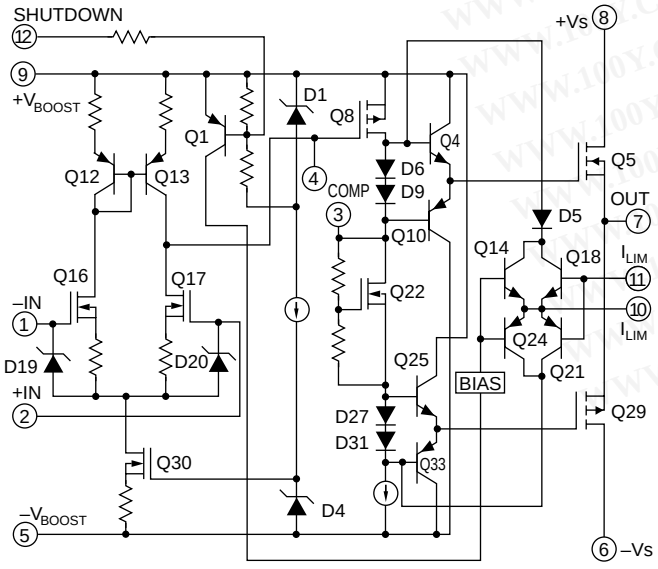
The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

## TYPICAL APPLICATION

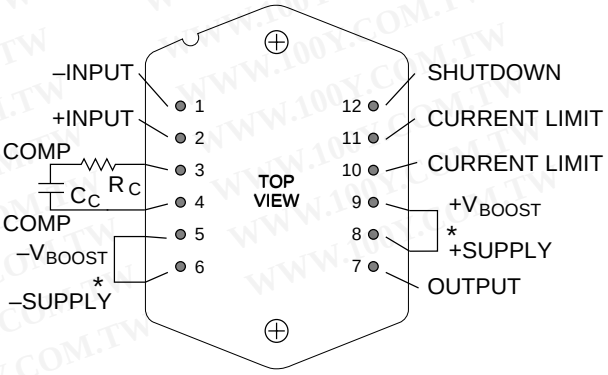
The high power bandwidth of the PA05 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA05. Control logic turns off the amplifier's output during shutdown.




## EQUIVALENT SCHEMATIC




## EXTERNAL CONNECTIONS




### PHASE COMPENSATION

| Gain | $C_C$ | $R_C$ |
|---|---|---|
| 1 | 470pF | 120Ω |
| >3 | 220pF | 120Ω |
| ≥10 | 82pF | 120Ω |

**$C_C$ RATED FOR FULL SUPPLY VOLTAGE**

*See *BOOST OPERATION* paragraph.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| SUPPLY VOLTAGE, $+V_S$ to $-V_S$ | 100V |
| BOOST VOLTAGE | SUPPLY VOLTAGE +20V |
| OUTPUT CURRENT, continuous within SOA | 30A |
| POWER DISSIPATION, internal | 250W |
| INPUT VOLTAGE, differential | ±20V |
| INPUT VOLTAGE, common mode | $\pm V_B$ |
| TEMPERATURE, pin solder - 10s | 300°C |
| TEMPERATURE, junction[2] | 175°C |
| TEMPERATURE, storage | –65 to +150°C |
| OPERATING TEMPERATURE RANGE, case | –55 to +125°C |

## SPECIFICATIONS

| | | PA05 | | | PA05A | | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS[1]** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **INPUT** | | | | | | | | |
| OFFSET VOLTAGE, initial | | | 5 | 10 | | 2 | 5 | mV |
| OFFSET VOLTAGE, vs. temperature | Full temperature range | | 20 | 50 | | 10 | 30 | µV/°C |
| OFFSET VOLTAGE, vs. supply | | | 10 | 30 | | * | * | µV/V |
| OFFSET VOLTAGE, vs. power | Full temperature range | | 30 | | | 10 | | µV/W |
| BIAS CURRENT, initial | | | 10 | 50 | | 5 | 20 | pA |
| BIAS CURRENT, vs. supply | | | .01 | | | * | | pA/V |
| OFFSET CURRENT, initial | | | 10 | 50 | | 5 | 20 | pA |
| INPUT IMPEDANCE, DC | | | $10^{11}$ | | | * | | Ω |
| INPUT CAPACITANCE | | | 13 | | | * | | pF |
| COMMON MODE VOLTAGE RANGE | Full temperature range | $\pm V_B$–8 | | | * | | | V |
| COMMON MODE REJECTION, DC | Full temp. range, $V_{CM}$ = ±20V | 90 | 100 | | * | * | | dB |
| INPUT NOISE | 100KHz BW, $R_S$ = 1KΩ | | 10 | | | * | | µVrms |
| **GAIN** | | | | | | | | |
| OPEN LOOP, @ 15Hz | Full temperature range, $C_C$ = 82pF | 94 | 102 | | * | * | | dB |
| GAIN BANDWIDTH PRODUCT | $R_L$ = 10Ω | | 3 | | | * | | MHz |
| POWER BANDWIDTH | $R_L$ = 4Ω, $V_O$ = 80$V_{P-P}$, $A_V$ = –10 | | 400 | | | * | | kHz |
| | $C_C$ = 82pF, $R_C$ = 120Ω | | | | | | | |
| PHASE MARGIN | Full temperature range, $C_C$ = 470pF | | 60 | | | * | | ° |
| **OUTPUT** | | | | | | | | |
| VOLTAGE SWING | $I_O$ = 20A | $\pm V_S$–9.5 | $\pm V_S$–8.7 | | * | * | | V |
| VOLTAGE SWING | $V_{BOOST}$ = Vs + 5V, $I_O$ = 30A | $\pm V_S$–5.8 | $\pm V_S$–5.0 | | * | * | | V |
| CURRENT, peak | | 30 | | | * | | | A |
| SETTLING TIME to .1% | $A_V$ = +1, 10V step, $R_L$ = 4Ω | | 2.5 | | | * | | µs |
| SLEW RATE | $A_V$ = –10, $C_C$ = 82pF, $R_C$ = 120Ω | 80 | 100 | | | * | | V/µs |
| CAPACITIVE LOAD | Full temperature range, $A_V$ = +1 | 2.2 | | | * | | | nF |
| RESISTANCE | $I_O$ = 0, No load, 2MHz | | 5 | | | * | | Ω |
| | $I_O$ = 1A, 2MHz | | 2 | | | * | | Ω |
| **POWER SUPPLY** | | | | | | | | |
| VOLTAGE | Full temperature range | ±15 | ±45 | ±50 | * | * | * | V |
| CURRENT, quiescent, boost supply | | | 46 | 56 | | * | * | mA |
| CURRENT, quiescent, total | | | 90 | 120 | | * | * | mA |
| CURRENT, quiescent, total, shutdown | | | 46 | 56 | | * | * | mA |
| **THERMAL** | | | | | | | | |
| RESISTANCE, AC, junction to case[3] | Full temperature range, F>60Hz | | .3 | .4 | | * | * | °C/W |
| RESISTANCE, DC, junction to case | Full temperature range, F<60Hz | | .4 | .5 | | * | * | °C/W |
| RESISTANCE, junction to air[4] | Full temperature range | | 12 | | | * | | °C/W |
| TEMPERATURE RANGE, case | Meets full range specification | –25 | | 85 | * | | * | °C |

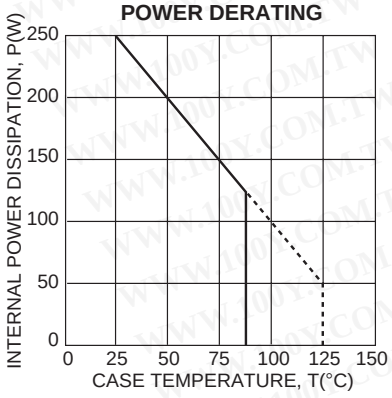
NOTES: * The specification of PA05A is identical to the specification for PA05 in applicable column to the left.
1. Unless otherwise noted: $T_C$ = 25°C, $C_C$ = 470pF, $R_C$ = 120 ohms. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The PA05 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

**CAUTION** The PA05 is constructed from MOSFET transistors. ESD handling procedures must be observed.

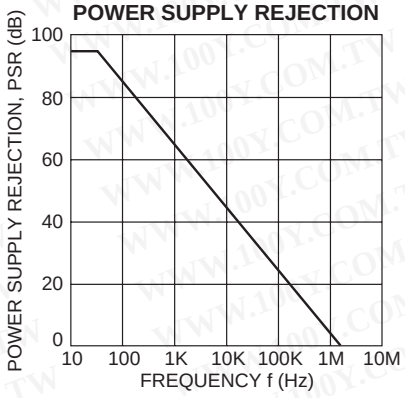
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

## TYPICAL PERFORMANCE GRAPHS

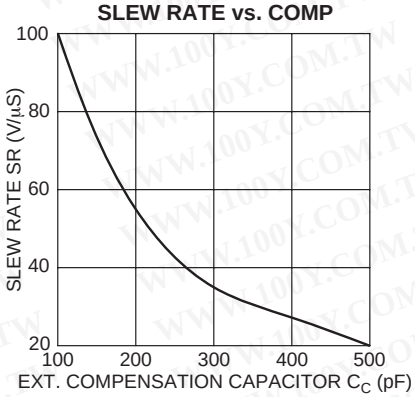
### POWER DERATING



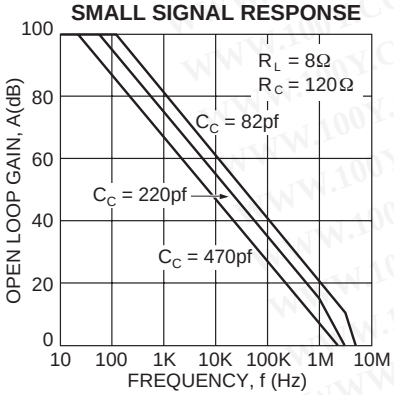

### POWER SUPPLY REJECTION



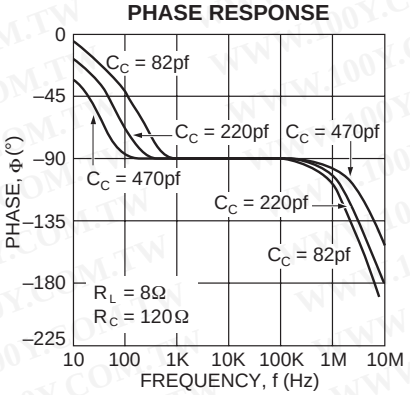

### SLEW RATE vs. COMP



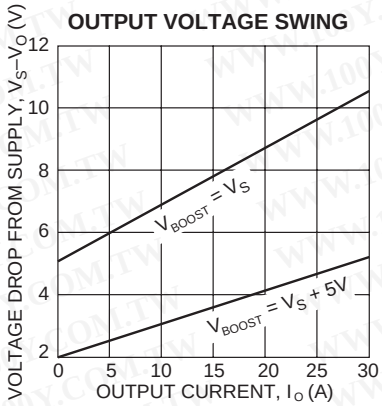

### SMALL SIGNAL RESPONSE



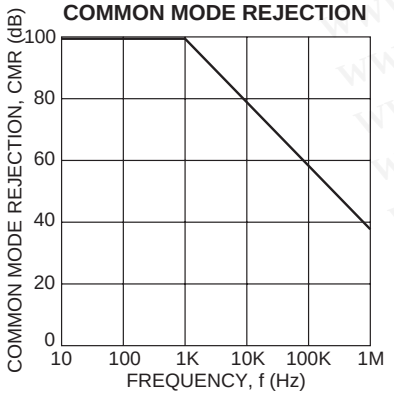

### PHASE RESPONSE



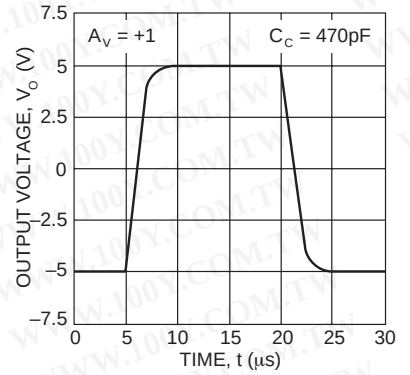

### OUTPUT VOLTAGE SWING



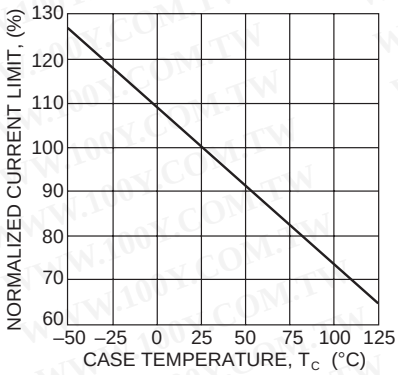

### COMMON MODE REJECTION



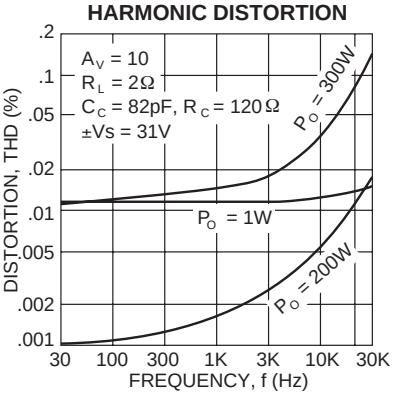

### PULSE RESPONSE



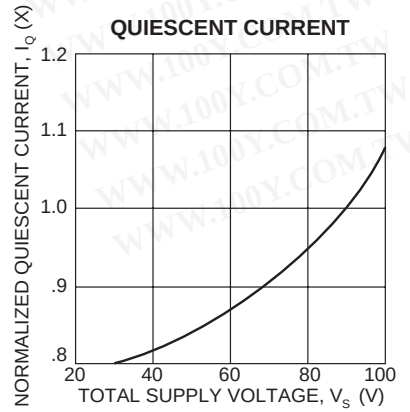

### CURRENT LIMIT



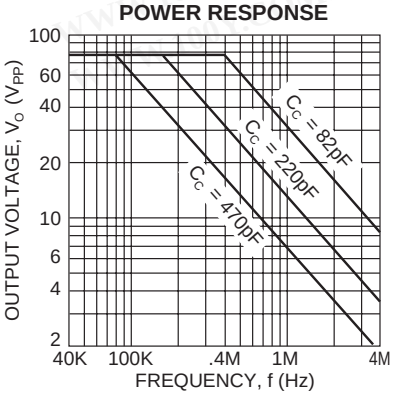

### HARMONIC DISTORTION




### QUIESCENT CURRENT




### POWER RESPONSE



## GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

## CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. *For the current limit to work correctly, pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, $R_{CL}$, as shown in Figure 1.* This connection will bypass any parasitic resistances, $R_P$ formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1. If current limiting is not used, pins 10 and 11 must be tied to pin 7.

The value of the current limit resistor can be calculated as follows:

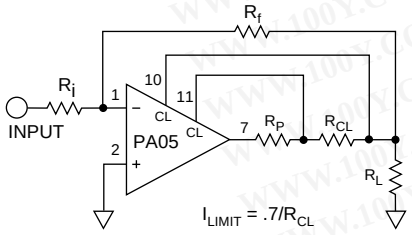


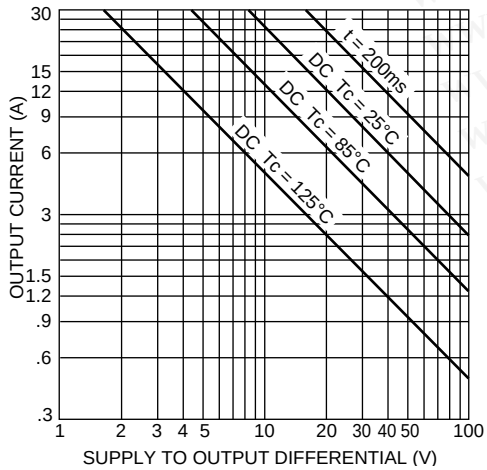

FIGURE 1. CURRENT LIMIT

## SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.




The output stage thermal protection circuit engages when junction temperatures reach approximately 175C. If the condition remains that caused the shutdown, the amplifier may oscillate in and out of shutdown, creating high peak power stresses reducing the reliability of the device.

## SHUTDOWN OPERATION

To disable the output stage, pin 12 is connected to ground via relay contacts or via an electronic switch. The switching device must be capable of sinking 2mA to complete shutdown and capable of standing off the supply voltage $+V_S$. See Figure 2 for suggested circuits.

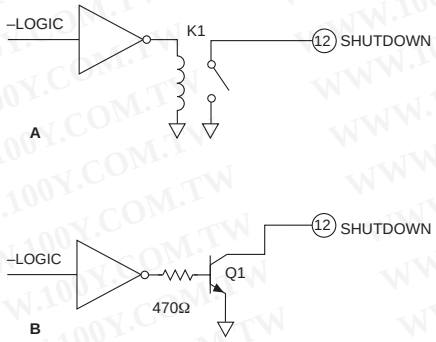



FIGURE 2. SHUTDOWN OPERATION

From an internal circuitry standpoint, shutdown is just a special case of current limit where the allowed output current is zero. As with current limit, however, a small current does flow in the output during shutdown. A load impedance of 100 ohms or less is required to insure the output transistors are turned off. Note that even though the output transistors are off the output pin is not open circuited because of the shutdown operating current.

## BOOST OPERATION

With the $V_{BOOST}$ feature, the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 9), and $–V_{BOOST}$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $–V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the $V_{BOOST}$ pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $–V_{BOOST}$ and $–V_S$ pins. The boost voltage pins must not be at a voltage lower than the $V_S$ pins.

## COMPENSATION

The external compensation components $C_C$ and $R_C$ are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 470 pF with at least 60 degrees of phase margin. At higher gains, more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select $C_C$ and $R_C$ for the application.





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