

# PA10 • PA10A

## FEATURES

- GAIN BANDWIDTH PRODUCT — 4MHz
- TEMPERATURE RANGE —  $-55$  to  $+125^{\circ}\text{C}$  (PA10A)
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE —  $\pm 10\text{V}$  to  $\pm 50\text{V}$
- HIGH OUTPUT CURRENT —  $\pm 5\text{A}$  Peak

## APPLICATIONS

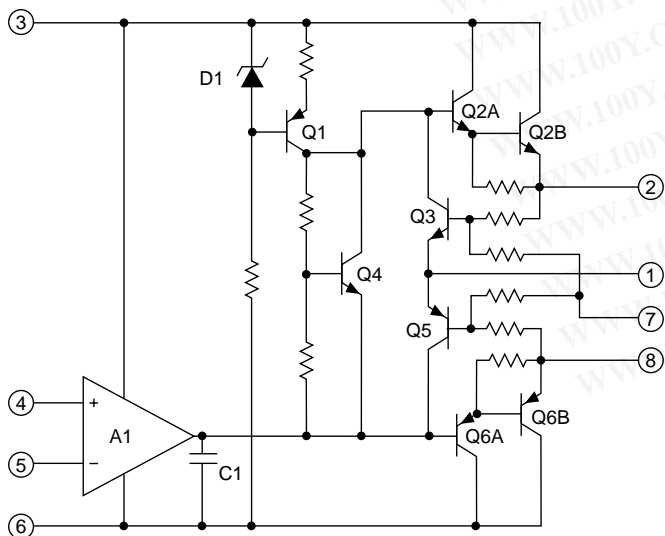
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

## DESCRIPTION

The PA10 and PA10A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

## EQUIVALENT SCHEMATIC



8-pin TO-3  
PACKAGE STYLE CE

## TYPICAL APPLICATION

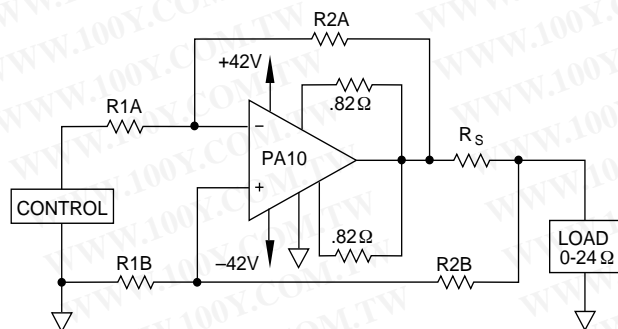
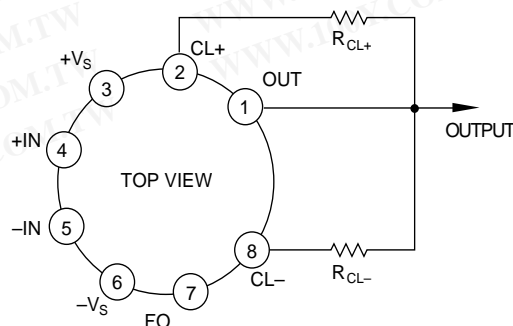


FIGURE 1. VOLTAGE-TO-CURRENT CONVERSION

DC and low distortion AC current waveforms are delivered to a grounded load by using matched resistors (A and B sections) and taking advantage of the high common mode rejection of the PA10.

Foldover current limit is used to modify current limits based on output voltage. When load resistance drops to 0, the current is limited based on output voltage. When load resistance drops to 0, the current limit is 0.79A resulting in an internal dissipation of 33.3 W. When output voltage increases to 36V, the current limit is 1.69A. Refer to Application Note 9 on foldover limiting for details.

## EXTERNAL CONNECTIONS



# PA10 • PA10A

## ABSOLUTE MAXIMUM RATINGS SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	67W
INPUT VOLTAGE, differential	$\pm V_S - 3V$
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction <sup>1</sup>	200°C
TEMPERATURE RANGE, storage	-65 to +150°C
OPERATING TEMPERATURE RANGE, case	-55 to +125°C

### SPECIFICATIONS

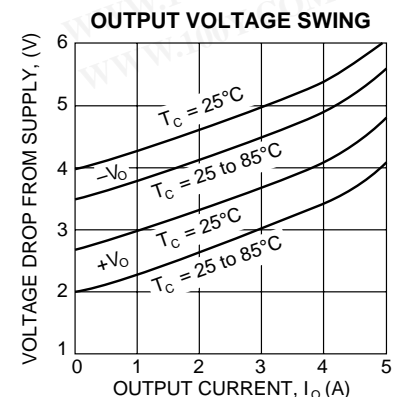
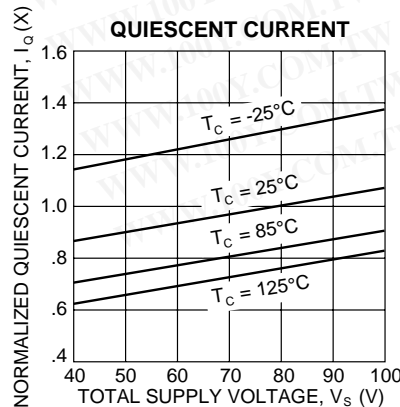
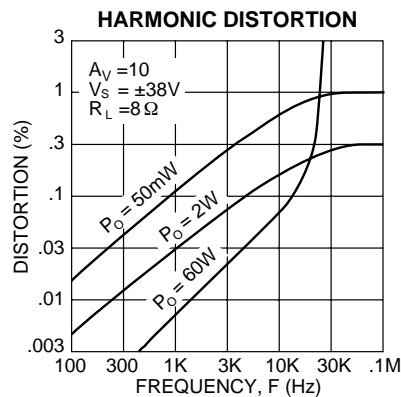
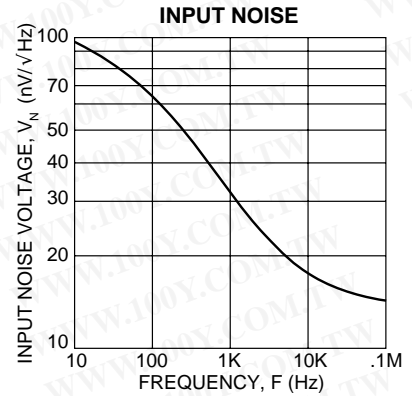
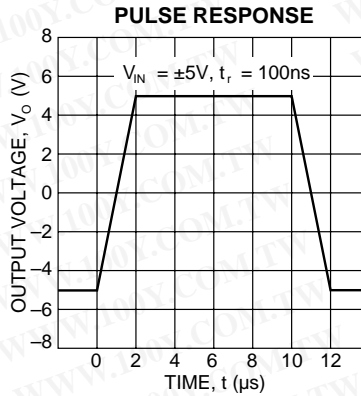
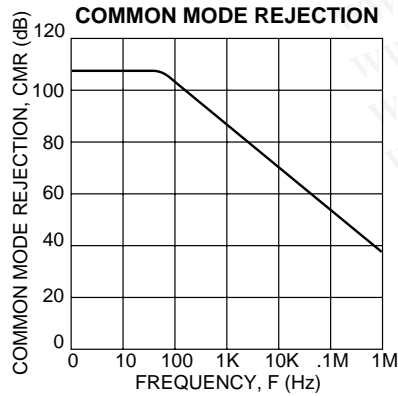
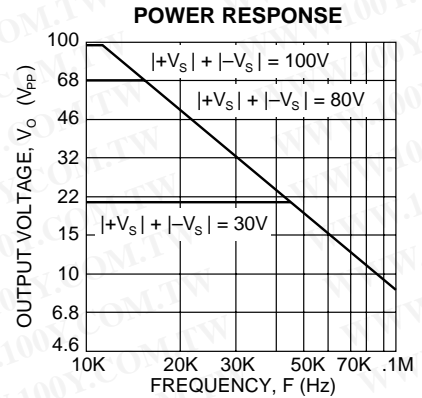
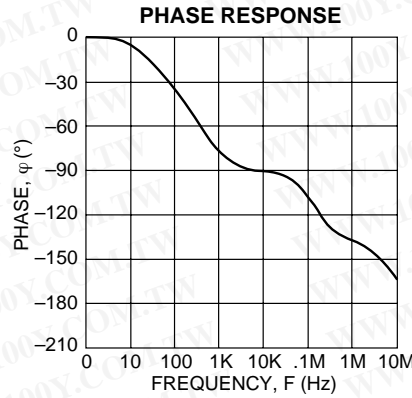
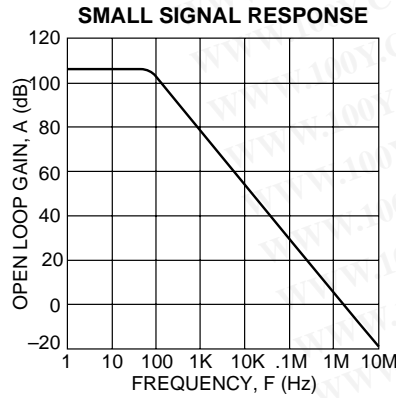
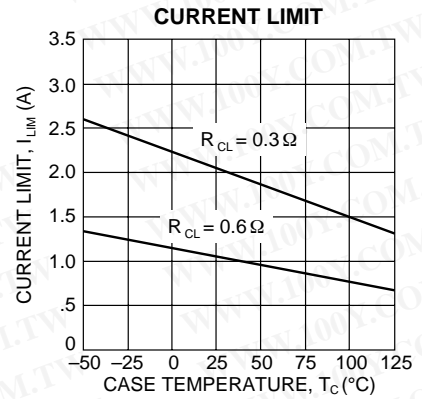
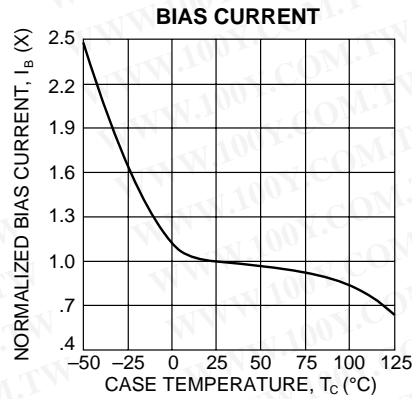
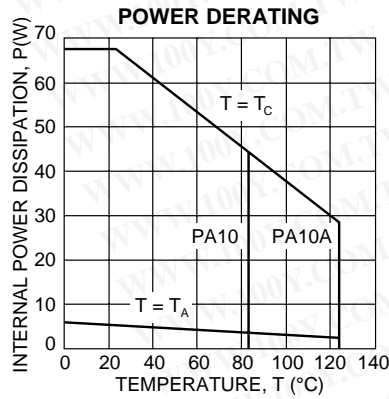
SPECIFICATIONS		PA10			PA10A			
PARAMETER	TEST CONDITIONS <sup>2, 5</sup>	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T <sub>C</sub> = 25°C		±2	±6		±1	±4	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	μV/°C
OFFSET VOLTAGE, vs. supply	T <sub>C</sub> = 25°C		±30	±200		*	*	μV/V
OFFSET VOLTAGE, vs. power	T <sub>C</sub> = 25°C		±20			*		μV/W
BIAS CURRENT, initial	T <sub>C</sub> = 25°C		12	30		10	20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T <sub>C</sub> = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T <sub>C</sub> = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T <sub>C</sub> = 25°C		200			*		MΩ
INPUT CAPACITANCE	T <sub>C</sub> = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE <sup>3</sup>	Full temperature range	±V <sub>S</sub> -5	±V <sub>S</sub> -3		*	*		V
COMMON MODE REJECTION, DC <sup>3</sup>	Full temp. range, V <sub>CM</sub> = ±V <sub>S</sub> -6V	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T <sub>C</sub> = 25°C, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 15Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T <sub>C</sub> = 25°C, 15Ω load		4			*		MHz
POWER BANDWIDTH	T <sub>C</sub> = 25°C, 15Ω load	10	15		*	*		kHz
PHASE MARGIN	Full temp. range, 15Ω load		20			*		°
OUTPUT								
VOLTAGE SWING <sup>3</sup>	T <sub>C</sub> = 25°C, I <sub>O</sub> = 5A	±V <sub>S</sub> -8	±V <sub>S</sub> -5		±V <sub>S</sub> -6	*		V
VOLTAGE SWING <sup>3</sup>	Full temp. range, I <sub>O</sub> = 2A	±V <sub>S</sub> -6			*			V
VOLTAGE SWING <sup>3</sup>	Full temp. range, I <sub>O</sub> = 80mA	±V <sub>S</sub> -5			*			V
CURRENT, peak	T <sub>C</sub> = 25°C	5			*			A
SETTLING TIME to .1%	T <sub>C</sub> = 25°C, 2V step		2			*		μs
SLEW RATE	T <sub>C</sub> = 25°C	2	3		*	*		V/μs
CAPACITIVE LOAD	Full temperature range, A <sub>V</sub> = 1			.68			*	nF
CAPACITIVE LOAD	Full temperature range, A <sub>V</sub> = 2.5			10			*	nF
CAPACITIVE LOAD	Full temperature range, A <sub>V</sub> > 10			SOA			*	nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	T <sub>C</sub> = 25°C	8	15	30	*	*	*	mA
THERMAL								
RESISTANCE, AC, junction to case <sup>4</sup>	T <sub>C</sub> = -55 to +125°C, F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	T <sub>C</sub> = -55 to +125°C		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air	T <sub>C</sub> = -55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	-55		+125	°C

NOTES: \* The specification of PA10A is identical to the specification for PA10 in applicable column to the left.

- Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
- The power supply voltage for all tests is  $\pm 40$ , unless otherwise noted as a test condition.
- $+V_S$  and  $-V_S$  denote the positive and negative supply rail respectively. Total  $V_S$  is measured from  $+V_S$  to  $-V_S$ .
- Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
- Full temperature range specifications are guaranteed but not tested.

### CAUTION

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.





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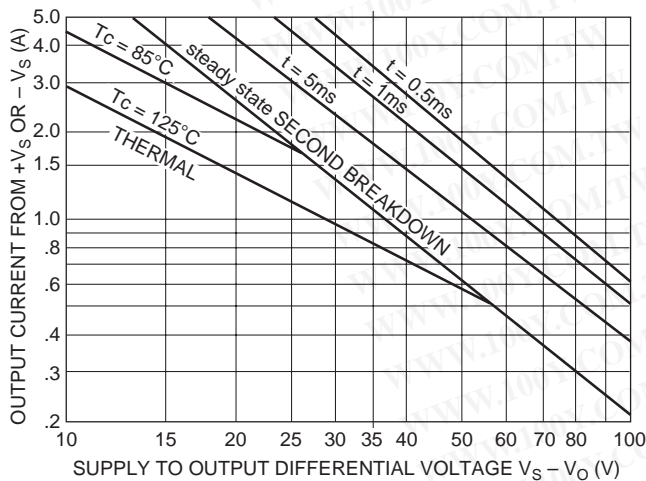
## GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit [www.apexmicrotech.com](http://www.apexmicrotech.com) for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads.

1. For DC outputs, especially those resulting from fault conditions, check worst case stress levels against the new SOA graph.

For sine wave outputs, use Power Design<sup>1</sup> to plot a load line. Make sure the load line does not cross the 0.5ms limit and that excursions beyond any other second breakdown line do not exceed the time label, and have a duty cycle of no more than 10%.

For other waveform outputs, manual load line plotting is recommended. Applications Note 22, SOA AND LOAD LINES, will be helpful. A Spice type analysis can be very useful in that a hardware setup often calls for instruments or amplifiers with wide common mode rejection ranges.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at Tc = 85°C:

$\pm V_s$	SHORT TO $\pm V_s$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.21A	.61A
40V	.3A	.87A
35V	.36A	1.0A
30V	.46A	1.4A
25V	.61A	1.7A
20V	.87A	2.2A
15V	1.4A	2.9A

## CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Visit the Apex web site at [www.apexmicrotech.com](http://www.apexmicrotech.com) for a copy of the Power Design spreadsheet (Excel) which plots current limits vs. steady state SOA. Beware that current limit should be thought of as a  $\pm 20\%$  function initially and varies about 2:1 over the range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

For fixed current limit, leave pin 7 open and use equations 1 and 2.

$$R_{CL} = 0.65 / I_{CL} \quad (1)$$

$$I_{CL} = 0.65 / R_{CL} \quad (2)$$

Where:

$I_{CL}$  is the current limit in amperes.

$R_{CL}$  is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 7 and use equations 3 and 4.

$$I_{CL} = \frac{0.65 + (V_o * 0.014)}{R_{CL}} \quad (3)$$

$$R_{CL} = \frac{0.65 + (V_o * 0.014)}{I_{CL}} \quad (4)$$

Where:

$V_o$  is the output voltage in volts.

Most designers start with either equation 1 to set  $R_{CL}$  for the desired current at 0v out, or with equation 4 to set  $R_{CL}$  at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor ( $R_{FO}$ ) between pin 7 and ground. Use equations 4 and 5 with this new resistor in the circuit.

$$I_{CL} = \frac{0.65 + \frac{V_o * 0.14}{10.14 + R_{FO}}}{R_{CL}} \quad (5)$$

$$R_{CL} = \frac{0.65 + \frac{V_o * 0.14}{10.14 + R_{FO}}}{I_{CL}} \quad (6)$$

Where:

$R_{FO}$  is in K ohms.

<sup>1</sup> Note 1. Power Design is a self-extracting Excel spreadsheet available free from [www.apexmicrotech.com](http://www.apexmicrotech.com)